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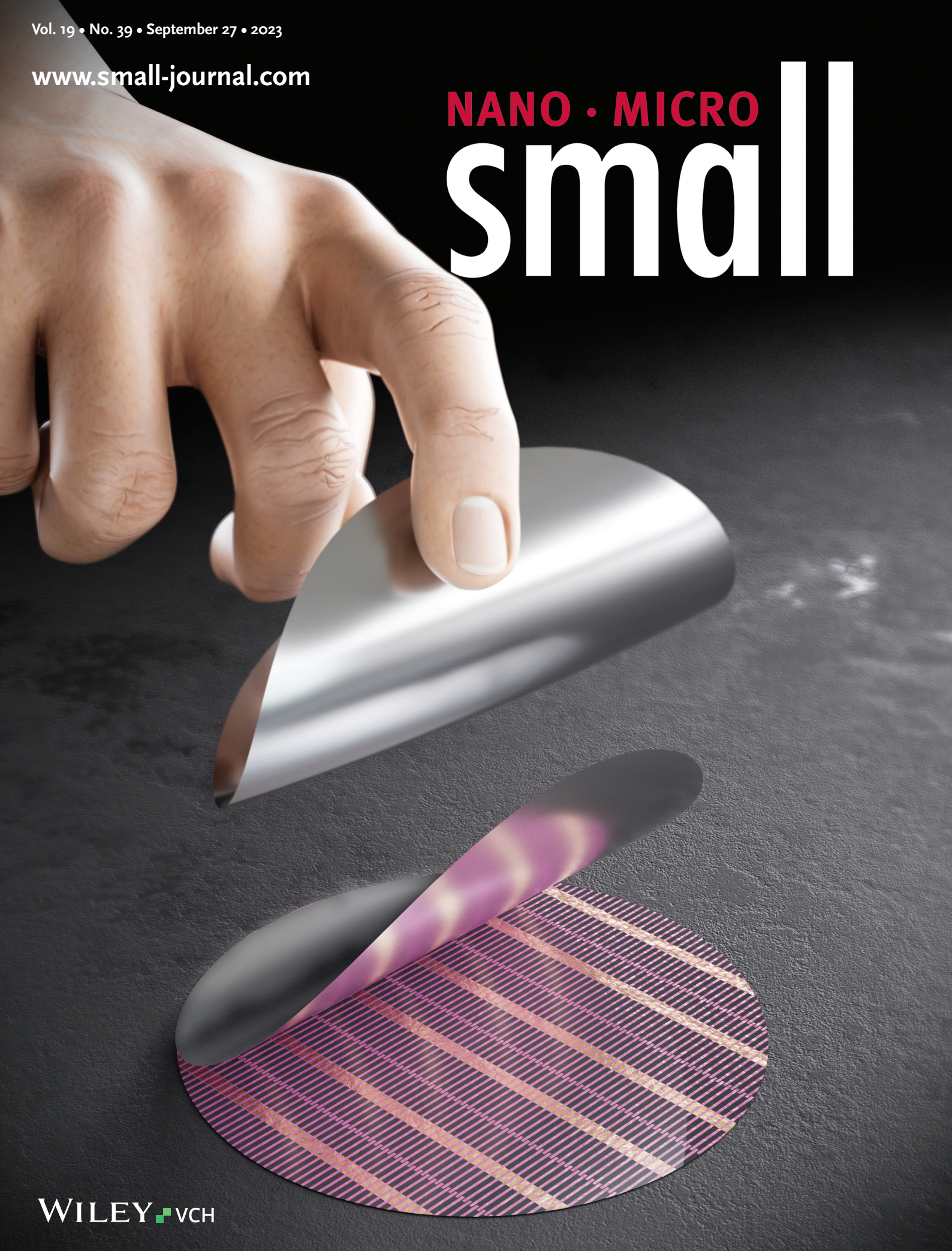

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RESEARCH ARTICLE

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Ultrathin Crystalline Silicon Nano and Micro Membranes with High Areal Density for Low-Cost Flexible Electronics

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Ultrathin crystalline silicon is widely used as an active material for high-performance, flexible, and stretchable electronics, from simple passive and active components to complex integrated circuits, due to its excellent electrical and mechanical properties. However, in contrast to conventional silicon wafer-based devices, ultrathin crystalline silicon-based electronics require an expensive and rather complicated fabrication process. Although silicon-on-insulator (SOI) wafers are commonly used to obtain a single layer of crystalline silicon, they are costly and difficult to process. Therefore, as an alternative to SOI wafers-based thin layers, here, a simple transfer method is proposed for printing ultrathin multiple crystalline silicon sheets with thicknesses between 300 nm to 13 µm and high areal density (>90%) from a single mother wafer. Theoretically, the silicon nano/micro membrane can be generated until the mother wafer is completely consumed. In addition, the electronic applications of silicon membranes are successfully demonstrated through the fabrication of a flexible solar cell and flexible NMOS transistor arrays.

1. Introduction

In recent decades, flexible electronics have demonstrated their functionalities in various forms, resulting in innovative advancements in diverse electronic systems such as flexible displays,[1-3] healthcare monitoring,[4,5] e-skin sensors,[6,7] wearable electronics,[8–10] and implantable devices,[11-14] which were previously impossible to demonstrate with conventional rigid-based electronics. As a result of the development of flexible electronics, the constituent materials and manufacturing techniques for flexible electronics have undergone continuous improvement to maintain their high electrical performance despite substantial mechanical deformation. Among various electronic materials, ultrathin semiconducting materials with high electrical performance are primarily

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considered, and the efforts of thinning down these materials with various methods (i.e., top-down and bottom-up approaches) contribute to the fabrication of flexible electronics.[15–19]

Active, flexible electronics rely heavily on inorganic and organic semiconductors. The superior electrical, optical, and thermal properties of group IV single-element semiconducting materials, III–V compound semiconducting materials, and metal oxide semiconductors were highlighted in previous research.[20–23] With these inorganic materials, fine thickness adjustment and high reproducibility of fabrication were also possible due to their deposition-based fabrication process. Even though III–V compound semiconducting materials, such as GaN, GaAs, InP, and InSb, exhibit exceptional optoelectronic properties, the epitaxial growth technique primarily used to grow these materials frequently results in lattice mismatch or thermal expansion coefficient mismatch.[24] In addition to these mechanical misfit issues, their deposition method is dependent on high-vacuum equipment, such as molecular beam epitaxy and metal–organic chemical vapor deposition.[25] Conversely, oxide semiconductors, such as ZnO, IGO, and IGZO, require a relatively simple manufacturing process, but their electrical mobility lags significantly behind inorganic semiconductors.[26,27]

In contrast, organic semiconductor devices have attracted interest owing to their excellent mechanical properties (low Young's modulus), ease of fabrication, and compatibility with flexible substrates. These advantages have expanded the applications of semiconductors to include flexible or even stretchable electronics. However, poor electrical performance, low thermal durability, and low electrical stability of organic semiconductors continue to hinder the development of flexible electronics based on organic semiconductors.[16,28–31] Carbon-based materials such as graphene, graphene oxide, reduced graphene oxide, and carbon nanotube have received a great deal of attention because of their exceptional electronic, optical, thermal, and mechanical properties resulting from their unique structures.[32,33] These materials can be synthesized using various methods including graphite exfoliation, laser ablation, and chemical vapor deposition. Despite the development of these methods for mass production, the high cost of methods and the lack of uniformity are still major challenges for their practical applications.[34–37]

Silicon (Si), as a single-element semiconductor, is still regarded as irreplaceable and promising among all semiconducting materials thanks to its high electrical performance and well-established and inexpensive manufacturing process. Single-crystalline Si exhibits excellent electrical, mechanical, and optical properties. Although the bending stiffness of bulk Si is extremely high, it can be drastically reduced by thinning the material.[38–43] Therefore, numerous studies have developed ultrathin single-crystalline Si-based flexible electronics.

Representative transfer methods were introduced to establish a single-crystalline Si membrane on a flexible substrate, with novel applications including lightweight devices,[44,45] bendable or foldable devices,[42,46,47] wearable devices,[9,14,48] implantable devices,[49–51] and photovoltaic devices.[52–54] A silicon-on-insulator (SOI) wafer was utilized to transfer a single-crystalline Si membrane on a flexible substrate. This wafer is composed of thin Si (on top), a buried oxide layer (in the middle), and bulk Si (at the bottom), so that after defining the hole array patterns on the top Si layer, the burried oxide layer (BOX) can be selectively etched away to release the Si membrane by dipping the wafer in hydrofluoric acid (HF). However, S wafers are more expensive than bulk Si wafers and only permit the transfer of the top Si membrane from the SOI wafer once. In addition, since the Si layer thickness is a product specification, it is impossible to obtain a thickness higher than the specification. To overcome these limitations, numerous researchers have attempted to detach a thin Si membrane from a bulk wafer by forming a scalable nano/micro ribbon structure and fabricating a flexible photovoltaic or a transistor.[55–59] However, the nano/micro scale ribbon structure limited the applicability of the detached Si membrane because the transferred Si membrane is composed of isolated individual cells that form sparse arrays with a loss of effective device area, making it difficult to form a high-density electrodes array (e.g., integrated circuits, photodetector arrays). In addition, the width of the existing nanoribbon has a short length of less than 10 μm, and the distance between ribbon cells is on a scale of several micrometers. Due to the limitations of the ribbon width and distance between cells, to create a single cell with a length of 100 μm, at least 10 cells must be connected, and even when the cells are connected, the arrays still have a low areal fill factor.

Here, we present a method for fabricating multiple silicon nano/micro membrane sheets (SiNMMS) from a single mother wafer, as well as applications for flexible Si electronics. Designing interlocking and anchoring connections between densely packed Si microbar cells to form a single large membrane with a high areal density is a key technology for forming SiNMMS. Also, a horizontal undercut is performed beneath the Si layer using an anisotropic wet etch process with a user-adjustable thickness between a few hundred nanometers and tens of micrometers,

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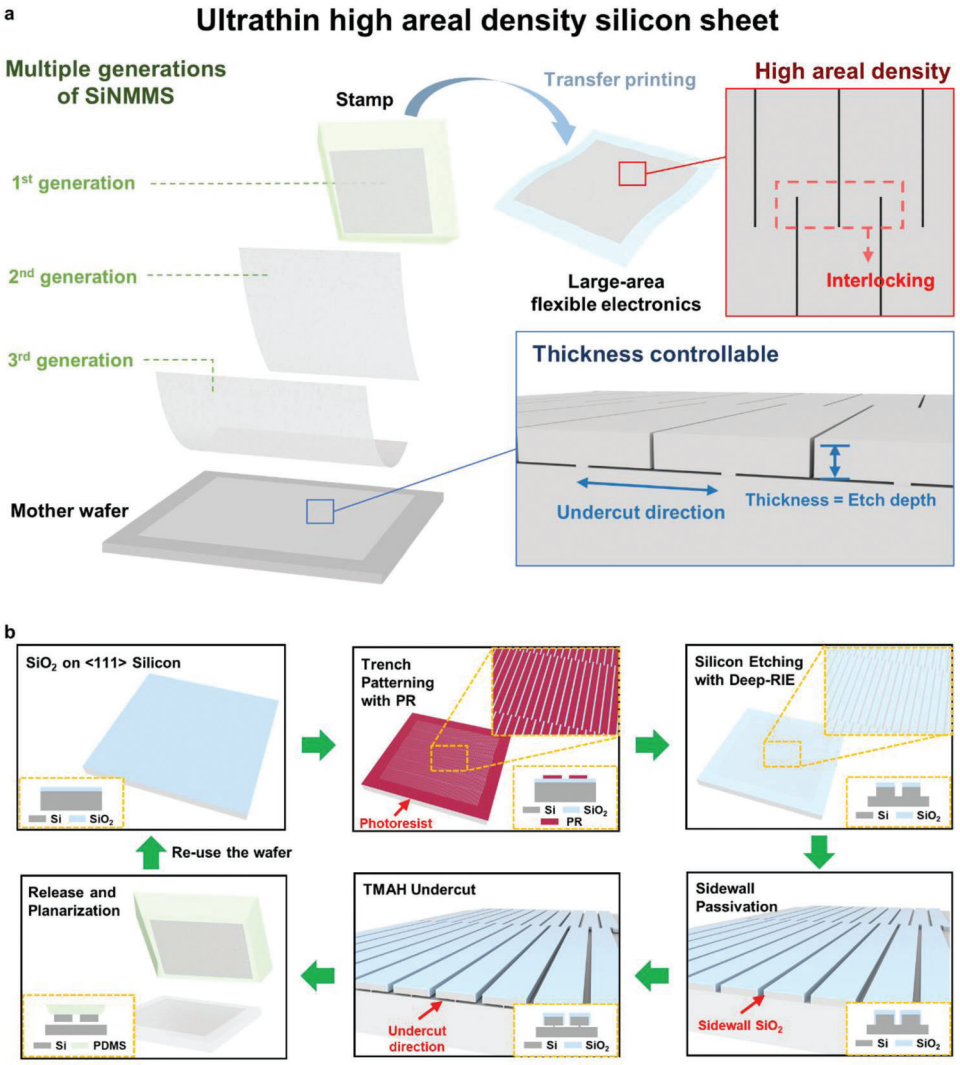

Figure 1. Advantages and transfer process of ultrathin nano and micro membranes of crystalline silicon sheet. a) Schematic diagram presenting three advantages of SiNMMS: 1) multiple generations, 2) high areal density, 3) thickness controllable. Interlocking design, undercut direction, and thickness are marked on the figure. b) Schematic illustration of the overall fabrication process of high areal density silicon nano/micro-membrane sheet (SiNMMS).

like a selective buried oxide layer etch process in an SOI wafer. By adjusting the thickness by reactive ion etching (RIE) and the patterning of the areal dimensions, we can maximize the areal density (>90%) of a nanomembrane sheet using this method. In addition, as we can acquire a membrane with a sheet-like structure, the subsequent applications are expanded from a single electrode array to include a transistor, integrated circuits, etc. By modulating external doping concentrations and their dimensions, SiNMMS could produce a diverse range of flexible active devices. These high-quality SiNMMS can be generated multiple times at a low cost and with the same level of quality as membrane sheets produced from SOI wafers by planarizing the wafer until the mother wafer is completely consumed. Here, to validate the device applications of SiNMMS, a flexible solar cell and flexible transistor arrays were successfully fabricated directly on SiNMMS and their electrical properties were evaluated.

2. Results and Discussion

2.1. Advantages and Fabrication Process of SiNMMS

Figure 1a shows multiple generations of a thickness-controllable SiNMMS with high areal density and the transfer of large-area SiNMMS on a flexible substrate. The key advantages of this technology are that specifications of SiNMMS, areal density, and thickness, can be determined by adjusting the size and etching thickness of the trench pattern. A detailed explanation about controlling the areal density and thickness of SiNMMS is mentioned in Section 2.2. Figure 1b presents the overall SiNMMS transfer fabrication procedure that begins with the preparation of <111> direction Si wafer.

In order to wet etch the sidewalls of a <111> Si wafer with potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) solutions,[56–58] the trench of the wafer was vertically

patterned to the <110> planar direction. In the case of <111> direction Si, the atoms are densely packed. This leads to two orders of magnitude slower etching rate compared to the <110> plane when exposed to alkaline solutions such as KOH or TMAH. The slower etching rate in the <111> direction can be attributed to both higher backbond surface states and a lower density of dangling bonds. The higher backbond surface states in the <111> plane contribute to its increased mechanical stability compared to the <110> plane. These surface states affect the overall reactivity and etching behavior of the surface. Additionally, the lower density of dangling bonds on the <111> plane reduces the number of reactive sites available for the etchant solution to interact with, further contributing to the slower etching rate.[60–62] The trench pattern between each Si microbar cell is a key technology in the SiNMMS fabrication procedure. The trench pattern forms multiple interlocking and anchoring designs, connecting each Si microbar to a single, large Si membrane. Next, the Si is anisotropically etched to the desired nano/micro membrane thickness using a deep-RIE system while minimizing Si loss, yielding a membrane with a high areal density. During the undercut process, second thermal oxidation is performed to protect the sidewall from the TMAH solution. The undercut SiNMMS is released, and the remaining mother wafer is planarized using TMAH or KOH solutions to recover it as a reusable state for the subsequent generation of processes. For the undercut and planarization process, we immersed the wafer in TMAH or KOH solutions on a 110 °C hot plate, as those solutions etch Si mostly in a direction of <110>. Multiple SiNMMS are generated from a single mother wafer by repeating this cycle, resulting in high cost-efficiency. Various adhesive materials, such as SU-8, polyimide (PI), or photocurable polymer, can be used to transfer the released SiNMMS to various existing flexible substrates (Figures S1, S2, Supporting Information). Notes S1, S2 in Supporting Information describe the detailed SiNMMS transfer method.

This SiNMMS transfer method has the advantage that the transferred sheet membrane can be fabricated both into a large-scale electronic device and an array of electronic cells, which was a limitation of the nanoribbon transfer method. Furthermore, in conjunction with partial Si doping, this large-scale Si membrane process improves the applicability of active transistor arrays and solar cells. These advantages of low-cost SiNMMS could replace SOI wafer-produced membrane sheets.

2.2. Thickness and Areal Density Controllable SiNMMS

Trench-patterned Si wafer is designed to interlock and anchor each Si microbar, with a width and pitch of 12 μm and 62 μm, respectively (**Figure 2**a). Each trench pattern row is intended to vertically overlap the adjacent row by 60 μm, forming an interlocking design for stable SiNMMS transfer. Without this interlocking strategy in the trench pattern, SiNMMS is easily broken into a nano/micro bar shape during the undercut process. The overlapped area is set as described above to minimize the loss of Si areal density while preventing the disconnection of the Si membrane caused by undesirable Si cracks that may occur during the transfer process.

Figure 2b,c represents scanning electron microscope (SEM) images of the mother wafer before and after detaching the SiNMMS. At the top and bottom border lines, the end of the trench is designed with a square bracket shape, which facilitates the release of SiNMMS from a mother wafer. In addition, the surface roughness of the mother wafer after detachment was measured to ensure the reprocessability of the mother wafer following planarization. Atomic force microscope (AFM) result demonstrates that the surface roughness of the mother wafer is under 30 nm after planarization, proving the possibility of reusing the mother wafer for multiple transfer processes (Figure 2d,e).

Additional experiments have been conducted to increase the fill factor by reducing the width of the trench pattern. The fill factor of 12 μm-width trench patterned SiNMMS is 74% (Figure 2f). And the fill factor rose to 84% and 90% with 6 μm and 3 μm trench pattern widths, respectively (Figure 2g,h; Figure S3, Supporting Information). This result indicates that it is possible to control the areal density of SiNMMS by adjusting the width of the trench pattern.

Also, SiNMMS thickness can be precisely adjusted by controlling the number of cycles of the Bosch process with the STS-RIE system, resulting in various membrane thicknesses ranging from 300 nm to 7 μm (Figure 2i). Theoretically, if the thickness of the Si mother wafer is sufficient for the STS-RIE operation, it is possible to adjust the membrane thickness to Si mother wafer. Due to the trench pattern, it is confirmed that the SiNMMS is completely connected as a sheet form with the desired thickness. Prior to the transfer procedure, SEM images reveal two types of interconnected SiNMMS (300 nm and 7 μm) (Figure 2j).

2.3. Mechanical Characteristics and Multiple Generation of SiNMMS and Multiple Times of Transfer Printing

In general, the conventional transfer method utilizing an SOI wafer necessitates a hole arrangement pattern for etching the underlying BOX layer to allow a thin Si membrane to float.[42,63] Similar to the SOI wafer transfer process, the appearance of wrinkles on the surface of SiNMMS after the undercut process indicated its separation from a mother wafer (**Figure 3**a). After detaching from the wafer, SiNMMS is picked up by a PDMS stamp (Figure 3b). Next, SiNMMS is transferred onto a flexible substrate using the conventional transfer printing method with various substrates and adhesive layers. Finally, the SiNMMS on the flexible substrate is wrapped around a 7 mm-diameter rod to demonstrate its mechanical flexibility (Figure 3c).

It is essential to analyze the maximum bending strain in the Si sheet to achieve a small bending radius without exceeding the fracture limit (1%).[64,65] The thinness of single crystalline inorganic semiconductor membranes leads to low flexural rigidity and energy release rate, enabling a novel approach to multi-layer integration, distinct from traditional wafer bonding or epitaxy methods.[61] Also, a photocurable epoxy, SU-8, is spin coated after the transfer process to locate a brittle Si sheet layer near the neutral mechanical plane (NMP) for mechanical characterization and further applications. The finite element analysis (FEA) simulation of a 3-point bending test reveals the distribution of principal strain in Si sheet for x- and y-axis bending (Figure 3d,e). The maximum strain in the Si sheet during x (or y)-axis bending with a 2 mm radius is 0.86% (or 1%) (Figure 3f). Due to the smaller distance between the Si sheet and the NMP (18.3 μm for the x-axis

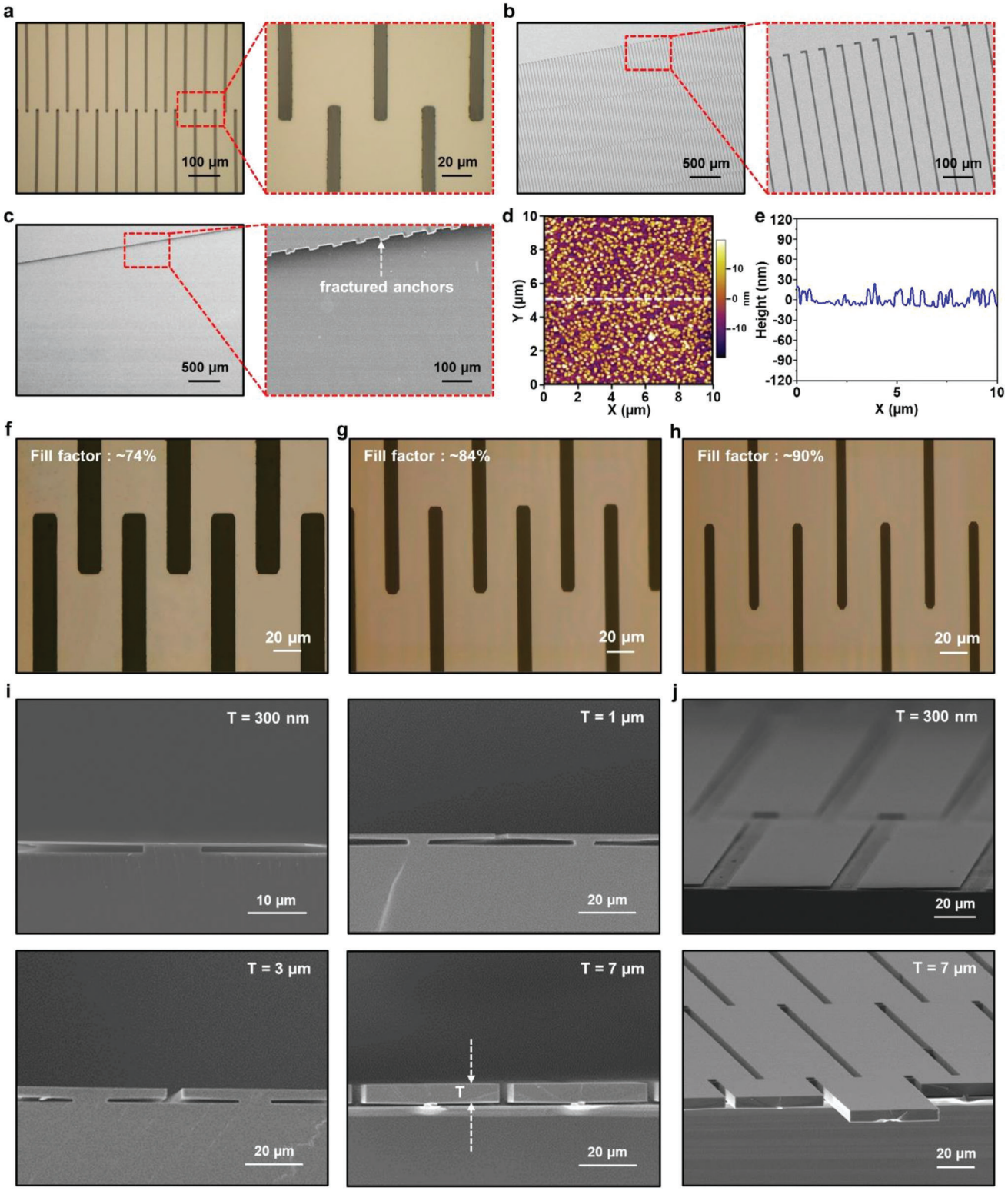

Figure 2. Design strategies for SiNMMS generation and controllability of areal density and thickness. a) Optical image of a trench pattern with a width of 12 μm and a pitch of 62 μm on SiNMMS released from a mother wafer. The overlapped region of the trench pattern enables the transfer of the Si membrane sheet. b) SEM image of the trench pattern terminal region. The square bracket shape is necessary for the smooth detachment of SiNMMS. c) SEM image of the mother wafer after SiNMMS detachment. d) AFM image of the mother wafer surface after planarization. e) Surface roughness of the mother wafer after planarization. d,e) The reprocessability of multiple uses of the wafer. f) Image of a 12 μm wide trench pattern with a fill factor of 74%. g) 6 μm width with 84% fill factor. h) 3 μm width with 90% fill factor. i) SEM images of the side view of SiNMMS. Each image depicts 300 nm, 1 μm, 3 μm, and 7 μm SiNMMS. j) SEM images of two types of interconnected SiNMMS (Thickness = 300 nm and 7 μm).

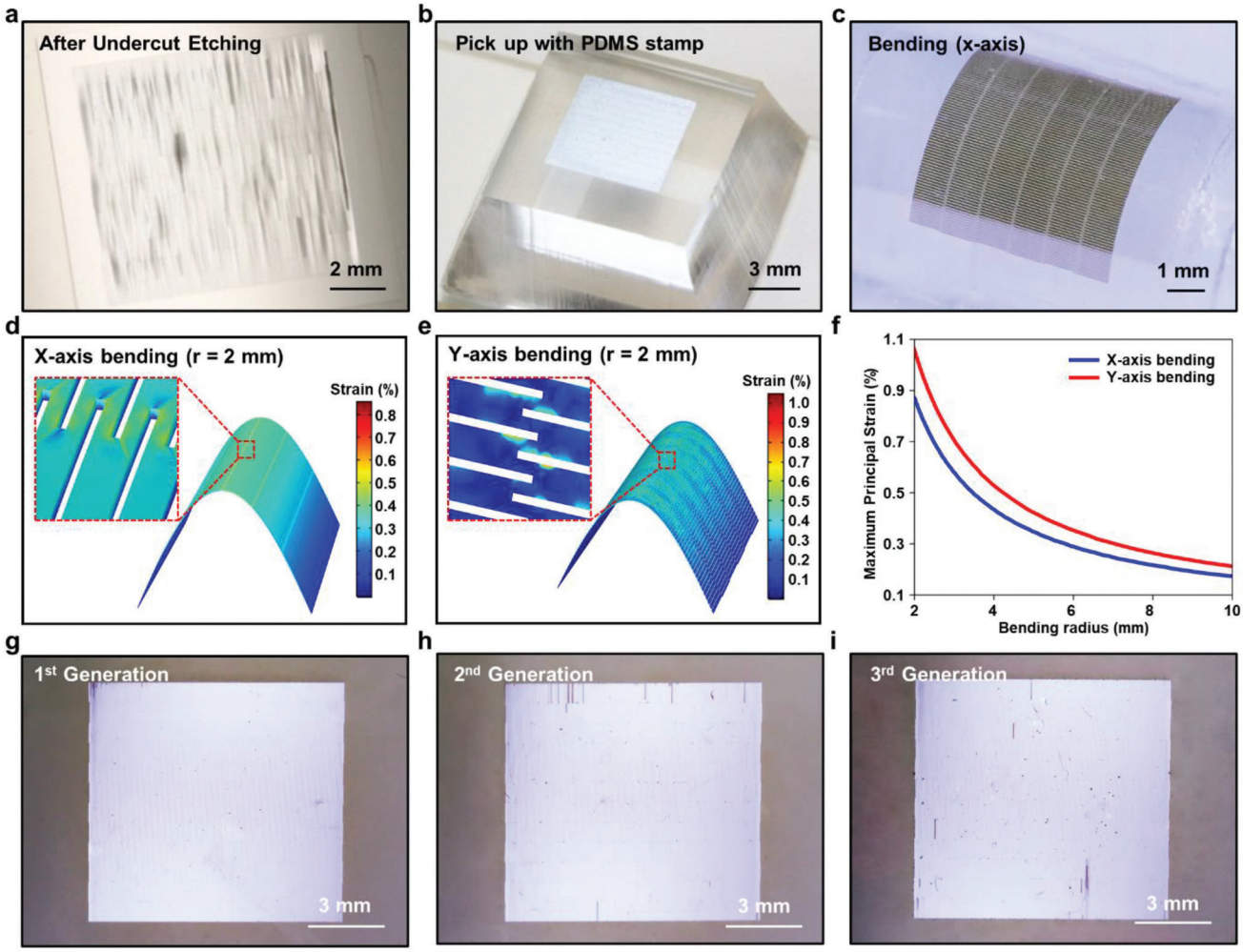

Figure 3. Mechanical characteristics and multiple generations of ultrathin crystalline silicon membrane. a) Photograph of the surface of the mother wafer following SiNMMS undercut etching. b) Photograph of SiNMMS after picked up with a PDMS stamp. c) Photograph of an SiNMMS on a flexible substrate wrapped around a rod (radius of 7 mm). It demonstrates the mechanical flexibility of SiNMMS without deformation. d) SiNMMS FEA simulation for *x*-axis bending. The maximum strain is 0.86%, less than the fracture limit (1%). e) SiNMMS FEA simulation for *y*-axis bending. The strain maximum is 1%. f) *X*-axis and *Y*-axis principal strain maximum based on bending radius. g–i) Multiple generations of 10 mm × 10 mm SiNMMS from a mother wafer.

bending and 27.5 μm for the *y*-axis bending), there is less strain in the *x*-axis bending (Detailed investigation for the mechanical analysis is explained in the method).

As stated in the introduction, conventional Si membrane transfer is not cost-effective because the method is based on expensive SOI wafers, and the Si membrane on the SOI wafer can only be generated once. This single-use limitation is due to the necessity of etching a sacrificial layer during the transfer process, and the SOI wafer contains only one such layer, the buried oxide layer. However, the transfer process introduced in this research uses the Si layer as a sacrificial layer, allowing for multiple transfer cycles. After one cycle of Si sheet transfer, the mother wafer can be reconditioned using TMAH or KOH solutions. These solutions etch Si in an anisotropic direction, allowing for the preparation of the wafer for the next generation cycle. In contrast, the mother wafer was reused and the 1st, 2nd, and 3rd generations of 10 mm × 10 mm size high areal density SiNMMS transferred on a flexible PET substrate were represented (Figure 3g–i).

2.4. 1st Application: A Flexible Solar Cell

This paper demonstrates the use of a flexible photovoltaic application with a high areal density Si micro membrane sheet. Si is the most commonly used material for solar cells due to its excellent electrical and optical properties and low cost.[66,67] There have been numerous attempts to maximize the power-to-weight ratio by thinning the Si wafer, ultimately leading to the fabrication of flexible solar cells to increase solar power efficiency.[68–72] Si micro membrane sheet transfer method-fabricated flexible solar cell consists of Si p–n junction, silver (Ag) electrode, PET/photocurable polymer substrate, and SU-8 encapsulation layers with a total thickness of 67 μm, while the Si sheet

thickness is 13 μm (**Figure 4**a,b; Figure S4, Supporting Information). The micro-thickness Si membrane consists of three vertical layers, p+ Si, p- Si, and n+ Si, to create a p–n junction for photovoltaic devices.

The fabrication of a flexible Si solar cell begins with the boron and phosphorus doping to produce the top p+ and n+ layers of the solar cell (Figure 4c). Trench patterning, undercutting, and bottom doping were then performed, along with sidewall passivation. The SiO_2 passivation layers on the top and sidewalls prevented undesired regions from being doped, while doping the undercut Si regions with boron to form a back surface field. The Si p–n junction was detached from the mother wafer using a PDMS stamp and then transferred onto a flexible PET substrate using a photocurable polymer. Lastly, Ag was deposited on both of the n+ and p+ sides to make contact with the doped region. After completing each step of the preceding method, flexible solar cells on a PET/photocurable polymer substrate were successfully fabricated (Figure 4d).

In Figure 4e, the current density–voltage (J–V) curves of a solar cell before and after applying a back surface reflector (BSR) are shown. All data were measured under AM 1.5G solar simulation conditions. Before applying BSR, the cell showed an open circuit voltage (V_{OC}) of 0.431 V, a short circuit current density (J_{SC}) of 20.23 mA cm^{-2}, a fill factor of 65.07, and a power conversion efficiency (PCE) of 5.68%. With BSR underneath the device, V_{OC} and J_{SC} of the device increased to 0.443 V and 27.72 mA cm^{-2}, while the fill factor decreased to 64.06, resulting in 7.87% of PCE with 38.7% increase compared to the device without BSR. Additionally, measurements of external quantum efficiency (EQE) under the same AM 1.5G solar spectrum conditions showed a similar integrated J_{SC} value of 26.72 mA cm^{-2} at 1100 nm wavelength (Figure 4f). The EQE data indicated that the quantum efficiency (QE) had a maximum value of 85% between 680–700 nm, and over 60% between 470–880 nm. The significant decrease in QE value at wavelengths above 900 nm was due to the thinness of the 13 μm Si, which has a limitation of low absorption rate at longer wavelength photons near the bandgap.[73] These results suggest that SiNMMS can be utilized as high-performance and high-areal-density photovoltaic devices.

2.5. 2nd Application: A Flexible Transistor Array

As a significant component of memory, displays, and active devices, the transistor is one of the most fundamental units in many areas of electronics. Particularly, Si-based transistors have been intensively researched due to their exceptional cost-effectiveness and superior electrical performance.[74–76] In addition, its flexibility has expanded its applications to include deformable displays, wearable electronics,[77–79] and biosensing systems.[80–82]

The exploded and cross-sectional views of n-type metal-oxide-semiconductor field-effect transistors (NMOSFETs) fabricated on a flexible Kapton film substrate with a flexible PI adhesive layer are depicted (**Figure 5**a,b). Si was doped to create source and drain regions except for the channel region (channel length, $L = 15$ μm, channel width, $W = 50$ μm, and total Si thickness = 300 nm). Al_2O_3 (26 nm) was deposited on top of the Si layer as a gate oxide layer, along with Cr/Au layers for source, drain, and gate contact electrodes.

Creating a partial doping region excluding channels on a <111> direction wafer is the first step in fabricating flexible transistors using an Si nanomembrane sheet transfer. Thermally grown SiO_2 (t-SiO_2) is formed for the partial doping mask of the source and drain area (Figure 5c). After n+ doping of the exposed Si area was completed, the t-SiO_2 doping mask was removed. Then, the trench patterning, sidewall passivation, and Si undercut steps were carried out. SiO_2 passivation layer was removed just before the release, and an Si nanomembrane sheet was detached and transferred onto a flexible Kapton film substrate using PI adhesive. Next, Al_2O_3 was deposited using atomic layer deposition (ALD) as the gate oxide layer of the transistor and contact vias were patterned to expose the Si layer of the source and drain region. For metallic contact, a Cr/Au layer was deposited via thermal evaporation, and the source, drain, and gate electrodes of each transistor were patterned. In total, 471 flexible transistors were fabricated on a 5 mm × 5 mm Si nanomembrane sheet.

Under 0.1 V drain/source voltage (V_{DS}) bias, the electrical performance of the fabricated flexible Si transistors was evaluated. The performance of the transistor was derived from drain current (I_D)-gate/source voltage (V_{GS}) curve using the standard NMOSFET model (mobility ≈ 241 cm^2 V^{-1} s^{-1}, on/off ratio ≥ 10^6, threshold voltage (V_{th}) ≈ 0.038 V, and subthreshold swings ≈ 212 mV dec^{-1}). Seven different gate voltage biases (V_G) were applied to measure the I_D–V_{DS} curve, and I_D exhibits well-behaved current saturation with increasing V_{DS} (Figure 5d). The V_{th} value shifted from 0.038 V to 1.26 V and 1.49 V as the NMOSFET was fabricated based on the 2nd and 3rd generated SiNMMS. Drain current at 5 V gate voltage was also decreased to 83.1% and 75% each, compared to the 1st generation NMOSFET (Figure 5e). Exposure to KOH or TMAH solutions damages the surface of crystalline Si, leading to the formation of impurities. These surface impurities subsequently induce defects at the Si-oxide interface, resulting in the charge trap. Ultimately, these trapped charges cause a shift in the threshold voltage of the transistor and a decrease in channel mobility, adversely affecting the performance of the device.[83–85] Despite slight performance degradation, multiple generated devices showed sufficient quality to be applied to practical applications. The issues of decreasing performance with multiple generations of the devices can be resolved through channel doping, gate oxide deposition techniques to reduce charge traps and optimization of chemical and mechanical polishing (CMP) to minimize the surface impurities.

3. Conclusion

In this article, we introduce a novel method for transferring a single-crystalline Si nano/micro membrane in sheet form. The process can be repeated multiple times on a single mother wafer until it is fully consumed, leading to high cost-efficiency. Also, the thickness ranging from 300 nm to 13 μm and areal density ranging from 74% to 90% of released SiNMMS can be tailored for the future applications. Transfer processes of sheets ranging in size from 5 mm × 5 mm to 10 mm × 10 mm were performed to demonstrate the scalability of this method with various pattern dimensions. Furthermore, the released SiNMMS were transferred onto various flexible substrates with suitable adhesive layers, demonstrating broad applicability of the method. Flexible solar cells and transistor arrays based on SiNMMS were

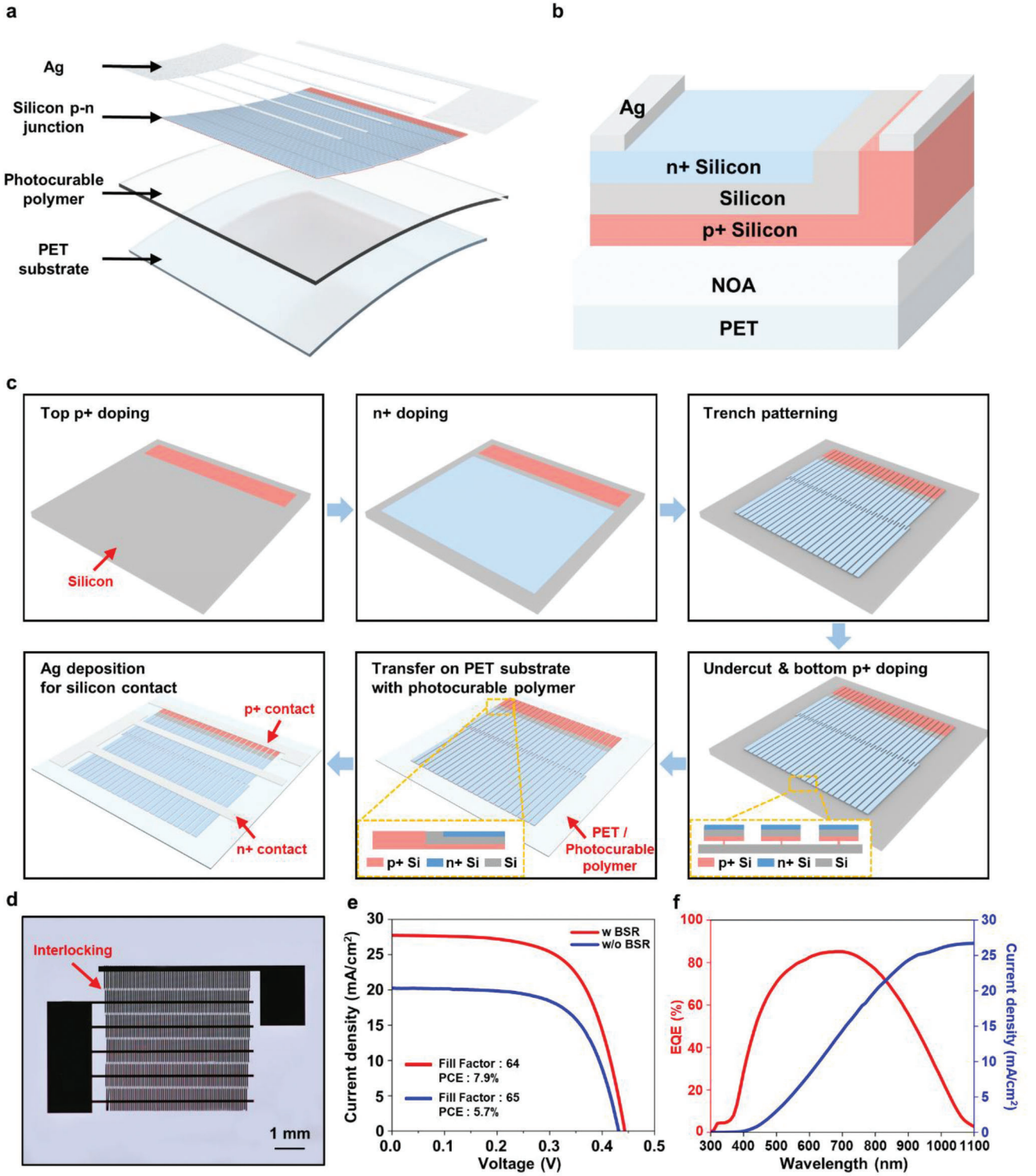

Figure 4. Flexible solar cell based on SiNMMS and its optical characteristics. a) An exploded view of a flexible Si p–n junction solar cell. b) Schematic illustration of an Si solar cell on a flexible PET/photocurable polymer substrate. c) Schematic illustration of the fabrication process of a flexible Si solar cell. d) Photograph of a fully manufactured 5 mm × 5 mm size flexible Si solar cell. e) Current density–voltage characteristic of a flexible Si solar cell (w BSR: fill factor = 64.06; open circuit voltage = 0.443 V; power conversion efficiency = 7.87%, w/o BSR: fill factor = 65.07; open circuit voltage = 0.431 V; power conversion efficiency = 5.68%). f) EQE spectrum of a flexible Si solar cell.

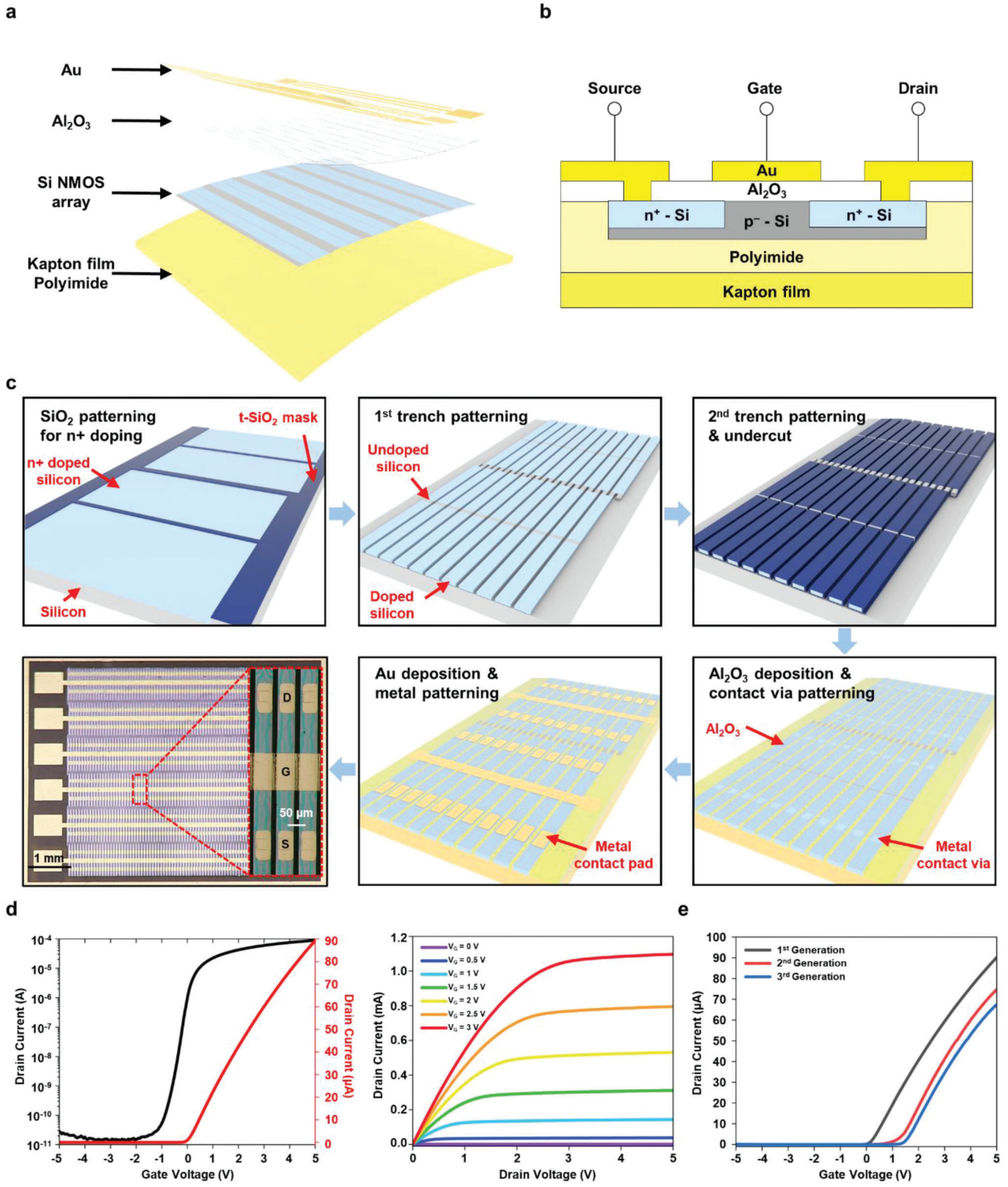

Figure 5. Flexible NMOSFET array based on SiNMMS and its electrical characteristics. a) An exploded view of the flexible Si NMOSFET array. b) Cross-sectional view of an Si NMOSFET on a flexible Kapton film substrate. c) Schematic illustration of the fabrication process of a flexible Si NMOSFET array and optical image of 471 flexible transistors in a 5 mm × 5 mm Si nanomembrane sheet. Inset shows an exploded optical image of 3 transistors (D, drain; G, gate; S, source). d) The transfer characteristics (I_D–V_{GS}) of a NMOSFET (V_{DS} = 0.1 V, V_{th} ≈ 0.038 V, on/off ratio ≥ 10^6) and the output characteristics (I_D–V_{DS}) of a NMOSFET (V_G = 0 V, 0.5 V, 1 V, 1.5 V, 2 V, 2.5 V, and 3 V). e) The transfer characteristics (I_D–V_{GS}) of multiple generation SiNMMS-based NMOSFET.

successfully fabricated from a single mother wafer, and the results suggest opportunities in the research areas of novel flexible inorganic electronics and unusual device applications.

4. Experimental Section

Materials and Equipment: <111> Si wafer (p-type, thickness = 525 ± 25 µm, resistivity = 1–10 Ω cm) was purchased from Prolog. Using hydrogen peroxide (H_2O_2, DUKSAN) and 94% sulfuric acid (H_2SO_4, DUKSAN), the Si wafer was piranha-cleaned. Here, 25 wt% TMAH dispersed in H_2O and anisotropic silicon <110> etchant was purchased from Sigma–Aldrich for the Si undercut process. Top and side views of the SiNMMS were observed using FE-SEM (IT-500HR). The transistor characteristics were acquired using a probe station (MST 5500B, MSTECH). The roughness of the Si wafer after transfer and planarization was measured by an atomic force microscope (AFM, NX-10, Park Systems). The characteristic of the photovoltaic device was measured using a solar simulator (Oriel Sol3A, Newport) and EQE measurement system (QEX10, PV measurements INC).

Silicon Sheet Transfer Fabrication Method: <111> Si wafer was cleaned with piranha solution (H_2SO_4:H_2O_2 = 3:1) at 130 °C for 20 min before being immersed in buffered oxide etchant (6:1 BOE, DUKSAN) to remove native oxide. The dry oxidation of a 200 nm t-SiO_2 layer was conducted in a furnace (EMF-60FA, EMS TECH) and the trench patterning process was processed. A positive photoresist layer (PR) (AZ 5214, AZ Electronic Materials, USA) was spin-coated at 3000 rpm with a spin coater (ACE-200, DONG AH TRADE CORP) for 30 s and then baked at 110 °C for 110 s. The trench pattern was defined by 8 s of UV exposure with the mask aligner and exposure system (MDA-400S(IM), MIDAS system) and 1 min of soaking in developer (AZ 300 MIF Developer, MERCK). The pattern of trenches was vertically aligned with the <110> plane direction. The exposed SiO_2 layer was removed using RIE (Q190620-M01, Young Hi-Tech) with CF_4/O_2 at 20/2 sccm and 150 W for 90 s and 6:1 BOE wet etching for 1 min. Stable SiNMMS with a large area and high areal density could be generated by designing each row of the trench pattern to partially overlap an adjacent row. STS-RIE (Omega LPX-DSI Etch System, Spts) with the Bosch process was conducted to anisotropically etch Si, and the etching time was controlled to achieve the desired thickness of the Si membrane. After the etching process, the Si wafer was cleaned again with acetone/IPA/DI rinsing and additional piranha solution to remove any residual PR and sidewall polymer produced from the Bosch process. The wafer was immersed in a boiling TMAH solution for 3 min to eliminate sidewall ripples caused by the Bosch process. Sidewall passivation of 80 nm t-SiO_2 was subsequently conducted through a second dry oxidation process. The t-SiO_2 layer of the trench was etched using RIE, and the wafer was then immersed in a boiling TMAH solution for 30 min (hotplate 110 °C) to undercut the bottom layer of SiNMMS (Figure S5, Supporting Information). TMAH solution etches Si in the <110> direction dozens of times faster than in the <100> direction, allowing Si to be etched anisotropically.[60–62] After the undercut, slide glass spin-coated with polydimethylsiloxane (PDMS, Dow corning) at 3000 rpm was prepared and 23-µm polyethylene terephthalate film (PET, GFM Korea) was laminated on it. The Si sheet was transferred to the PET substrate spin-coated with 500 rpm Norland optical adhesive 61 (NOA 61) (Edmund optics) using a PDMS stamp. NOA 61 served as an adhesive layer between the PET substrate and the Si sheet, as well as filling the vias created during the trench patterning procedure (Figure S6, Supporting Information). The PDMS stamp was removed from the PET substrate following the complete curing of NOA 61 for 100 s of UV exposure from both the top and bottom. Through the planarization process, the remaining Si wafer was recycled.

FEA Simulation Step: The Solid Mechanics model in COMSOL was used to simulate the 3-point bending analysis of the reusable Si sheet encapsulated by the SU-8 film. In the 3-point bending test, a vertical load applied to the center of the specimen was counterbalanced by the supports or boundary loads (represented by anti-symmetrical boundary constraints for faster convergence) at the two ends. The maximum bending strain ϵ_{max} is given by $\epsilon_{max} = y/r$, where r is the bending radius and y is the distance between the Si sheet and the NMP of the composite structure. The NMP location h_b can be determined using the formula:[86]

$$h_b^{x,y} = \frac{\sum_{i=1}^{n} E_{p,i} \times h_i \times h_{mi}}{\sum_{i=1}^{n} E_{p,i} \times h_i} \quad (1)$$

where $E_{p,i} = \frac{E_i}{1-\mu^2}$ is the plane-strain Young's modulus, μ is the Poisson's ratio, h_i is the average thickness of each layer ($i \leq n$) in the composite, and h_{mi} is given by $h_{mi} = \sum_{j=1}^{i} h_j - 0.5h_j$. The composite layup along the x- and y-axes was distinct, resulting in an orientation-dependent NMP location. As the thickness of the Si sheet increased to 9 µm (on top of the NOA with a thickness of 40 µm), the NMP location h_b shifted to 9.3 µm and 18.5 µm below the top surface of the NOA for the x- and y-axes bending, respectively. Therefore, the maximum principal strain for x-axis bending, 0.86%, was less than that for y-axis bending, 1%. The stress distribution across the thickness of the heterogeneous composite layup (Figure S7, Supporting Information) could also be used to determine the location of the NMP ($\sigma = 0$). The NMP for y-axis bending exhibited more pronounced undulations and was located further below the NOA top surface than the NMP for x-axis bending (Figure S8, Supporting Information), resulting in a greater maximum bending strain in the Si sheet (Figure S9, Supporting Information).

Solar Cell Fabrication: Single-crystalline <111> Si wafer was fabricated using the piranha cleaning method and dry oxidized to grow a 220 nm SiO_2 layer for a boron doping mask. The doping region was defined using conventional photolithography and the doping process was performed using a boron spin-on dopant (SOD, B153, Filmtronics) at 1000 °C for 30 min. Any undesired oxide was removed by soaking in hydrofluoric acid (HF, DUKSAN) for 1 min. A 180 nm SiO_2 layer was then dry oxidized for a phosphorous doping mask. The doping region was doped with a phosphorus SOD (P509, Filmtronics) at 1000 °C for 5 min. The unwanted oxide was removed by HF, and the residue was cleaned with piranha solution. Then, the same Si sheet transfer fabrication processed previously was continued until the undercut. After the undercut, the remaining SiO_2 that passivates the sidewall and top surface served as a boron doping mask. The bottom of the SiNMMS was doped with a boron SOD at 1000 °C for 30 min, and then the entire SiO_2 layer was removed by immersing in HF. The fabricated SiNMMS was released from the mother wafer using a PDMS stamp and subsequently transferred to a PET substrate with a photocurable polymer. Ag was deposited on the SiNMMS using a thermal evaporator (KVE-T2000, Korea Vacuum Tech) and photolithography was processed to define the contact pad. For the BSR, textured white paper was placed under the solar cell.

Transistor Fabrication: Single-crystalline <111> Si wafer was prepared using the piranha cleaning process and dry oxidized to obtain a 200 nm SiO_2 layer for the phosphorus doping mask. Conventional photolithography was processed to define the source and drain regions, followed by the t-SiO_2 etching and cleaning processes described previously. The doping process was performed in a furnace with phosphorus diffusion sources at 950 °C for 10 min and unwanted oxide was removed in HF. Then, the same method used for Si sheet transfer fabrication was applied to the transfer printing step with liquid polyimide (PI, Poly(pyromellitic dianhydride-co-4,4′-oxydianiline), amic acid solution, Sigma-Aldrich) coated Kapton film (25.6 µm, Dupont) (PI transfer method: Spin coating was conducted at 3000 rpm followed by pre-baking at 110 °C for 30 s; the resultant intermediate was attached to the receiver substrate, and post-baked at 110 °C for 1 min; PDMS stamp was then detached; PI hard baking was next conducted at 150 °C for 5 min and 220 °C for 2 h in a vacuum oven (SH-VDO-08NG, SH SCIENTIFIC)). 26 nm of Al_2O_3 was deposited as the gate oxide of the transistor by ALD (MOMAN), and conventional photolithography was processed to define contact vias for the source and drain electrodes. The contact vias were opened by etching the Al_2O_3 layer with 6:1 BOE for 15 s, and then the PR was cleaned with acetone. Using thermal

evaporation and photolithography, the source, drain, and gate electrodes were defined.

Statistical Analysis: Statistical analysis of graph data was plotted using Origin Lab software.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

J.Y.L., J.W.S., K.B.K., and J.E.J. have contributed equally to this work. The project was designed by J.Y.L., J.W.S., K.B.K., J.E.J., K.J.Y., and J.A.R. Device fabrication was performed by J.Y.L., J.W.S., K.B.K., J.E.J., and K.J.Y. The FEA simulation was performed by A.D. and H.Y.C. Data analysis was performed by J.Y.L., J.W.S., K.B.K., and J.E.J. The manuscript was written and edited by J.Y.L., J.W.S., K.B.K., J.E.J., K.J.Y., and J.A.R. All authors discussed the results and commented on the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

flexible electronics, reusable silicon, semiconductor electronics applications, silicon nano/micro membrane sheet transfer

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