

Three-Dimensional Silicon Electronic Systems Fabricated by Compressive Buckling Process

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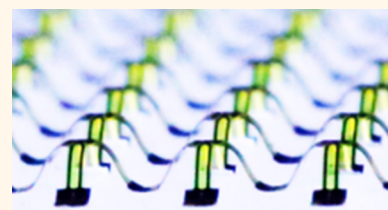
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Supporting Information

ABSTRACT: Recently developed approaches in deterministic assembly allow for controlled, geometric transformation of two-dimensional structures into complex, engineered three-dimensional layouts. Attractive features include applicability to wide ranging layout designs and dimensions along with the capacity to integrate planar thin film materials and device layouts. The work reported here establishes further capabilities for directly embedding high-performance electronic devices into the resultant 3D constructs based on silicon nanomembranes (Si NMs) as the active materials in custom devices or microscale components released from commercial wafer sources. Systematic experimental studies and theoretical analysis illustrate the key ideas through varied 3D architectures, from interconnected bridges and coils to extended chiral structures, each of which embed n-channel Si NM MOSFETs (nMOS), Si NM diodes, and p-channel silicon MOSFETs (pMOS). Examples in stretchable/deformable systems highlight additional features of these platforms. These strategies are immediately applicable to other wide-ranging classes of materials and device technologies that can be rendered in two-dimensional layouts, from systems for energy storage, to photovoltaics, optoelectronics, and others.

KEYWORDS: three-dimensional electronics, mechanical buckling, silicon transistor, silicon diode



Complex three-dimensional (3D) mesostructures are ubiquitous in nature, where architectural layouts are intimately related to overall function. Similar 3D

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concepts could provide powerful options in the design of microelectronic devices,^{1,2} optoelectronic components,^{3,4} energy storage systems,^{5–7} biomedical sensors, and microsurgical tools.^{8,9} Such possibilities serve as motivation for research into 3D fabrication/assembly processes such as 3D printing,^{10,11} multiphoton lithography,^{12–14} guided assembly,^{15–17} and origami/kirigami.^{18–22} Although certain of these approaches offer powerful capabilities, few combine design versatility and compatibility with the highly sophisticated 2D device structures and active materials that currently dominate existing microsystems technologies. The results reported here demonstrate strategies for embedding monocrystalline silicon nanomembrane (Si NM)-based device components, including transistors and diodes, into 3D open-mesh frameworks through advanced versions of recently reported approaches in deterministic assembly driven by processes of mechanical buckling.^{23–25} Here, 2D precursors formed using planar growth/deposition/transfer processes and microfabrication techniques, including examples that exploit released microscale components released from wafers processed in commercial silicon foundries, bond selectively at lithographically defined sites to a prestrained elastomer substrate. Release of the prestrain geometrically transforms these 2D systems into deterministically controlled 3D architectures, without adverse effect on the device performance. Examples presented here include 3D n-channel Si NM MOSFETs (nMOS) and diodes in networks of interconnected bridges and chiral structures. These demonstrations illustrate how concepts in 3D assembly can apply not only to advanced materials, as reported previously, but also to fully formed electronic devices with multilayer designs, thereby establishing clear paths to other classes of 2D technologies in optoelectronics, microelectromechanical systems, chem/bio sensors and others.

RESULTS AND DISCUSSION

Figure 1a presents a schematic illustration²⁶ of the mechanical buckling processes and related sequences in fabrication that enable the construction of silicon devices, including Si NM transistors (nMOS and pMOS) and arrays of diodes, in extended 3D architectures. The first step involves spin-casting a layer of poly(methyl methacrylate) (PMMA) followed by a layer of polyimide (PI) on a silicon (Si) wafer. Transfer printing delivers Si NMs with patterned regions of doping onto the surface of the PI. Si NMs, gate oxide, and metal electrodes are micropatterned by photolithography and dry/wet etching process (see the Experimental Section for details). Casting a coating of PI and forming a structure by RIE completes the fabrication of a 2D precursor circuit. Dissolving the PMMA with acetone releases the circuit onto a polydimethylsiloxane (PDMS) stamp. Evaporating layers of Ti/SiO₂ onto bonding sites on the backside of this platform prepares the system for integration onto an elastomer substrate with surface activated by exposure to ultraviolet induced ozone (UVO). Condensation reactions *via* exposed –Si–OH groups yield siloxane linkages (–O–Si–O–) and strong adhesion at the bonding sites;²⁷ weak van der Waals adhesion dominates in all other areas. Releasing the prestrain geometrically transforms the 2D system into a 3D architecture by a process of guided delamination and buckling of the nonbonded regions. The geometry of the 2D precursor, the locations of the bonding sites, and the magnitude and nature of the prestrain define the final 3D configuration.²⁸ Parts b and c of Figure 1 show schematic illustrations of 2D precursors to 3D architectures of Si NM nMOS transistors and diodes on an elastomer substrate. Optical microscope images in Figure 1d show Si NMs after

transfer printing onto PI (left), after depositing the gate oxide and wet etching (middle), and after metallization (right).

Figure 2 highlights an interconnected 3D bridge structure with Si NM nMOS transistors and bonding sites, and Figure 2a presents top and tilted-view optical microscope images. In general, long (1.55 mm), narrow (0.25 mm), and thin (3 μ m PI/100 nm Au/5 nm Cr/3 μ m PI) interconnects and small bonding sites (0.4 mm \times 0.4 mm) reduce the strain in the system, thus allowing the use of larger maximum prestrains in the assembly process. Here, the functional layers consist of Si, SiO₂, Cr, and Au located at the neutral mechanical plane of the multilayer stack to minimize the strain induced by bending. Mechanics simulations using finite element analysis (FEA; see the Experimental Section for details) indicate that, for an equi-biaxial prestrain of 100%, the peak strains remain much below the fracture strains (Si: \sim 1%, SiO₂: \sim 1.2%)^{29,30} or the yield strains (Cr: 0.3% and Au: 0.3%)³¹ of the active materials (Figure 2b). The result ensures that the deformations associated with 2D to 3D geometrical transformation are elastic and completely reversible. As shown in Figure 2a,b, the deformed configurations obtained by FEA agree with experiments without any parameter fitting.

Parts a and b of Figure 3 feature images and mechanical simulations for the case where the elastomer substrate is mechanically bent (radius \sim 2.5 mm) and slid. On the Si NM layer, the change of strain is from 0.2% to 0.21% during the bending process, then from 0.21% to 2.3% during the shearing process. Parts c and d of Figure 3 show transfer curves in linear scales and current–voltage characteristics of a representative Si NM transistor (channel lengths and widths of 20 and 80 μ m) on a flat elastomer substrate before and after the bending and shearing deformations. The mobility before and after the deformation (\sim 430 cm²/V s and \sim 450 cm²/V s, respectively) shows little change compared to that in the 2D layout.³² No significant changes occur in the threshold voltage (0.05 V) or the $I_{\text{on}}/I_{\text{off}}$ ratio ($>10^7$) before and after bending and shearing deformations (Figures S1 and S2).

Other 3D geometries and device types are also possible. As an example, Figure 4 shows a double-helical 3D structure that includes an array of Si NM diodes. The design principles and the assembly processes are similar to those for the table structure in Figure 2. Figure 4a presents top and tilted-view optical microscope images. Mechanics simulations indicate that for an equi-biaxial prestrain of 50% the deformations are purely elastic, as shown in Figure 4b. Parts c and d of Figure 4 present the electrical characteristics of a diode before (black) and after light exposure (red), indicating \sim 7 nA increments in off current.

These same concepts also allow for the formation of 3D interconnected mesostructures that include high performance silicon devices sourced from commercial CMOS foundries (XII0 SOI technology, X-FAB Semiconductor Foundries). The process in this case involves controlled release of fully formed, ultrathin (several micrometers) circuit microcomponents from the near surface of a completed wafer by anisotropic wet chemical etching. Assembly/integration of these components by transfer printing into 2D precursors allow their transformation into 3D architectures according to previously described processes (Figure 5a).^{33–35} In the example introduced here, the undercut yields pairs of body-tied silicon pMOS transistors, tethered by lithographically patterned anchors at each corner across trenches formed by wet etching of the underlying silicon wafer with the buried oxide as an etch stop, as shown in Figure 5b, for transfer printing (Figure 5c). Measurements from 3D silicon pMOS transistors reveal that their transfer characteristics (Figure 5d) and gate leakage

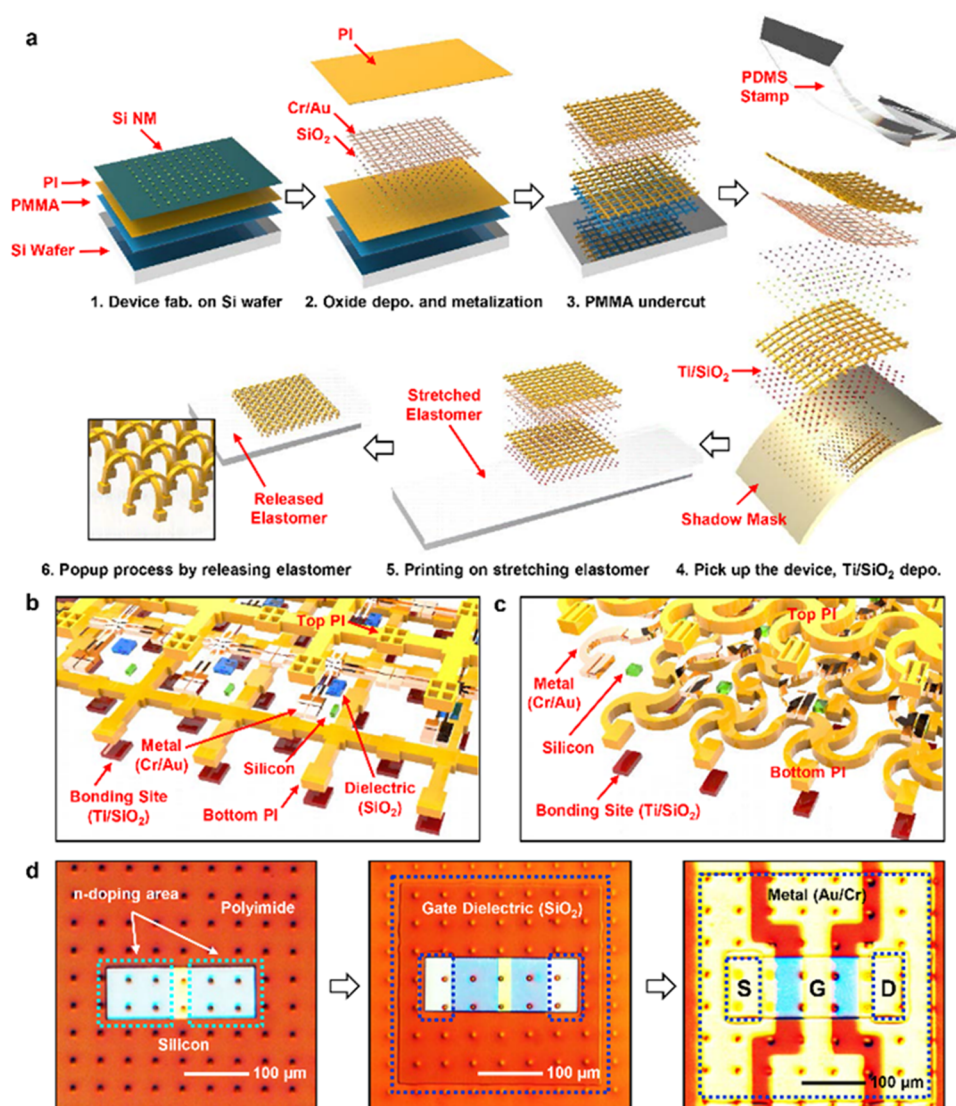


Figure 1. Materials and procedures for forming three-dimensional (3D) silicon nanomembrane (Si NM) devices on an elastomer substrate. (a) Schematic illustration for the fabrication of 3D Si NM nMOS transistors and diode arrays on a temporary substrate (top left) and for the deposition of gate oxide and metallization (top middle). Defining a mesh-type structure and then dissolving the PMMA layer allows release of a 2D circuit sheet (top middle). Retrieving the circuit onto a PDMS stamp enables deposition of Ti/SiO₂ onto lithographically defined bonding sites on the exposed backside surface (bottom right). Transfer printing delivers the system onto a prestretched elastomer substrate (bottom middle). Releasing the prestretching forms an engineered 3D architecture (bottom left). (b, c) Schematic illustrations of a 2D precursor to a 3D architecture of Si NM nMOS transistors and diodes on an elastomer substrate. (d) Optical microscope images of Si NMs transfer printed onto a layer of polyimide (left), after deposition of gate oxide and wet etching (middle), and after metallization (right).

levels (Figure 5e) are almost unaltered by the processing—from release to transfer printing to 2D precursor definition to geometrical transformation into 3D architectures—with on/off ratios as high as $\sim 10^7$ under a source-drain bias of 100 mV. The mobility is $210 \text{ cm}^2/\text{Vs}$ with subthreshold swing of 110 mV/decade, and V_{th} is -1.5 V (thickness of gate oxide = 25 nm, channel lengths and widths of 1 and 6 μm). Figure S3 shows log scale plots of the transfer curves and gate leakage of a representative silicon nMOS transistor on a flat elastomer substrate before and after the bending and shearing deformations.

CONCLUSION

The results presented here establish straightforward means to convert advanced 2D electronic systems into well-controlled, complex 3D architectures. The schemes are fully compatible with the most sophisticated materials and device designs in

conventional planar formats, thereby foreshadowing their use with other technologies, such as those in energy storage, photovoltaics, optoelectronics, and others. Heterogeneous collections of materials and multilayer, stacked geometries represent additional possibilities naturally compatible with a transfer printing based method for fabricating the 2D precursors. The presence of the elastomer substrate affords opportunities in reversible control of the 3D geometries through deformations of the supporting substrate. Collectively, these features suggest opportunities in integration with dynamic,³⁶ low modulus biological systems,^{37–39} as scaffolds, sensors, and/or actuators.^{40,41}

EXPERIMENTAL SECTION

Silicon nMOS Transistors in 3D Frameworks. Phosphorus doping at 950 °C defined highly doped areas for source and drain contacts on n-type silicon on insulator (SOI, top silicon $\sim 300 \text{ nm}$,

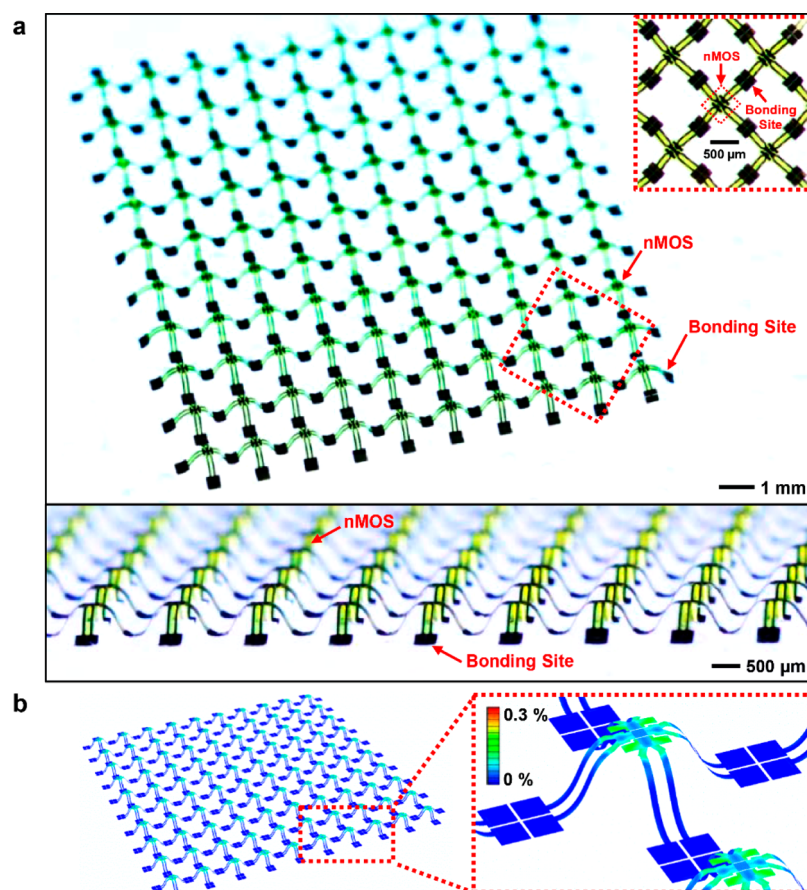


Figure 2. 3D-interconnected bridge structure with an array of Si NM nMOS transistors. (a) Optical microscope images of the final 3D system in top down and angled views. Magnified image (inset). (b) Finite element analysis results that define the 3D geometries and distributions of strain.

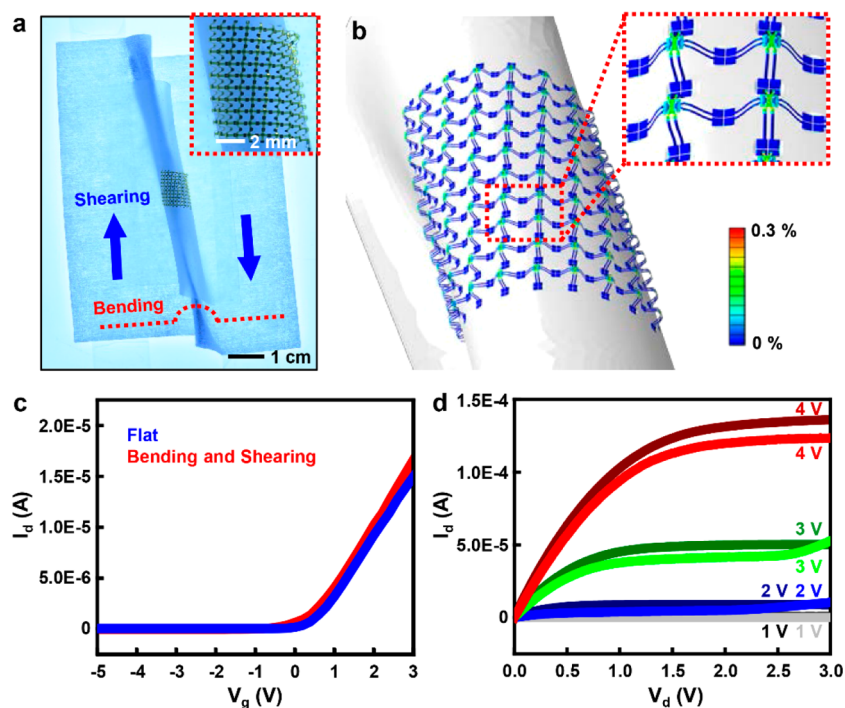


Figure 3. Images (a) and mechanical simulations (b) of bending (radius ~ 2.5 mm) and shearing the elastomer substrate. (c) Linear scale plots of transfer curves and (d) current–voltage characteristics of a representative Si NM nMOS transistor (channel length/width = $20/80 \mu\text{m}$) in the 3D system before (black, blue, green, and red) and after (gray, dark blue, dark olive, and brown) the bending and shearing process.

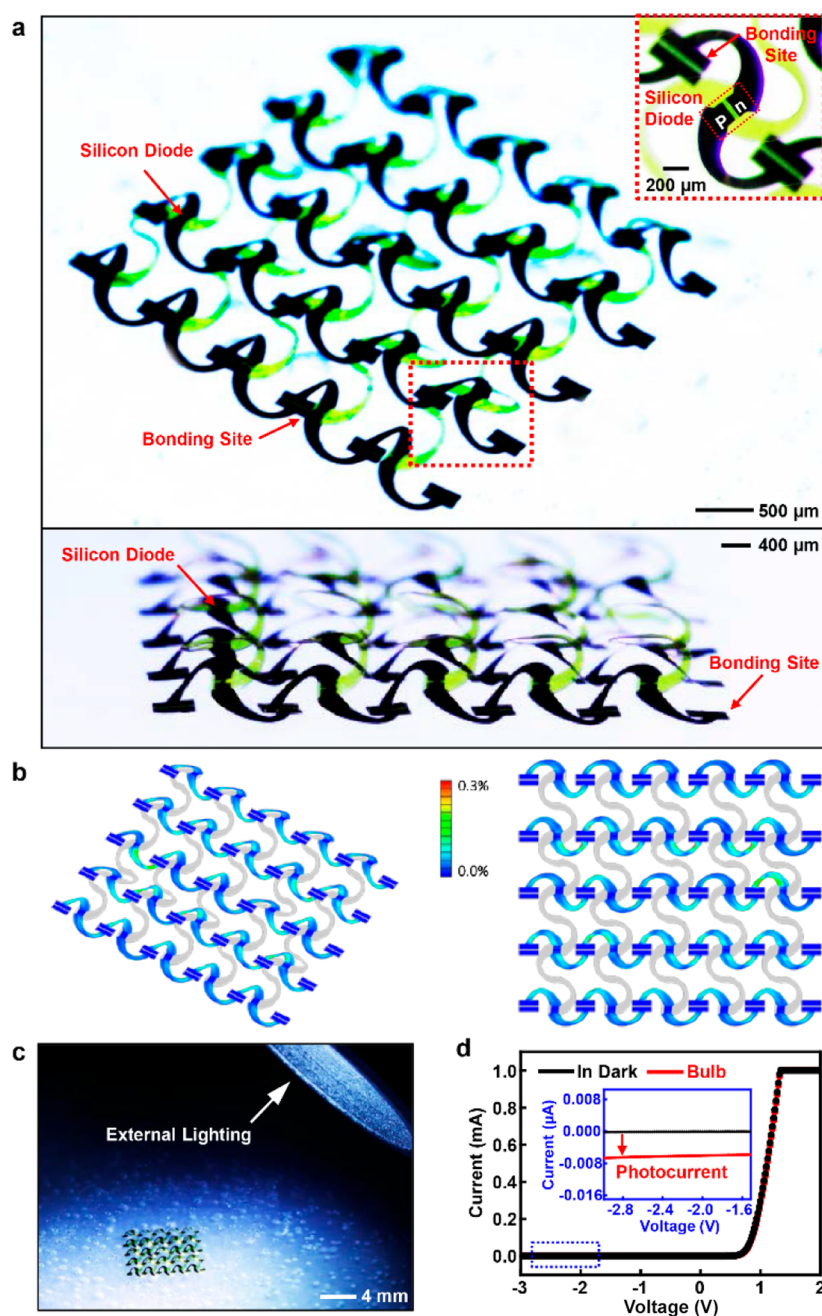


Figure 4. 3D-twisted chiral structure with an array of Si NM diodes. (a) Optical microscope images of the final 3D system in top down and angled views. Magnified image (inset). (b) Finite element analysis results that define the 3D geometries and distributions of strain. (c) Photograph of illumination of the system with an external light source. (d) Dark current and photocurrent graph of 3D silicon diode array in reversed bias state.

SOITEC, France) wafers for n-type transistors. Removal of the buried oxide by wet etching with HF released the top device silicon from the SOI, and enabled transfer printing of the resulting Si nanomembranes (NMs) onto spin-casted films of polyimide ($\sim 3 \mu\text{m}$, HD microsystems INC) and a sacrificial layer of PMMA ($\sim 100 \text{ nm}$, MicroChem INC) on a silicon wafer. Patterned regions of silicon resulted from photolithography and reactive ion etching (RIE, Plasmatherm, Inc., USA) with sulfur hexafluoride (SF_6 gas, 50 mTorr, 80 W, 30 sccm, 100 s) left silicon only in the active regions of the device. A thin layer of SiO_2 ($\sim 100 \text{ nm}$) formed by PECVD served as the gate dielectric. Creating openings in this layer using a buffered oxide etchant (Transene Company, Inc., USA) defined contact pads for source and drain electrodes. A 200/5 nm bilayer of Au/Cr, deposited by electron beam evaporation, served as source, drain, gate electrodes, as well as interconnects. Coating a thin layer of PI ($\sim 3 \mu\text{m}$)

as a passivation layer and forming a segmented, mesh structure by RIE (O_2 gas, 150 mTorr, 100 W, 20 sccm) completed the formation of a 2D precursor circuit composed of silicon devices and metal interconnects. Dissolving the PMMA layer with acetone released the circuit from the silicon wafer. Retrieving the circuit onto a PDMS stamp and then evaporating layers of Ti/ SiO_2 (3/30 nm) selectively onto bonding sites on the exposed backside surface prepared the system for localized strong adhesion onto a prestrained elastomer substrate pretreated by exposure to ultraviolet induced ozone (3 min). Releasing the prestrain led to geometrical transformation of the 2D precursor into a 3D configuration.

Silicon Diodes in 3D Frameworks. The fabrication began by defining phosphorus (1000 $^\circ\text{C}$, 10 min) and boron (1000 $^\circ\text{C}$, 20 min) doped regions on a silicon on insulator (SOI, top silicon $\sim 300 \text{ nm}$, SOITEC, France) wafer. The other steps followed those outlined above.

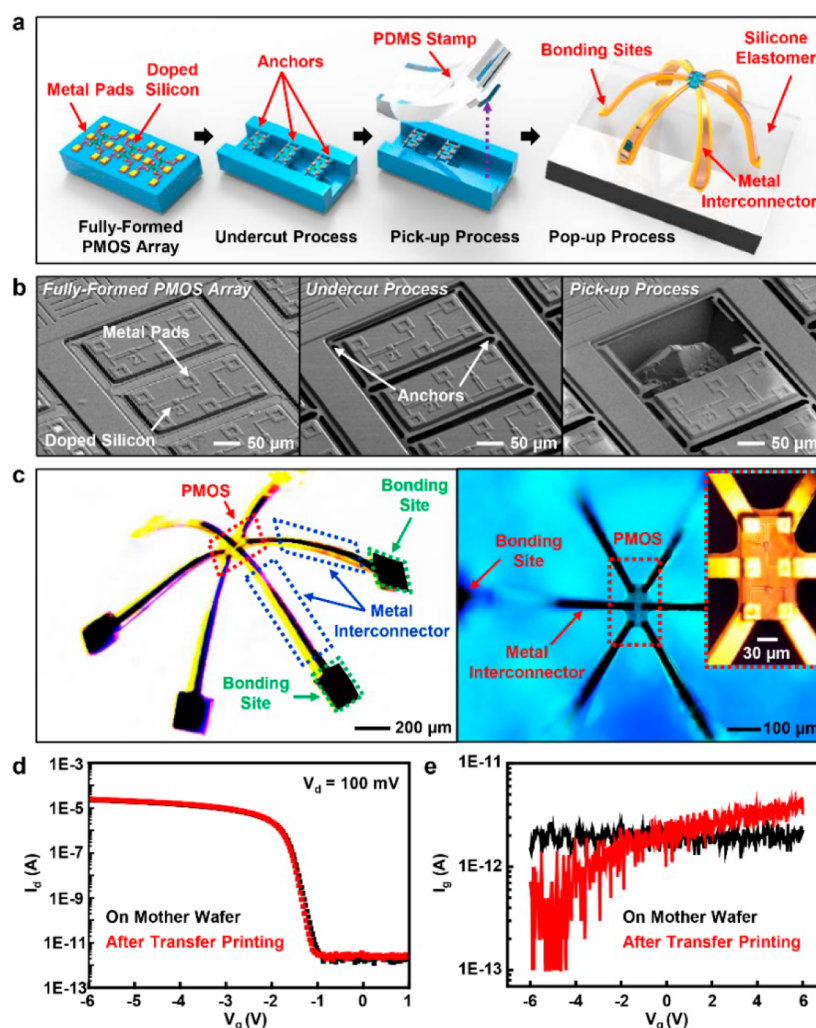


Figure 5. 3D mesostructures populated with a silicon pMOS transistor derived from a commercial foundry process. (a) Schematic illustration of the process for retrieving a silicon pMOS transistor from a foundry SOI platform and integrating it into a 3D structure. (b) Scanning electron microscope images of devices after delineation and trench etching (left), undercut etching (middle), and retrieval (right). (c) Tilted and top-view optical microscope images of 3D structure with an integrated silicon pMOS transistor. The metal interconnectors within the device are connected to the bonding sites of the 3D structure. (d) Transfer curves and (e) gate leakage of a representative device on the original (mother) wafer and after transfer printing silicon pMOS transistors placed on mother wafer and that of silicon pMOS transistors after transfer printing on thin polyimide film.

Foundry-Based Silicon pMOS Transistors in 3D Frameworks.

Foundry-processed 6 in. SOI (100) wafers with active layers of Si (~250 nm), gate oxides (~25 nm), interlayer dielectrics (~750 nm), intermetal dielectrics (~650 nm), Ti/TiN (~100 nm), and W interconnects (~300 nm) served as the source of silicon transistors. Photolithography and ICP-RIE (STS Mesc Multiplex) with SF₆ yielded isolated devices and formed trenches into the underlying Si (100) handle wafer through the intermetal dielectric, interlayer dielectric, and buried oxide. A 600 nm thick, low-stress SiN_x layer deposited by PECVD (STS Mesc Multiplex tool; mixed frequency RF power of 20 W) served as the anchor and etching barrier. Additional ICP-RIE defined the former to tether the devices to their lithographically defined locations and to prevent them from washing away during the undercut etching process. This undercut involved complete immersion in a solution of 8.3% TMAH (at 85 °C) or 18% KOH (at 70 °C). Devices released in this way exist in freely suspended configurations, suitable for transfer printing from the source wafer onto a target substrate.

Finite Element Analyses. Three-dimensional (3D) finite element analyses (FEA) were used to study the buckling process of 3D silicon electronic devices *via* the commercial software ABAQUS, where the compressive forces associated with relaxation of the prestrain in a supporting elastomer substrate exert on the two-dimensional precursor

at bonding regions. Eight-node 3D solid elements were used for the Ecoflex substrate (2 mm thickness), and four-node shell elements were used for thin layers of SiO₂ (30 nm thickness), Ti (3 nm thickness), polyimide (2 μm), Si (200 nm), Cr (5 nm), and Au (200 nm thickness). The elastic modulus and Poisson's ratio for materials used in the simulations were 0.06 MPa and 0.49 for Ecoflex; 75 GPa and 0.17 for SiO₂; 110 GPa and 0.32 for Ti; 2.5 GPa and 0.34 for polyimide; 130 GPa and 0.27 for Si; 279 GPa and 0.21 for Cr; and 78 GPa and 0.44 for Au.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nano.8b00180.

Supporting figures S1–S3 (PDF)

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Notes

The authors declare no competing financial interest.

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