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Thin, Transferred Layers of Silicon Dioxide and Silicon Nitride as Water and Ion Barriers for Implantable Flexible Electronic Systems

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Thin, physically transferred layers of silicon dioxide (SiO_2) thermally grown on the surfaces of silicon wafers offer excellent properties as long-lived, hermetic biofluid barriers in flexible electronic implants. This paper explores materials and physics aspects of the transport of ions through the SiO_2 and the resultant effects on device performance and reliability. Accelerated soak tests of devices under electrical bias stress relative to a surrounding phosphate buffered saline (PBS) solution at a pH of 7.4 reveal the field dependence of these processes. Similar experimental protocols establish that coatings of SiN_x on the SiO_2 can block the passage of ions. Systematic experimental and theoretical investigations reveal the details associated with transport though this bilayer structure, and they serve as the basis for lifetime projections corresponding to more than a decade of immersion in PBS solution at 37 °C for the case of 100/200 nm of SiO_2/SiN_x. Temperature-dependent simulations offer further understanding of two competing failure mechanisms—dissolution and ion diffusion—on device lifetime. These findings establish a basic physical understanding of effects that are essential to the stable operation of flexible electronics as chronic implants.

1. Introduction

High performance, flexible integrated electronic/optoelectronic systems offer powerful capabilities in a range of important applications, from devices for neuromodulation and bioelectronic medicines, to advanced surgical diagnostic systems to tools for biomedical research. Some of the most sophisticated systems use ultrathin inorganic active materials (e.g., nanomembranes of silicon, and others) as the basis for flexible transistors capable of supporting amplification and multiplexed addressing in flexible sheets for high resolution electrophysiological mapping on the cortical or epicardial surfaces[1–5] and injectable needles for optical stimulation of targeted neural circuits in the brain.[6–9] These platforms can bend and conform as

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minimally invasive interfaces to soft, dynamic biological systems, while offering many of the performance characteristics associated with rigid, planar integrated circuits, and optoelectronic components built on semiconductor wafers.[10–20] A critical challenge in realizing chronically implantable bioelectronic systems of this type is in the development of broadly useful material coatings that can serve as robust, long-lived barriers to surrounding biofluids.

The ideal coating would offer low flexural rigidity in thin film form, and compatibility not only with the surrounding biology but also with a range of materials in the underlying electronics. The essential requirement is for negligible permeability (arising from combined effects of intrinsic as well as extrinsic, i.e., pinholes, grain boundaries, defects, etc., properties) to water and to ions and other species in biofluids, with lifetimes measured in decades. Conventional encapsulation strategies, such as bulk metal/ceramic enclosures, thin-film polymers, and organic/inorganic multilayer stacks (deposited in research oriented cleanroom facilities), fail to meet these requirements.[21–27]

Recent research establishes that thin, transferred layers of SiO_2 thermally grown on silicon wafers offer exceptional characteristics in this context.[28] The extremely low water permeability intrinsic to SiO_2, taken together with the high levels of perfection that are possible in thermally grown material on silicon wafers, allows layers of SiO_2 with thicknesses of only a few hundred nanometers to support, over areas measured in square centimeters, device lifetimes of many decades, as extrapolated from temperature-dependent studies of immersion in phosphate buffered saline (PBS) solution. Alternatives based on conventional coatings deposited or grown in the typical fashion in standard, academic laboratory conditions, offer lifetimes that are many orders of magnitude shorter than those of transferred, thermal SiO_2. Nevertheless, despite the superior barrier properties, the possibility of ion penetration through thermal SiO_2 while immersed in biofluids is of concern due to the potential of such species to shift and/or degrade the switching properties of the underlying transistors when in proximity to the channel regions. Furthermore, the competing effects of hydrolysis of SiO_2 and ion diffusion in biofluids demand attention.

The results presented here address these and other key issues. The studies exploit test platforms that consist of thermally grown SiO_2 on silicon-on-insulator (SOI) wafers as barriers in flexible silicon devices. Specifically, various voltages (AC, DC) applied between biofluids and n-channel metal–oxide–semiconductors (NMOS) transistors reveal essential aspects of ion transport through measurements of electrostatically induced shifts in the properties of the transistors. Temperature-dependent drift-diffusion modeling establishes the coupling of dissolution and ion diffusion and their effects on device lifetime. Additional results demonstrate that layers of SiN_x formed by low pressure chemical vapor deposition (LPCVD) can serve as highly effective ion barriers, which in combination with thermal SiO_2, yield bilayers (i.e., SiO_2/SiN_x) that are simultaneously impermeable to water and ions. A combination of electrical tests, temperature-dependent measurements and related simulations indicate that this bilayer structure provides superior capabilities of relevance to use in flexible electronic implants, independent of bias conditions.

2. Results and Discussion

The fabrication process utilizes thermally grown layers of SiO_2 transferred onto flexible electronic platforms (**Figure 1**a). Unlike conventional processing sequences, in which deposition of the encapsulation material occurs last, the scheme here (Figure 1a) starts with a fully formed barrier layer in which device fabrication occurs in a layer-by-layer fashion on top. Briefly, the process begins with formation of isolated silicon transistors on an SOI wafer (≈100-nm-thick device Si and 1-µm-thick buried thermal SiO_2). Solid source doping with phosphorus forms source and drain contacts at concentrations of $\approx 10^{19}$ cm^{-3}. Thermal oxidation and atomic layer deposition at ≈1150 and 80 °C, respectively, yield a dielectric stack of thermal SiO_2 (30 nm)/Al_2O_3 (13 nm). Photolithographically patterned metallization (Cr/Au, 10/300 nm) defines source, drain, and gate electrodes. A transfer process bonds the front side of this substrate to a thin polymer film (Kapton, DuPont, 13 µm) laminated onto a glass substrate coated with a layer of dimethylsiloxane (PDMS; 10 µm) as a temporary support. This process begins with spin casting and curing a coating of polyimide (PI-2545, HD MicroSystems; 3.5 µm) uniformly across the transistors, followed by deposition of a thin layer of Al_2O_3 (20 nm). A commercial adhesive (Kwik-Sil, World Precision Instruments) enhances the adhesion between the Al_2O_3 and the PDMS (coated with Ti (5 nm)/SiO_2 (50 nm)) on the temporary support. After bonding, inductively coupled plasma reactive ion etching (Surface Technology System) with a gas flow of SF_6/O_2 40/3 sccm at a pressure of 50 mT removes the silicon wafer. This step leaves the buried thermal SiO_2 of the SOI wafer as a biofluid barrier.

Peeling the material stack from the temporary substrate yields a piece of flexible electronics encapsulated by a layer of thermal SiO_2 that has low rigidity and good bendability by virtue of its small thickness. Figure 1b shows a schematic illustration of the multilayer configuration as an exploded view. Recent work demonstrates that SiO_2 formed and manipulated in a similar fashion can serve as a flexible/bendable dielectric/encapsulation for high resolution, actively multiplexed electrophysiological mapping systems for use on the surfaces of the heart.[29] These results provide strong evidence for broad applications in advanced bioimplants. Figure 1c,d displays an optical image and a colorized scanning electron microscope (SEM) image of such a piece of flexible electronics with a set of NMOS transistors (channel width W = 300 µm, length L = 20 µm). Figure 1e presents transfer characteristics of a representative transistor (in Figure 1d) in both linear and semi-log scale at a supply voltage V_{DS} = 0.1 V. The on and off currents are 0.2 mA and 1 pA, respectively. The inset shows that the leakage current between the gate and source electrodes (I_{GS}) is below 10 pA. The transistor exhibits a peak effective electron mobility of ≈400 cm^2 V^{-1} s^{-1}, which is consistent with transistors fabricated by the traditional process.[30]

Previous research demonstrates that the water permeability through thermal SiO_2 is extremely small and that a slow hydrolysis process is the cause of eventual failure.[28] In addition to water, ions in biofluids (mostly small, positive species such as Na^+ and K^+) can adversely affect the performance of the transistors, mainly by electrostatically shifting their threshold

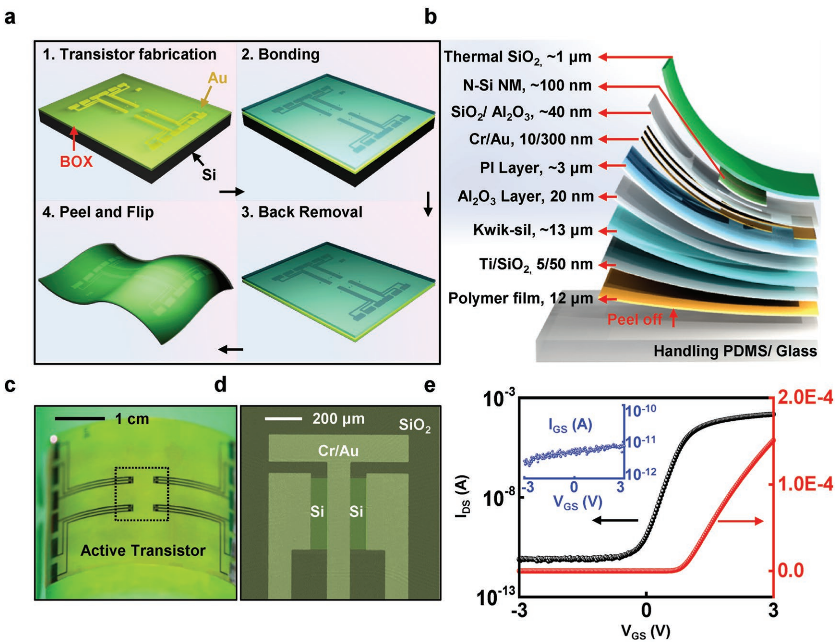

Figure 1. Thin layers of SiO_2 thermally grown on device-grade silicon wafers, deployed as barrier layers in flexible electronic implants. a) Scheme for fabricating test structures that include silicon transistors: (1) Fabrication of transistors on an SOI wafer. (2) Bonding of this wafer, face down, onto to a glass substrate that is coated with a thin film of polyimide (Kapton, 12 µm). (3) Removal of the silicon handle wafer by dry etching. (4) Release of the final flexible test structure from the substrate. b) Schematic illustration of the material stack layout and various thickness of the different layers at the location of an NMOS transistor. c) Optical image of a sample produced in this manner with a 1-µm-thick layer of thermal SiO_2 on its top surface. d) Colorized SEM images of a transistor structure before bonding. e) Transfer characteristics in both linear and semi-log scale, at a supply voltage V_{DS} = 0.1 V. The inset shows the gate leakage current.

voltage (V_T).[31] Results of accelerated soak tests of NMOS transistors during application of an external bias in an accelerated immersion test (in PBS solution at 96 °C and pH of 7.4) are in **Figure 2**a–f. Here, the accelerated ion involves immersion tests refer to those performed at elevated temperatures to increase the rate of the hydrolysis reaction. A bias (V_{app}) exists between a platinum probe in the PBS solution and the transistor electrodes (source, drain, and gate), as illustrated in the insets. Figure 2a–c presents transfer characteristics measured with V_{app} at AC, negative DC and 0 V conditions. All transistors in such cases exhibit a fixed V_T until sudden failure due to hydrolysis of the SiO_2 (corresponding to a dissolution rate of ≈80 nm d^{-1} in 96 °C, consistent with previous reports in ref. [28]), $Si + 4H_2O \rightarrow Si(OH)_4 + H_2$. At 0 V, V_T remains nearly constant, consistent with the lack of an electrical field to drive preferential flow of ions through the SiO_2. Here results at 0 V also match with reported results.[28] For an AC bias consisting of a square wave with amplitude of 3 V and frequency of 100 Hz, the period is much shorter than the time for ions to transport through the SiO_2 layer. This condition therefore has little effect on net ionic flow, such that again V_T remains constant. The negative DC condition corresponds to a constant potential of −3 V. In this case, positive ions such as Na^+ are repelled from the transistor structure, thereby preventing their diffusion through the SiO_2. As expected, thermal SiO_2 provides an outstanding barrier from negative ions such as Cl^-, due to their large size. Here as well, V_T remains constant. These results therefore demonstrate that thermal SiO_2 can perform as an outstanding ion barrier under certain bias conditions, i.e., AC, zero, or DC at negative voltages.

Nevertheless, for positive biases, V_T exhibits time-dependent shifts. Figure 2d–f displays accelerated test data, similar to that in Figure 2a–c, but with various V_{app} from 1.5 to 4.5 V at increments of 1.5 V. For present purposes, device failure is defined as the point when the SiO_2 disappears due to hydrolysis or at which the shift in the threshold voltage ΔV_T for a 1 µm equivalent oxide thickness (EOT) reaches 1 V (less than 5 d under these accelerated conditions). The insets show the transfer characteristics just before failure by hydrolysis. The positive V_{app} serves as a driving force for positive ion transport through the SiO_2, the result of which shifts V_T through electrostatic interactions with the transistor channel. Specifically, because the thickness of the Si is around 100 nm, the layer of Na^+ near the channel can lead to an accumulation of electrons. These positive ions act as a virtual gate, such that the transistor turns on with a more negative V_G at the front gate, corresponding to a negative shift in V_T for an NMOS device. The magnitude of this ΔV_T increases significantly with V_{app} (for a certain fixed thickness), as shown in Figure 2d–f.

Results of modeling of Na^+ transport processes appear in Figure 2g,h. As the area of the barrier layer (y and z planes) is much larger than its thickness (x direction), our analysis can exploit a 1D model[32] where $x = 0$ and $x = 1$ µm in Figure 2g correspond to the PBS/SiO_2 and SiO_2/Si interfaces, respectively. At the PBS/SiO_2 interface, the Na^+ concentration in PBS solution (137 mmol L^{-1} (8.24×10^{25} m^{-3})) is larger than its solubility limit (33 mmol L^{-1} (2×10^{25} m^{-3})) inside thermal SiO_2.[33] The Na^+ dissolution in thermal SiO_2 is sufficiently fast that it does not limit the total drift-diffusion process. Nevertheless, a retardation occurs at the Si/SiO_2 boundary where Na^+ diffusivity $D_{Na^+,SiO_2} \gg D_{Na^+,Si}$,[34–36] as illustrated in Appendix and Figure S1 (Supporting Information). The concentration of Na^+ ($c_{[Na^+]}$, in unit of # m^{-3}) in the barrier layer follows from the time-dependent solutions of the coupled Poisson's equation and continuity equation

$$\frac{\partial^2 \phi(x.t)}{\partial x^2} = -\frac{q \cdot c_{[Na^+]}}{\varepsilon} \tag{1}$$

$$\frac{\partial c_{[Na^+]}}{\partial t} = -\frac{\partial}{\partial x}\left(\mu_{[Na^+]} c_{[Na^+]} \frac{\partial \phi(x.t)}{\partial x} - D_{[Na^+]} \frac{\partial c_{[Na^+]}}{\partial x} \right) \tag{2}$$

where $\phi(x.t)$ is the electrical potential, ε is the dielectric permittivity. μ_{Na^+} and D_{Na^+} are the mobility and diffusivity of Na^+. Einstein's relation: $\frac{D_{Na^+}}{\mu_{Na^+}} = \frac{kT}{q}$ connects these quantities. A constant boundary condition ($V = V_{app}$ and $V = 0$)

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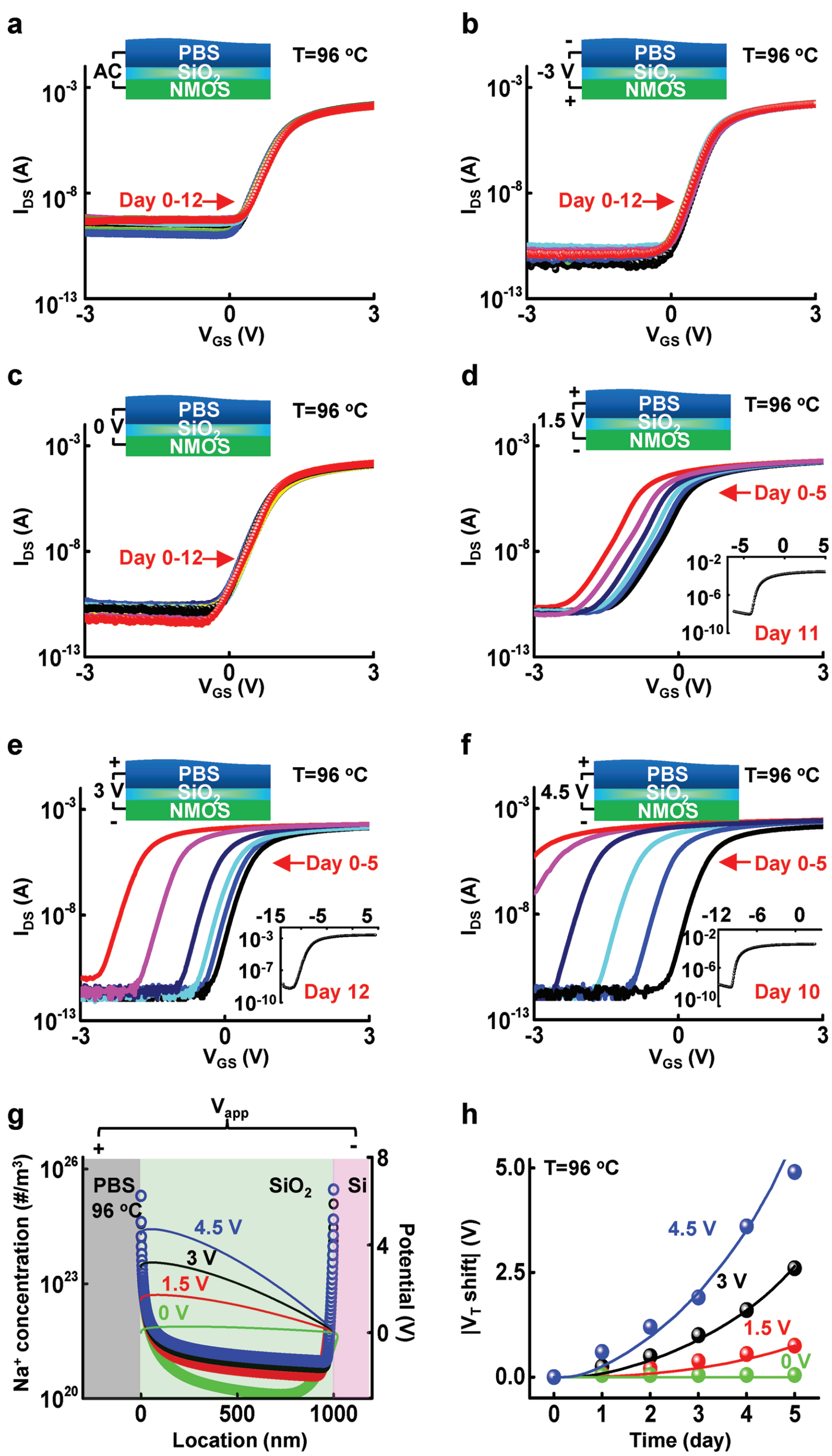

Figure 2. Experimental and simulation results for the behavior of NMOS transistors encapsulated with thermal SiO_2 in various tests of immersion in PBS solution at pH 7.4 and 96 °C. a–f) Results of tests during different electrical bias conditions (AC |3 V|, DC −3 V, DC 0 V, DC +1.5 V, DC +3 V, DC +4.5 V). Schematic illustrations of the samples and bias configurations appear in the upper insets. Lower insets in frames (c)–(f) correspond to I_{DS}–V_{GS} curves collected just before failure. g) Computed Na^+ concentration profiles and potential distributions within a layer of thermal SiO_2 after 10 d of immersion in PBS at T = 96 °C. The applied bias is 0, 1.5, 3, and 4.5 V, respectively. h) Shift in the threshold voltage as a function of time with different bias voltages at T = 96 °C. The solid dots are experimental data and the lines are simulations.

corresponds to the applied bias across the PBS/SiO_2 and SiO_2/Si interfaces, respectively. Figure 2g shows the spatially distributed Na^+ concentration and electrostatic potential profile computed after 10 d for the case of h = 1 µm thermal SiO_2 in 96 °C (without considering hydrolysis). Consistent with the experimental result shown in Figure 2h, V_{app} varies from 0 to 4.5 V with increments of 1.5 V. The Na^+ concentration decreases significantly near x = 0 and Na^+ accumulates at the other side, namely at x = 1 µm. The voltage drops primarily across the oxide layer because the resistance of the SiO_2 is much larger than the PBS solution and the 200 nm Si layer below. The potential barriers due to the charge accumulation near the PBS/SiO_2 and SiO_2/Si interfaces delay the Na^+ transport process.

Figure 2h shows the shift in V_T within 5 d for different bias voltages at T = 96 °C. The drift-diffusion process accelerates with increasing V_{app}, leading to an accelerated V_T shift, which is closely related to the layer of surface charge density Q_s of Na^+ located at the thermal SiO_2/substrate Si interface. We calculate Q_s (in unit of C m^{-2}) from the spatially distributed Na^+ density shown in Figure 2g by integrating Na^+ concentration over the thickness of the accumulated Na^+ layer Δh

$$Q_S = q\int_{h-\Delta h}^{h} \rho_a(x,t)\,\mathrm{d}x \tag{3}$$

where q is the elementary charge and ρ_a is the Na^+ bulk density (in unit of m^{-3}), which can be obtained with recalibrated Na^+ diffusion coefficient. t is the time and h is the thickness of the thermal SiO_2 layer. Similar to the inversion charge density calculation in the metal–oxide–semiconductor field-effect transistor (MOSFET), this Δh can be expressed as[37]

$$\Delta h = \frac{kT/q}{V_{app}} \cdot h \tag{4}$$

Next, to account for the hydrolysis of the SiO_2 layer, we shrink the thickness h in our Na^+ transport numerical simulation as a time-dependent variable

$$h(t) = h_0 - r_{dis} \cdot t \tag{5}$$

where h_0 is the initial thermal SiO_2 thickness (1 µm in this particular case), r_{dis} is the SiO_2 dissolution rate (≈80 nm d^{-1} at 96 °C from soaking experiment). To find the relationship between Q_S and ΔV_T, we numerically simulate a 2D NMOS transistor with commercial software (Sentaurus Technology Computer Aided Design; Appendix and Figure S1, Supporting Information) using experimentally determined device parameters. Figure 2h shows that the numerical result predicted by this model (solid lines) fits well with experimental data extracted from Figure 2c–f (solid dots) with V_{app} from 0 to 4.5 V. Specifically, ΔV_T increases with time and by larger amounts as the bias increases.

The addition of a layer of silicon nitride, whose ion diffusivity is much lower than that of SiO_2, can further suppress ion diffusion. **Figure 3**a displays an exploded-view schematic illustration of a system similar to the one in Figure 1, but with an additional coating of LPCVD SiN_x to form a bilayer encapsulation. Thicknesses are indicated. Formation of the SiN_x (200 nm thick, <250 MPa tensile stress, Rogue Valley Microdevices) relies on high temperature (≈1100 K) growth on a layer of thermal SiO_2 (200 nm thickness) on a silicon wafer (500 µm thick, 100 mm diameter; university wafer). The fabrication scheme begins with transfer printing[38] of Si nanomembranes (NMs; derived from the top silicon layer of SOI wafers) onto the SiN_x surface coated with a layer of polyimide as an adhesive (diluted PI 2545, thickness <300 nm, which is water-permeable material). Subsequent fabrication steps follow those described previously for the case of single-layer SiO_2 encapsulation.

Despite its low ion diffusivity, SiN_x has limitations as a standalone encapsulation layer. First, its dissolution rate is much higher than that of thermal SiO_2. Figure 3b indicates that LPCVD SiN_x dissolves at a rate of ≈0.3 nm d^{-1} at 37 °C and a pH of 7.4. This value is approximately ten times higher than that of thermal SiO_2 (≈4 × 10^{-2} nm d^{-1}) under similar conditions.[28] Silicon nitride hydrolyzes in two steps:[39] (1) oxidation into silicon oxide and (2) hydrolysis of silicon oxide, where the overall reaction is $Si_3N_4 + 12H_2O \rightarrow 3Si(OH)_4 + 4NH_3$. Temperature-dependent studies of hydrolysis of LPCVD SiN_x in PBS reveal additional insights (Figure 3b). These experiments involve pieces of SiO_2/Si wafers (100 nm thick SiO_2, 1 cm × 2 cm dies) with 200 nm thick LPCVD SiN_x layers on top. PDMS wells bonded to the SiN_x confine the PBS solution to targeted regions of these wafers, as shown in the inset of Figure 3b. Ellipsometry defines the thicknesses as a function of immersion time at room temperature (RT), 37, 50, 70, and 96 °C, respectively. As expected, the thickness of LPCVD SiN_x decreases linearly with time, to determine the dissolution rate. The rate at a pH of 7.4 and 37 °C is ≈0.3 nm d^{-1}, consistent with previous reports.[37] The relationship between dissolution rate and temperature (Figure 3c) is consistent with Arrhenius scaling and an activation energy of E_A = 0.97 eV. This value is lower than that of thermal SiO_2 (1.32 eV).[28]

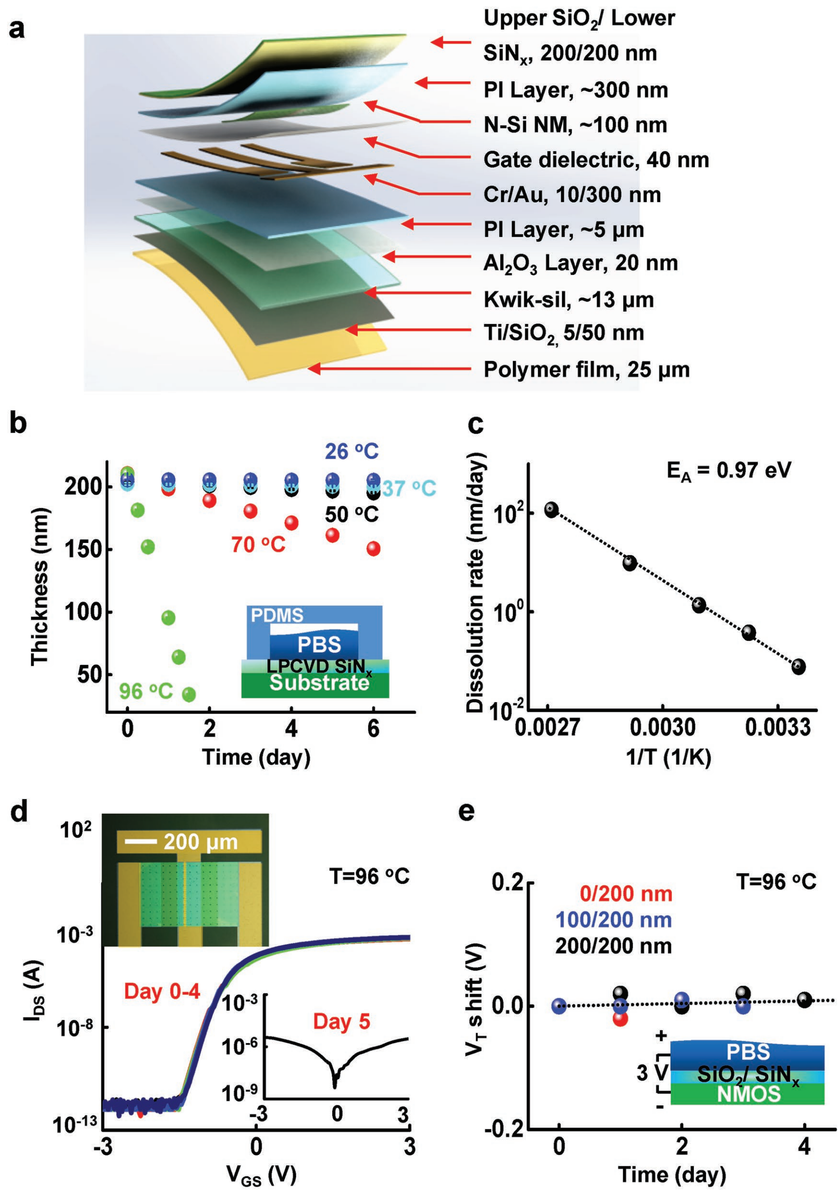

Figure 3. Properties of encapsulation layers that include LPCVD SiN_x. a) Schematic illustration of a material stack that uses a bilayer of thermal SiO_2/LPCVD SiN_x as an ion and water barrier for underlying silicon transistors. b) Thickness of a layer of LPCVD SiN_x as a function of time of immersion in PBS at pH 7.4 and at various temperatures. The inset shows the geometry of the test structure. c) Data that indicate a linear relationship between dissolution rate and $1/T$. d) Electrical characteristics of NMOS transistors encapsulated by SiO_2/SiN_x (200/200 nm) in PBS soak tests at 96 °C and an applied bias, V_{app} = 3 V. The upper inset shows an optical image of a typical device. The bottom inset shows transfer characteristics collected at the failure time of 5 d. e) Threshold voltage shift as a function of time with V_{app} = 3 V bias at T = 96 °C, for three different bilayer thicknesses of SiO_2/SiN_x indicated in the legend. The solid dots are experimental data and the dotted line is a simulation. The bottom inset provides a schematic illustration.

Another additional limitation of LPCVD SiN_x as a single-layer encapsulation is the tendency to form pinholes and defects during deposition in typical cleanrooms available to academic labs. Experiments that involve magnesium test structures (Mg, 300 nm thick, ≈1 cm^2 area) in Appendix and Figure S2 (Supporting Information), indicate that the spatial density of visible pinholes in 200 nm thick layers of LPCVD SiN_x is 1–2 per square centimeter for our materials. Although improved deposition conditions offer the potential to reduce this value significantly, most academic cleanrooms do not afford the necessary levels of control.

These considerations motivate the use of a bilayer encapsulation that combines both thermal SiO_2 (contacted with PBS) and LPCVD SiN_x (substrate for transistor). Here, the SiO_2 layer serves as a pinhole-free water barrier with slow dissolution rates and SiN_x serves as a barrier to ions. The inset of Figure 3d displays an optical image of a transistor (channel width W = 300 µm, length L = 20 µm) that incorporates a front-side encapsulation bilayer of SiO_2/SiN_x fabricated using the process described previously. Even with V_{app} of 3 V (same as upper inset of Figure 2e), the key performance characteristics of these transistors remain constant in accelerated soak tests (in 96 °C PBS solution) over the full duration of the experiments, Day 0–4 (Figure 3d). The devices catastrophically fail at Day 5 (lower inset of Figure 3d) as a result of hydrolysis of the SiO_2 and then the SiN_x. The projected lifetime is 16 years at 37 °C considering their dissolution rates (PBS, pH 7.4).[28,39] The bilayer also partially balances the opposite stress inside each film (thermal SiO_2, compressive stress and LPCVD SiN_x, tensile stress). This stress balancing can avoid the cracking in the SiN_x film and mitigate the curving of the final flexible device.

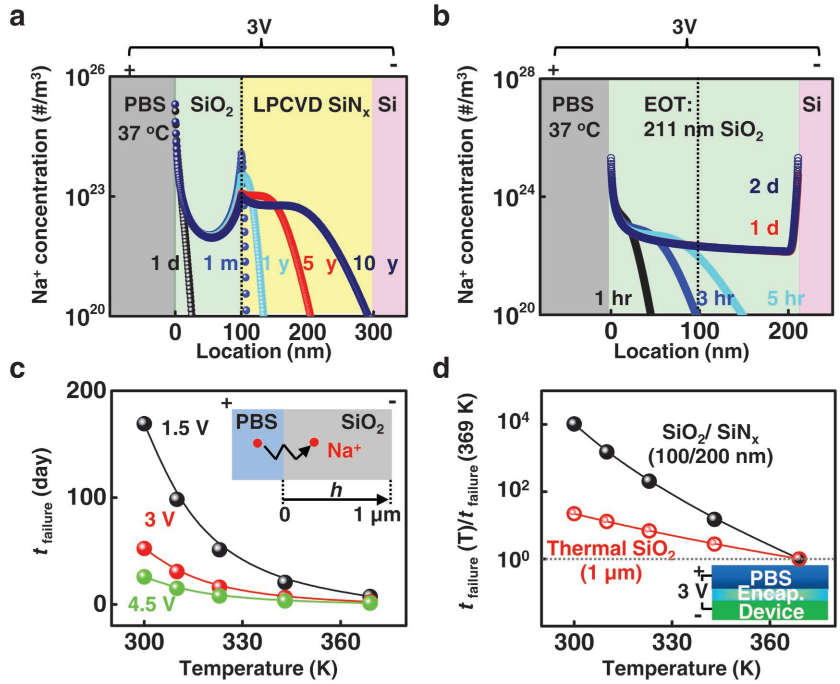

Figure 4. Simulations of ion diffusion through and dissolution of two encapsulation structures. a) Na^+ concentration profiles through a bilayer of h_1 = 100 nm thermal SiO_2 and h_2 = 200 nm LPCVD SiN_x at the end of 1 d, 30 d, 1 year, 5 years, and 10 years at T = 37 °C. b) Simulations of ion diffusion for an equivalent oxide thickness of SiO_2 that corresponds to SiO_2/SiN_x (100/200 nm). Na^+ concentration within h = 211 nm thermal SiO_2 layer at the end of 1 h, 3 h, 5 h, 1 d, and 2 d at T = 37 °C. c) Simulated failure times for an encapsulation of thermal SiO_2 associated with ion diffusion at V_{app} 1.5, 3, and 4.5 V. The inset provides a schematic illustration of the geometry. d) Accelerated factors for both ion diffusion and dissolution as a function of temperature in SiO_2 and SiO_2/SiN_x at thicknesses of 1 µm and 100/200 nm, respectively. The inset provides a schematic illustration of the geometry.

Accelerated soak tests under this same bias condition (3 V) with samples that have different thicknesses of SiO_2 (0, 100, and 200 nm) and a fixed thickness of SiN_x (200 nm) confirm these mechanisms (see Figure 3d and Appendix and Figure S3, Supporting Information), whereby hydrolysis of the top thermal SiO_2 occurs first followed by the bottom SiN_x. Values of ΔV_T extracted from data in Figure 3d and Appendix and Figure S3 (Supporting Information) appear in Figure 3e. The differences in lifetime are consistent with the dissolution rate of thermal SiO_2 in 96 °C PBS (≈80 nm d^{-1}). In all cases, the shifts in V_T are extraordinarily small (less than ≈0.05 V). These findings are consistent with simulations of a single layer of SiN_x (200 nm thickness) with 3 V bias (black line in Figure 3e).

Modeling of the distributions of Na^+ allows further comparisons of SiO_2/SiN_x and SiO_2 (**Figure 4**a,b). As before, the coupled drift-diffusion equation and Poisson's equation are solved in a 1D domain with V_{app} = 3 V. As shown in Figure 4a, the green and yellow regions correspond to SiO_2 (100 nm thickness) and SiN_x (200 nm thickness). The values of diffusion coefficients are 6.53×10^{-21} m^2 s^{-1} in thermal SiO_2[33] and 4.94×10^{-25} m^2 s^{-1} in LPCVD SiN_x at 37 °C.[40] Due to four orders of magnitude differences in diffusivity, Na^+ penetrates the top SiO_2 layer much faster than the underlying LPCVD SiN_x layer. Figure 4A shows that within the first month, Na^+ builds up inside the SiO_2 layer and reaches a short-term saturated concentration profile. At the SiO_2/SiN_x interface, Na^+ accumulates because the Na^+ influx from the SiO_2 side is much larger than the outflux into SiN_x side. After this saturation time interval inside SiO_2, Na^+ begins to slowly transfer into the SiN_x layer. From 1 year up to 10 years, the front end of Na^+ concentration spreads out toward the SiN_x/Si interface with increasing x (location axis, from 100–300 nm in Figure 4a). During this period, the accumulated Na^+ peak at the SiO_2/SiN_x interface gradually decreases to balance the Na^+ that flows into the SiN_x layer. Few Na^+ (less than 10^{20} m^{-3}) ions can penetrate through SiN_x/Si interface within 10 years.

The Na^+ concentration profile for a corresponding EOT of single layer of thermal SiO_2 reveals details (Figure 4b). Here, $\mathrm{EOT} = t_{\mathrm{high}-k} \times \left(\frac{k_{\mathrm{SiO_2}}}{k_{\mathrm{high}-k}}\right)$, where t is the thickness and k is the dielectric coefficient (3.9 for SiO_2[41] and ≈7 for SiN_x[31]), which indicates the thickness of a layer of SiO_2 that produces the same electrical field effect as the SiN_x. Specifically, an SiO_2 layer with thickness of ≈111 nm offers a capacitance similar to that of a layer of LPCVD SiN_x with 200 nm thickness. As a result, 100/200 nm SiO_2/SiN_x corresponds to a total 211 nm thick EOT of SiO_2. To make a reasonable comparison, the same boundary conditions and external voltages (3 V) are the same in these two cases, at 37 °C. Figure 4b presents Na^+ concentration profiles. The accumulated Na^+ at SiO_2/Si interface reaches its saturation limit in less than 2 d. The Na^+ does not significantly penetrate into the LPCVD SiN_x layer over a period of 10 years.

A simulation model based on a 1D domain of a 1 µm thick layer of SiO_2 (inset of Figure 4c) using COMSOL Multiphysics reveals the concentration distributions at different V_{app} (1.5, 3, and 4.5 V, same in upper insets of Figure 2d–f), with effects of temperature explicitly included. Here, Na^+ transports occur with a constant boundary condition at $h = 0$ and reflective boundary condition at $h = 1$ µm, corresponding to the PBS/SiO_2 and SiO_2/Si interfaces, and h is the thickness of thermal SiO_2. The Na^+ penetration rate depends on both applied electrical field and temperature. A failure threshold corresponds to the time at which the Na^+ concentration at the SiO_2/Si interface reaches 1/40 of its solubility limit:5×10^{23} m^{-3}. The temperature-dependent Na^+ diffusion coefficient is: $D = D_0 \cdot e^{-E_A/kT}$, where k is the Boltzmann constant and T is temperature. D_0 is the pre-exponential factor and E_A is the activation energy. The diffusion coefficient can be extracted from the data of Figure 2h, where D_0 and E_A are 2.29×10^{-13} m^2 s^{-1} and 0.464 eV, respectively. The calculations yield failure times in various temperature ranges (from 300 to 369 K, corresponding from RT to 96 °C) and at various V_{app}. In Figure 4c, together with the consideration of hydrolysis failure, failure time of 1 µm thick layer of SiO_2 depends exponentially on temperature, and the results at each temperature show a strong dependence on respective V_{app}. Specifically, the lifetime at RT under 1.5 V is ≈11 times longer than that of 4.5 V, while the difference at 96 °C is approximately ten times, which indicates that the lifetime differences respective to various V_{app} are about same at different temperatures.

Modeling can also capture the competition between dissolution and ion diffusion in SiO_2 and SiO_2/SiN_x. Figure 4d presents such competition for single layer of thermal SiO_2 and a bilayer of thermal SiO_2/LPCVD SiN_x at thicknesses of 1 µm and 100/200 nm, respectively. The inset of Figure 4d displays the configuration. We consider an acceleration factor (AF) for the failure time as a function of temperature, considering both dissolution and ion diffusion failures together. The AF is defined as $t_{failure}(T)/t_{failure}$ (369 K), normalized at 369 K. In the case of 1 µm thick SiO_2, the AF depends on data extracted from Figure 4c. Here, ion penetration dominates the failure time ratio because the corresponding dissolution failure time is much longer than ion-diffusion failure time. On the other hand, although SiO_2/SiN_x offers improved water/ion barrier properties than single thermal SiO_2, the SiN_x has higher dissolution rate than SiO_2. As a result, dissolution plays an important role. The AF of SiO_2/SiN_x (100/200 nm) uses the dissolution failure time from Figure 3e. The SiO_2 layer dissolves first, followed by the SiN_x. As a result, a bilayer of SiO_2/SiN_x offers a lifetime that is approximately three orders of magnitude larger than that of a single layer of SiO_2 at 1 µm thickness at 37 °C, due to the enhanced ion barrier properties. The bilayer therefore provides greatly superior performance, even at thicknesses significantly smaller than a corresponding single layer of SiO_2.

3. Conclusion

In summary, the results presented here represent a comprehensive study of ion transport and hydrolysis in ultrathin layers of thermal SiO_2 and LPCVD SiN_x in the context of encapsulation strategies for flexible electronic implants. A combination of experiments and simulations demonstrates that bias conditions strongly affect the rate of ion penetration through SiO_2, with implications for operational stability of encapsulated transistors. The addition of a layer of LPCVD SiN_x layer can effectively block transport of ions in ways supported by detailed studies of temperature and thickness-dependent transistor performance. In these systems, two different failure mechanisms must be considered. For a single layer of thermal SiO_2, ion diffusion is dominant due to the low dissolution rate of this material and the comparatively high ion diffusivity. For a bilayer of SiO_2/SiN_x, dissolution dominates due to excellent ion barrier properties of SiN_x. We note that in many practical cases, the SiN_x can be applied selectively to regions of the system that support transistors or other active semiconductor devices. Implementing this ion barrier structure in active flexible electronics and optoelectronics will create new possibilities for cardiac and neural and other forms of implants.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

flexible electronics, silicon dioxide, silicon nitride, thin film encapsulation, water/ion barrier

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