# Stability of MOSFET-Based Electronic Components in Wearable and Implantable Systems

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***Abstract*— Wearable and implantable electronic (WIE) devices are enabling a new generation of customized real-time health monitoring systems. Some of the highest performance systems involve MOSFET-based sensors as well as MOSFET-based digital and analog circuits. Protecting these transistors in a harsh fluidic environment is difficult because the requirement of wearability/flexibility demands ultrathin encapsulation. The charged ions (such as $Na^+$) from body-fluids can diffuse rapidly through the thin encapsulation layer and destabilize the transistors, and render the component nonfunctional. In this paper, we develop an analytical framework and scaling theory for $Na^+$ penetration into the encapsulation layer of WIE devices. Coupled with the physics of MOSFET degradation, the ion penetration model predicts lifetime of MOSFET-based electronics encapsulated by various types of encapsulating materials. The model is easily generalized to include multiple design parameters, such as stacks of encapsulation layers, encapsulation layer thicknesses, temperature/field dependent ion drift, and rate of dissolution of the encapsulation layer. Our simulations and experiments show that: 1) a multilayer encapsulation is essential to achieve multiobjective passivation, and 2) the encapsulation thickness must be optimized by accounting for charged ion penetration and dissolution of the encapsulation layer.**

***Index Terms*— Implantable, MOSFETs, reliability, wearable.**

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## I. Introduction

WEARABLE and implantable electronic (WIE) devices, such as a digital wristband, smart watch, and implantable cardioverter defibrillator have found widespread usage in healthcare and fitness applications [1]. The next generation wearable electronic devices (ultrathin film electronics [2], [3], for instance) must be lightweight and have smaller form factor. Numerous groups have experimentally demonstrated functional prototypes. For example, Kim *et al.* [4] have introduced "skin-like" membrane-based approach that integrates electrodes, electronics, sensors, power supply, and communication components. Kaltenbrunner *et al.* [5] fabricated ultrathin active-matrix array with resistive tactile sensors. Gao *et al.* [6] have developed wearable sensor array platform for multiplexed *in situ* perspiration analysis. Lee *et al.* [7] have introduced a "patch-like" electrochemical device for diabetes monitoring and therapy.

Long-term electromechanical stability and reliability are critical challenges for the next generation WIE systems. Comparing to the electronic components in traditional devices such as mobile phone, the electronic components in WIE systems need to operate in an electrochemical fluid, such as sweat, saliva, and blood [8], [9]. Temperature, pH, moisture, ion concentration, etc., in the electrochemical fluid offer a non-traditional operating environment for traditional electronics, hence reliability issues of those electronic components must be considered carefully. For some devices such as bioimplantable sensors in cardiology applications, the electronic system should have a long-term stability. For other applications such as transient electronics for brain monitoring, a precise predictable degradation lifetime is of great interest [10]–[12]. Due to the small physical dimension, lightweight, mechanical flexibility [13], and other requirements, proper design of packaging encapsulant without compromising electronic functionalities becomes an important design challenge for these electronic components.

Among various degradation mechanisms, charged ions penetrating into the encapsulation layer of wearable electronic devices directly disturb the electric field and lead to functional-failure of the electronic components. The family of MOSFET-based electronic device [14] is one of the most widely used electronic components in WIE system, because they allow highly complex integration of multiple sensing and signal

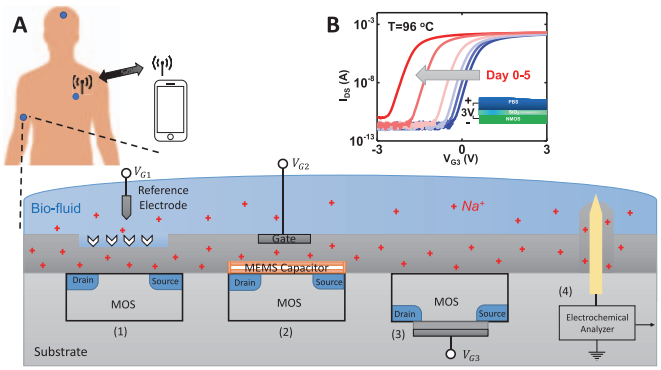


Fig. 1. (A) Schematic illustration of four categories of electronic components in WIE systems. (1) Chemical biosensor. (2) MEMS-based physical biosensor. (3) Implantable MOSFET for signal processing. (4) Amperometric biosensor electrode. (B) Measured $I_{ds}$–$V_{gs}$ curves for signal processing MOSFET from accelerated salt soaking experiments at the end of 0–5 days.

processing functions. Unfortunately, the performance and electrostatic integrity of MOSFETs are very sensitive to charged ions. This paper focuses on the performance degradation of MOSFET-based electronic components, more specifically, the threshold voltage shift $\Delta V_{\text{th}}$, of WIE systems.

The WIE components can be divided into four groups, as shown in Fig. 1.

1) *Chemical biosensors* such as classical Ion-Sensitive Field-Effect Transistor (ISFET) potentiometric sensor [15], [16]. They consist of an ion selective membrane layer on top of an insulated gate FET. The gate insulator plays an important role in protecting the channel of the ISFET from biofluid. Nevertheless, the charged ions penetrating into the gate insulation layer will eventually degrade the ISFET electronic performance.
2) *Micro-Electro-Mechanical Systems (MEMS)-based physical biosensors* [17]–[19] feature a microstructured dielectric gate oxide. The external pressure deforms the MEMS gate oxide, changes the gate capacitance, and modulates the drain current of the underlying MOSFET. Regarding its reliability, the charged ions from the human body can penetrate into the gate oxide layer and destabilize the MOSFET $I_{\text{ds}} - V_G$ response.
3) *Implantable MOSFET for signal processing* [20]. Unlike chemical or MEMS sensors, the signal processing circuitry does not involve sensing the surrounding, and may thus be entirely isolated. However, due to the ultrathin encapsulation in flexible WIE systems, the charged ions may nonetheless penetrate through the back encapsulation layer and shift the threshold voltage of the MOSFET.
4) *Amperometric biosensor electrode* for implantable applications. For these sensors, only the tip of the electrode must be exposed to the desired location, while the rest of the electrode must be isolated from the surrounding environment. As charged ions penetrate the encapsulant, the electrode inactive area could generate large parasitic amperometric signal, and rapidly degrade the signal-to-noise ratio of these sensors.

In this paper, we concentrate on MOSFET-based electronic device degradation mechanisms, cases (1), (2), and (3). To illustrate the importance of the stability/reliability of the devices, we conduct accelerated soaking experiments at 96 °C in standard phosphate-buffered saline solution (PBS), consisting of $Na_2HPO_4$ and NaCl dissolved in water. We apply an external voltage $V_0 = 3$ V across the test structure, with a back-gated nMOS device packaged inside (case 3). Details of the soaking test have been reported in [21] and [22]. Fig. 1(B) shows the measured $I_{\text{ds}} - V_{\text{gs}}$ curves of the nMOS at the end of 0–5 days. There are two key observations: 1) the nMOS threshold voltage becomes more negative over time, consistent with the hypothesis that positively charged $Na^+$ is gradually penetrating the encapsulation layer and distorting the electrostatics of the transistor channel and 2) the absolute value of $\Delta V_{\text{th}}$ increases nonlinearly and accelerates over time.

To explain the experimental observations, this paper is divided into the following sections. In Section II, we offer both a numerical framework and an analytical model for $Na^+$ transport through the encapsulation layer. In Section III, we provide two basic MOSFET degradation models (front-gate and back-gate cases) including the influence from the penetrated $Na^+$. The coupled model can be used to predict the overall device lifetime for arbitrary WIE systems. The measurement data from accelerated reliability experiments confirm our model to be precise and scalale. In Section IV, the model is used to develop design guidelines for encapsulation layers for WIE systems. Finally, we note that the problem of ion penetration is general, thus our model will be useful for the design of broad range of electronic, mechanical, and chemical systems such as eliminating undesiable potential induced degradation in photovoltaic systems [23], contact-pad induced ion drift in high-power electronics [24], and so on.

## II. Model System Part A: Ion Penetration

In this section, we will numerically simulate $Na^+$ penetration process through the encapsulation layer from the PBS solution. From the results of the numerical framework, we will then derive analytical models and scaling principles to describe this physical mechanism and offer design guidelines.

### A. Numerical Framework

The transport of $Na^+$ through the ion barrier layer can be described by the well-known space-charge-limited process [25]. We solve the corresponding transport equations [(1) and (2) below] using COMSOL Multiphysics simulator. Fig. 2(A) shows the schematic illustration of the structure where $x = 0$ and $x = h$ correspond to the PBS/ion barrier and ion barrier/Si interface. We determine the density of $Na^+$ (n) by solving the coupled Poisson's equation and continuity equation

$$\frac{\partial^2 \psi(x,t)}{\partial x^2} = -\frac{q \cdot n}{\kappa \epsilon_0} \tag{1}$$

$$\frac{\partial n}{\partial t} = -\frac{\partial}{\partial x}\left(\mu n \frac{\partial \psi(x,t)}{\partial x} - D\frac{\partial n}{\partial x}\right) \tag{2}$$

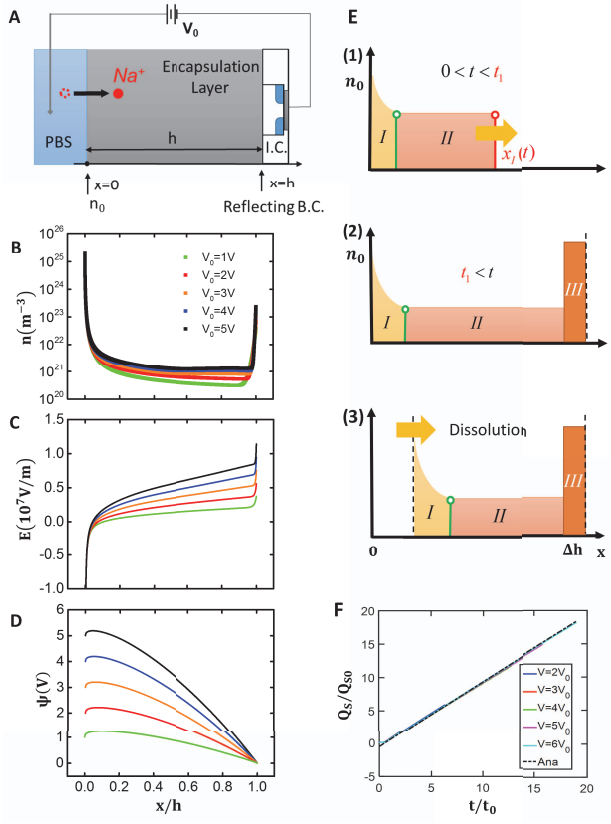


Fig. 2. Numerical framework of space-charge-limited $Na^+$ penetration process. (A) Schematic illustration of sodium ion penetration in 1-D single layer ion barrier domain with external applied voltage $V_0$. (B)–(D) $Na^+$ density, electrical field, and potential distribution within $h = 1000$ nm thermal $SiO_2$ layer at the end of $t = t_0 = ((kT \cdot h^2)/DqV)$ simulation. Potential bias $V_0$ is swept from 1 to 5 V with an increment of 1 V. (E) Schematic illustration of time-dependent $Na^+$ concentration profile. Region I: accumulated $Na^+$ near the PBS/encapsulant interface. Region II: approximate constant low $Na^+$ concentration middle region. Region III: accumulated $Na^+$ region near the encapsulant/Si interface. (F). Normalized surface density of $Na^+$ near the encapsulant/Si interface as a function of normalized time under different external biases.

where $\psi\ (x, t)$ is the electrical potential, $\kappa$ is the relative dielectric permittivity, $\epsilon_0$ is the vacuum permittivity constant, and $\mu$ and $D$ are the mobility and diffusivity of $Na^+$ in the encapsulation layer material (thermal $SiO_2$ for this illustrative example). Einstein's relation: $(D/\mu) = (kT/q)$ connects these quantities. The analysis makes the following assumptions, none of which should have significant effect on the key conclusions.

1) The area of the ion barrier in the $yz$ direction is much larger than its thickness in the $x$-direction. Therefore a simplified 1-D simulation is appropriate.
2) $Na^+$ incorporation in the oxide is fast enough so that it does not limit the total drift-diffusion process. This allows us to define a constant $Na^+$ density $(n_0)$ at the PBS/encapsulant interface. This interfacial concentration equals the solubility limit of $Na^+$ inside the encapsulant (i.e., 33 mmol/$L$($2 \times 10^{25}$ $m^{-3}$) in thermal $SiO_2$) [26].
3) The physics of moisture diffusion is not included and any coupled transport effect is ignored. Therefore, the $Na^+$ diffusion coefficient $D$ is uniform across the encapsulant.
4) $D$ of $Na^+$ inside thermal $SiO_2$ is much smaller than that of crystalline silicon it protects [27]–[29]. Therefore, a reflective boundary condition defines the thermal $SiO_2$/Si interface.
5) The externally applied voltage $V_0$ across the whole structure drops primarily across the encapsulation layer, and the capacitive drop over the ultrathin double-layer screening ions [30] may be ignored.

Fig. 2(B) shows the spatially distributed $Na^+$ density profile at the end of $t = t_0$ where $t_0$ is defined as the drift dominated transport time

$$t_0 = \frac{h}{\mu E} = \frac{kTh^2}{DqV_0} \tag{3}$$

where $h$ is the thickness of the encapsulation layer, $E$ is the electric field, $k$ is the Boltzmann's constant, and $T$ is the temperature. We swept the electrostatic potential $V_0$ from 1 to 5 V with an increment of 1 V. The $Na^+$ density decreases significantly near $x = 0$ and accumulates at $x = h$. According to Poisson's equation (1), the accumulated $Na^+$ near the two boundaries contribute to the significant jump of the electric field, as shown in Fig. 2(C).

Fig. 2(D) shows the potential distribution across the encapsulant. Interestingly, a self-induced potential barrier (with peak value higher than $V_0$) occurs inside the encapsulation layer. The additional accumulated $Na^+$ charges lead to a negative electric field near the interface of PBS solution and the encapsulant layer. From a transient prospective, this potential barrier gradually builds up and slows down the ion transport until $Na^+$ influx from the PBS solution is balanced by the negative interfacial electric field that is trying to push the ions back into the solution. In fact, we can model this internal potential barrier as an ion density dependent virtual voltage source [31]. As $V_0$ increases, the location of this virtual voltage source ($x_0$ where the electrical field reaches zero) consistently moves toward the left boundary. Moreover, the normalized potential barrier $v_r \equiv (V_{\text{peak}} - V_0)/V_0$ decreases with increasing $V_0$.

This virtual voltage source model explains the trend of the $Na^+$ density profiles under different external bias, shown in Fig. 2(B). If the ion drift is the dominate transport mechanism, all the five density profiles should have scaled to a universal curve at $t = t_0$. However, Fig. 2(B) shows that there is an excess $Na^+$ build-up inside the encapsulation layer with increasing $V_0$. The location of the virtual source shifts to the left and the relative magnitude of the virtual voltage source decreases, implying the relative ineffectiveness of the potential barrier in preventing $Na^+$ penetration into the encapsulant.

### *B. Analytical Model and Scaling Principles*

Intrigued by the essential simplicity of the density profiles obtained numerically, in this section we derive the time-dependent density distribution analytically for a single encapsulation layer. We solve the continuity equation and Poisson's equation self-consistently. An exact analytical solution is impossible, but a few simple, numerically validated

assumptions allow insightful approximate solution of this complex space-charge-limited ion transport problem.

Fig. 2(E) (1) shows the schematic illustration of $Na^+$ profile before the critical time $t_1$ at which $Na^+$ front reaches the right boundary. This critical transition time $t_1$ is calculated from [25] as

$$t_1 = 2\left(1 - e^{-\frac{1}{2}}\right) \cdot t_0 = 0.787 t_0. \tag{4}$$

The position of the front end $x_I(t)$ is given by

$$x_I(t) = -2 \ln \left(1 - \frac{1}{2}\frac{t}{t_0}\right) \cdot h. \tag{5}$$

In region II, the total current flux ($J = q\mu nE + \kappa\epsilon_0(\partial E/\partial t)$, the sum of conduction and displacement currents) is independent of position ($x$), so that $(\partial J/\partial x) = 0$. By taking the partial derivatives with respect to $x$ for both conduction current and displacement current, following the carrier flow line: $(dx(t)/dt) = \mu E$ suggested by [25], and canceling and rearranging terms, the density of $Na^+$ (before $t_1$) can be shown to follow a simple relationship:

$$\frac{dn}{dt} = -\frac{\mu q}{\kappa\epsilon_0} \cdot n^2. \tag{6}$$

By integrating both side of (6), $Na^+$ density in region II can be expressed as a time-dependent variable as

$$n_{II}(t) = \frac{n_0}{1 + \frac{\mu q}{\kappa\epsilon_0} n_0 \cdot t}. \tag{7}$$

In region I, however, there's no exact analytical solution for $n_I(t)$. Fortunately, the numerical simulation in Fig. 2(B) shows that the width of region I is negligibly small and the $Na^+$ density drops nearly four order of magnitude within this region. Therefore, the delta-function-shaped contribution of $Na^+$ from this region to the overall MOSFET device performance can be approximated by a constant. We will discuss this point further in Section III-A when we calculate the threshold voltage shift of a transistor.

After the critical transition time $t_1$, $x_I(t)$ reach the encapsulation layer/Si boundary. $Na^+$ ions begin to pile up and form region III, as shown in Fig. 2(E) (2). During this time interval, the $Na^+$ influx gradually reaches a steady-state value as first derived by Mott and Gurney [32]

$$J = \frac{9}{8}\kappa\epsilon_0\mu\frac{V_0^2}{h^3}. \tag{8}$$

Therefore, we can approximate the surface charge density of $Na^+$ in region III from the steady-state flux as

$$Q_s = J \cdot (t - t_1) = \frac{9}{8} q\kappa\epsilon_0\mu\frac{V_0^2}{h^3} \cdot (t - t_1). \tag{9}$$

Fig. 2(F) shows the normalized surface charge density in region III $Q_s/Q_0$ ($Q_0 = (9/8)\kappa\epsilon_0\mu\ (V_0^2/h^3)t_0$) as a function of normalized time $t/t_0$ for both numerical simulation result with different $V_0$ and analytical result from (9). After $t > t_1$, all the numerical results as well as the analytical solutions can be scaled to the same universal curve. This universality verifies the assumptions and approximations in our analytical derivation. Also, $Q_S$ scales linearly with time, as in (9). The upper-limit for (9) is defined by the requirement that $Na^+$ density $n = (Q_s/(q \cdot \Delta h))$ cannot exceed the dissolution limit for the chosen encapsulant material.

The encapsulation layer sometimes dissolves in the harsh salty environment. To account for this effective thinning through hydrolysis of the encapsulation layer, we make the encapsulant thickness $h$ [Fig. 2(E) (3)] a time-dependent variable, namely

$$h(t) = h_0 - r_{dis} \cdot t \tag{10}$$

where $r_{dis}$ is the encapsulation layer dissolution rate (in units of nm/day) measured from the soaking experiments conducted at different temperatures. As we will see in Section III the physical thinning of the encapsulation layer is essential to understand the nonlinear voltage shift reported in the experiments.

Now that we have developed both numerical and analytical models describing time-dependent $Na^+$ density profile, in Section III, we are going to explore the impact of the charged ions on the overall performance of the MOSFET-based devices.

## III. Model System Part B: MOSFET-Based Electronic Component Performance Degradation

In this section, we will establish how $\Delta V_{th}$ of a MOSFET is affected by the amount of charged ion distribution within the encapsulant. We will focus on two types of MOSFET-based components: 1) front-gated MOSFET for biosensor applications (Type 1 and Type 2 devices described in Section I) and 2) back-gate MOSFET for signal processing (Type 3 device in Section I). Eventually, we will use the $\Delta V_{th}$ model to design encapsulant layers for specific WIE systems.

### A. WIE System Containing Front-Gated MOSFET

Similar to the effect of mobile charges in the traditional MOSFET device gate oxide [33], the charged $Na^+$ in the encapsulation layer will shift the effective gate voltage seen by the transistor. The failure threshold $\Delta V_{th}$ can be expressed as a function of spatial distributed $Na^+$ density, as follows:

$$\Delta V_{th}(t) = \frac{q}{C_0}\left[\frac{1}{h}\int_0^h x \cdot n(x,t)dx\right] \tag{11}$$

where $C_0$ is the initial gate capacitance, $h$ is the thickness of the coating layer. The 1-D spatial coordinate is defined as $x = 0$ at the gate/oxide interface shown in Fig. 3(A).

As discussed in Section II-B, we derive the time-dependent analytical expression for $Na^+$ density profile $n(x,t)$ in region II [(7) and region III (9)]. Inserting $n(x,t)$ in (11), we find

$$\Delta V_{th} = \frac{\kappa\epsilon_0 V_0}{2h \cdot C_0} \cdot \left[-2\ln\left(1 - \frac{t/t_0}{2}\right)\right]^2 \cdot n_{II}(t) + V_{th,I} \quad (t < t_1) \tag{12}$$

$$\Delta V_{th} = \frac{\kappa\epsilon_0 V_0}{h \cdot C_0} \cdot \left[\frac{n_{II}(t_1)}{2} + \frac{9}{8}\left(\frac{t - t_1}{t_0}\right)\left(1 - \frac{kT}{2qV_0}\right)\right] + V_{th,I} \quad (t > t_1) \tag{13}$$

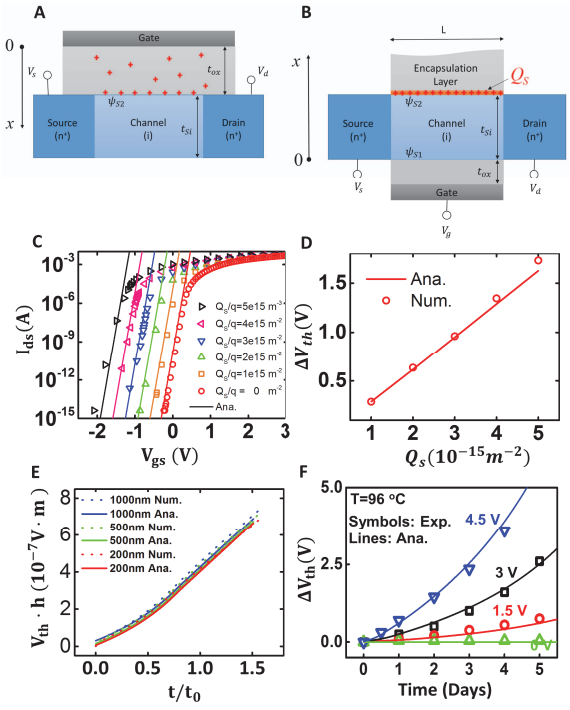


Fig. 3. Implantable electronic device performance degradation. (A) Schematic illustration of front-gate ISFET potentiometric sensor. (B) Schematic illustration of back-gate signal processing MOSFET. (C) Back-gate MOSFET $I_d$–$V_g$ curve with various back-gate charge surface density $Q_S$. Numerical (symbols) simulation vs. analytical (lines) result. (D) Back-gate MOSFET $\Delta V_{th}$ as a function of $Q_S$. (E) Front-gate MOSFET implantable device $\Delta V_{thas}$ a function of normalized time for different ion barrier thickness. Numerical (dashed lines) versus analytical (solid lines) results. (F) Back-gate MOSFET implantable device threshold voltage shift within five days soaking test under different $V_0$. Experimental (symbols) versus analytical (lines) results.

where $V_{th,I}$ is the threshold voltage shift contributed by in region I (see Fig. 2). Recall that we can treat $n_1(t)$ as a time-independent delta-function (once $t > t_1$), therefore the corresponding $V_{th}$ shift is also a time-independent constant. Our numerical simulations conclusively prove that this assumption is justified for the range of thicknesses typical of WIE systems.

Fig. 3(E) shows the product of threshold voltage shift and encapsulation layer thickness ($\Delta V_t \cdot h$) as a function of normalized time ($t/t_0$). Remarkably, all six curves scale to form a universal curve with two characteristic phases. The first phase corresponds to $t/t_0 < t_1/t_0$ when the $Na^+$ density front is yet to reach the other boundary of the ion barrier. Both numerical and analytical results (12) show a nonlinear $\Delta V_{th}$ increase. During the second phase where $t/t_0 > t_1/t_0$, $\Delta V_{th}$ is contributed by the accumulated surface charges in region III (at the encapsulant/Si interface.) (13) shows $\Delta V_{th}$ increases approximately linearly with time. This linear relationship is also confirmed by the COMSOL numerical simulation.

Similar to the concept of equivalent oxide thickness for classical MOSFET where different gate oxide materials share the same gate capacitance, we can also define an equivalent ion barrier effective thickness (EIBT) for various encapsulation layer materials. Two materials with same EIBT will be equally effective in protecting the MOSFET from ion-induced instability in a fluidic environment. From (13), we can derive an approximate compact expression at $t > t_1$ as

$$h \propto \sqrt[3]{D \cdot \kappa}. \tag{14}$$

The appearance of dielectric constant and mobility in (14) (as well as the cube-root dependence) reflects the space-charge-limited ion transport that defines the functional lifetime of MOSFETs. We will use this EIBT concept in Section IV to compare the performance of two candidate encapsulation layer materials.

### B. Back-Gated MOSFET for Signal Processing

Equation (9) defines the dependence of the surface charge density $Q_s$ on $V_0$ and the PBS soak time. In this Section, we will relate $Q_S$ to $\Delta V_{th}$ for a back-gated MOSFET within a WIE system.

Fig. 3(B) shows the 2-D cross section of embedded nMOS device underneath the ion protection encapsulation layer. For simplicity, we will focus on long channel transistors. Since the channel length ($L = 20\mu$m) is much larger than the Si substrate thickness ($t_{Si} = 100$ nm), we can simply solve for $V_{th}$ in 1-D as indicated in the $x$-direction. The assumption is easily removed, if needed [34].

We solve the simplified Poisson's equation in intrinsic Si channel MOSFET

$$\frac{\partial^2 \psi(x)}{\partial x^2} = \frac{q}{\kappa_{Si}\epsilon_0} \cdot n_i \cdot \exp\left[\frac{q \cdot \psi(x)}{kT}\right] \tag{15}$$

where $\psi(x)$ is the local potential at position $x$, $n_i$ is the electron density in intrinsic Si. By integrating both side with $x$ and applying the corresponding boundary conditions, the overall charge density inside the channel $Q_{total}$ and the potential at the back-gate oxide/channel interface $\psi_{S1}$ can be expressed as a function of $Q_s$

$$Q_{total} = \epsilon_{Si} \cdot \sqrt{\frac{2kTn_i}{\kappa_{Si}\epsilon_0} \cdot \left(\exp\left(\frac{q \cdot \psi(x)}{kT}\right) - \exp\left(\frac{q \cdot \psi_{S2}}{kT}\right)\right) + \left(\frac{Q_S}{\kappa_{Si}\epsilon_0}\right)^2} \tag{16}$$

$$\psi_{S1}(Q_S) = \frac{kT}{q} \ln\left[\left(\frac{Q_S \cdot Q_{ch}}{kT \cdot \kappa_{Si}\epsilon_0 \cdot n_i}\right) - \ln\left(\exp\left(\frac{Q_S}{kT \cdot C_{Si}}\right) - 1\right)\right] \tag{17}$$

where $Q_{ch}$ is defined as the charge density inside the Si channel when the $V_g$ reach the threshold voltage.

By inserting (16) and (17) back to the general expression for gate voltage: $V_G = \psi_{S1} + \psi_{fb} - (Q_{total}/C_{ox})$, the overall front-gate threshold voltage shift can be calculated as

$$\begin{aligned}\Delta V_{th}(Q_S) &= V_{th}(Q_S) - V_{th}(0) \\ &= -\frac{Q_S}{C_{ox}} + \frac{kT}{q} \ln\left[\left(\frac{Q_S \cdot Q_{ch}}{kT \cdot \kappa_{Si}\epsilon_0 \cdot n_i}\right) \right. \\ &\quad \left. - \ln\left(\exp\left(\frac{Q_S}{kT \cdot C_{Si}}\right) - 1\right)\right] \\ &\quad - \frac{kT}{q} \ln\left(\frac{Q_{ch}}{t_{Si} \cdot n_i}\right).\end{aligned} \tag{18}$$

The physical meaning of (18) is clear, the first three terms containing $Q_s$ correspond to the additional back-gate surface charge $Na^+$ that have penetrated the encapsulant. Both gate oxide capacitance $C_{ox}$ and $Si$ capacitance $C_{si}$ play important roles in this expression. The last term relates to the $\Delta V_{th}$ under standard MOSFET operation.

We can also express the $I_{ds}-V_{gs}$ relation under the influence of $Q_S$ as [33]

$$I_{ds} = \mu \frac{W}{L}\int_0^{V_{ds}} Q_{ch} dV_{ch} = \mu \frac{W}{L}\frac{(kT)^2 \cdot n_i \cdot \kappa_{Si}\epsilon_0}{Q_S} \cdot \exp\left[\frac{q}{kT}\left(V_{gs}-\Psi_{FB}+\frac{Q_S}{C_{ox}}\right)\right] \cdot \left[\exp\left(\frac{qQ_S}{kTC_{Si}}\right)-1\right]\cdot\left[1-\exp\left(-\frac{V_{ds}q}{kT}\right)\right]. \quad (19)$$

Fig. 3(C) shows the $I_{ds} - V_{gs}$ curves with different $Q_S$. In the sub-threshold region, the analytical solutions (solid lines) match perfectly with the Sentaurus numerical device simulation results (symbols). Fig. 3(D) shows the corresponding $\Delta V_{th}$ as a function of $Q_S$, with good match between the numerical and analytical simulations.

Fig. 3(F) shows the experimental data for the overall back-gated MOSFET threshold voltage shift for a soaking period of five days. To accelerate ion penetration, the soaking test was conducted at 96 °C. For simplicity, we assume that $Na^+$ diffusion coefficient follows an Arrhenius relationship [35]. The externally applied voltage ranges from 0 to 4.5 V, with an increment of 1.5 V. The drift-diffusion process is accelerated with increasing $V_0$, which leads to an increasing $\Delta V_{th}$. As we have mentioned in Section II-B, another interesting observation is that $\Delta V_{th}$ increases nonlinearly as a function of time. This phenomenon is caused by the dissolution of ion barrier (thermal $SiO_2$ in the experiment) at extreme high temperature (96 °C). As the encapsulation layer shrinks the average electric field across the encapsulant rises, which further accelerates the ion penetration process. Thus, we apply the dissolution model from Section II-B with the experimentally calibrated dissolution rate ~90 nm/ day at 96 °C. The analytical results predicted by this model (solid lines) perfectly reproduce the experimental data (solid dots).

With the validated model for both front-gated and back-gated MOSFETs, we are now ready to develop design principles for application-specific robust encapsulation of the WIE systems.

## IV. Results and Discussion

In this section, we will use both the numerical and analytical models to develop guidelines for the design of ion encapsulation layer. We will compare the performance of two widely used encapsulation layer materials ($SiO_2$ and $SiN_x$) along with their coupled bi-layer structure. Finally, we will provide a phase plot for mapping the failure time for back-gated MOSFET at various bias and temperature.

We apply the EIBT relationship derived in Section III-A for thermal $SiO_2$ and $SiN_x$. Comparing to a 200 nm $SiN_x$ encapsulation layer, the EIBT for $SiO_2$ is ~4500 nm by (14). In Fig. 4(D), we plot the front-gate MOSFET $\Delta V_{th}$ versus $t$

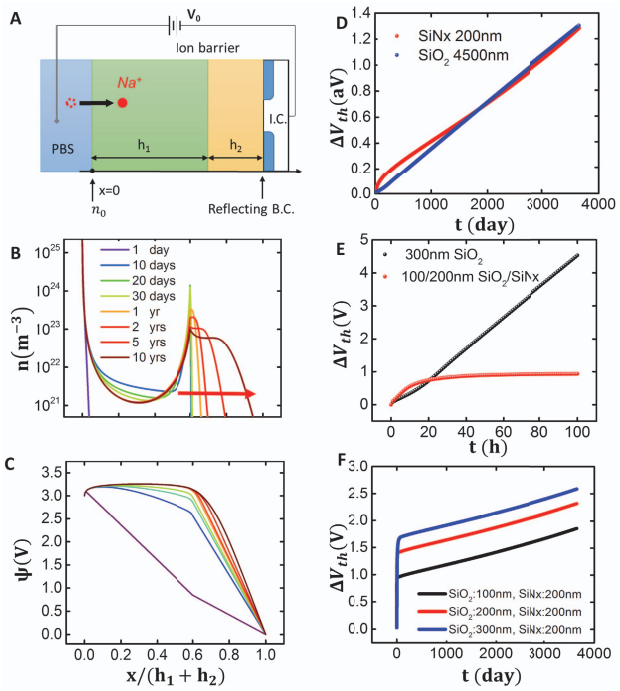


Fig. 4. Comparison of single layer/bi-layer encapsulant for front-gate MOSFET case. (A) Schematic illustration of sodium ion penetration in 1-D bi-layer ion barrier domain with external applied voltage $V_0$. (B) and (C) $Na^+$ concentration, electrical field and potential distribution within $h_1 = 300$ nm thermal $SiO_2$ and $h_2 = 200$ nm $SiN_x$ bi-layer ion barrier structure at the end various simulation time. The external bias is fixed at 3 V. D. Comparison of front-gate MOSFET $\Delta V_{th}$ for 200 nm $SiN_x$ and 4500 nm $SiO_2$. (E) Comparison of front-gate MOSFET $\Delta V_{th}$ under (1) 300-nm single-layer $SiO_2$ ion barrier. (2) 100/200-nm $SiO_2/SiN_x$ bi-layer ion barrier. (F) Comparison of front-gate MOSFET implantable device $\Delta V_{tunder}$ $SiO_2/SiN_x$ bi-layer structure with 100/200/300 nm $SiO_2$ and 200 nm $SiN_x$.

for both designs. Except for slight initial difference, the two curves are essentially identical for $t > t_1$. Therefore, a 200 nm $SiN_x$ layer has the same ion blocking capability as a 4500 nm $SiO_2$ layer. Obviously, materials with low ion diffusion coefficient is a good encapsulation layer candidate material especially for thin-film front-gate MOSFET-based WIE systems, but the additional effect of the dielectric constant ($\kappa$) is equally important and must be accounted for.

If $SiN_x$ is so effective in preventing ion diffusion, then why not design encapsulation layers based exclusively on $SiN_x$? Recall that in the analysis above, we focused exclusively on ion-induced instability of MOSFETs. Moisture penetration and corresponding corrosion/delamination, however, could be equally important degradation mechanisms for WIE system. In our previous work [22], we experimentally demonstrated that while thermal $SiO_2$ is a good moisture barrier material, $SiN_x$ is not. Therefore, the requirement for multiobjective encapsulation against moisture, ion presentation, and hydrolysis requires a stacked encapsulation approach, as follows.

As an illustrative example, let us consider a bi-layer $SiO_2/SiN_x$ encapsulation where the top thermal $SiO_2$ layer ($h_1 = 300$ nm) prevents moisture ingress, while the bottom $SiN_x$ layer ($h_2 = 200$ nm) suppresses $Na^+$ penetration [see Fig. 4(A)]. As before, we solve the coupled drift-diffusion equation and Poisson's equation [(1) and (2)] for a 1-D domain, with a $V_0 = 3$ V. The diffusion coefficients at 37 °C

are: $6.53\times10^{-21}$ m$^2$/s for thermal $SiO_2$ and $4.94\times10^{-25}$ m$^2$/s for $SiN_x$. Due to the four orders of magnitude difference in the diffusion coefficients, $Na^+$ penetrates the top $SiO_2$ layer at a much faster rate than the $SiN_x$ layer. Fig. 4(B) shows that within the first ten days, $Na^+$ ions build up inside the $SiO_2$ layer and reach a quasi-static profile. At the $SiO_2/SiN_x$ interface, $Na^+$ accumulates because of the $Na^+$ influx coming from the thermal $SiO_2$ side is much larger than the outflow into the $SiN_x$ side. After this initial transient, $Na^+$ begins to slowly penetrate into the $SiN_x$ layer. From one year up to ten years, the drift-front of $Na^+$ slowly approaches the $SiN_x$ layer. During this period, the accumulated $Na^+$ peak at $SiO_2/SiN_x$ interface gradually reduces in order to balance the amount of $Na^+$ injected into the $SiN_x$ layer.

Fig. 4(C) shows the potential distribution inside $SiO_2/SiN_x$ bi-layer structure. Initially, there is no free charge in the dielectrics, therefore the potential drops linearly over the two layers, with the ratio defined by their respective dielectric constants. Once $Na^+$ penetrates and saturates within $SiO_2$ layer, the potential at the $SiO_2/SiN_x$ interface rises quickly and approaches $V_0$. At the end of first month, most of potential drop distributes linearly over the $SiN_x$ layer. After one year, a self-induced potential barrier with $V_{\max} > V_0$ builds up inside the $SiO_2$ layer. The potential distribution across the $SiN_x$ layer gradually shows a nonlinear profile reflecting the slow penetration of $Na^+$ ions.

To compare the performance of the bi-layer ion barrier design to the single layer $SiO_2$ structure, we plot $\Delta V_{\text{th}}$ versus $t$ for front-gate case from our numerical simulation in Fig. 4(E). For the bi-layer layer structure (red line), $\Delta V_{\text{th}}$ increases within 0 to 20 h, then saturates to a constant value. The initial $\Delta V_{\text{th}}$ jump is due to the large amount of $Na^+$ penetrating into the $SiO_2$ layer where the ion diffusivity is relatively large. The saturation happens when $Na^+$ reach the second $SiN_x$ layer and penetrates at a much slower rate. For a single-layer $SiO_2$ (black line), however, there is no second ion barrier. As a result, $\Delta V_{\text{th}}$ increase and the implanted MOSFET device degrades at a much faster rate.

Fig. 4(F) explores the influence of the thickness of the top thermal $SiO_2$ layer ($h_1$) on the overall MOSFET degradation. We numerically simulate three bi-layer structures with 100, 200, and 300 nm top layer $SiO_2$ thickness and keep the same 200 nm thickness of $SiN_x$. Counter-intuitively, the thickner $SiO_2$ top layer produces higher initial $\Delta V_{\text{th}}$ jump; although one expects thicker oxides to reduce degradation. This counter-intuitive result can be explained as follows. As illustrated by (11), it is not the density, but the density moment of the spatially distributed $Na^+$ ions in the encapsulant that define to the threshold voltage shift of a front-gated MOSFET. Fig. 4(B) shows that $Na^+$ ions penetrate through the top $SiO_2$ layer and reach a saturated density profile in a relatively short period of time, however in a thicker oxide, the density moment of the charge profile, especially the peak at the $SiO_2/SiN_x$ interface, resides further away from the MOSFET top gate interface compared to a thinner oxide. This larger moment of $Na^+$ in $SiO_2$ layer in thicker oxides accounts for the higher initial $\Delta V_{\text{th}}$ jump in Fig. 4(F). After the initial jump, all three lines become parallel to each other and increase at a much slower rate reflecting $Na^+$ diffusion into the second $SiN_x$ layer. From the pure ion penetration point of view, thinner top moisture layer can effectively slow down the front-gate MOSFET device degradation process. But if we consider the dissolution of the barrier material, there is a trade off in the design of the moisture barrier layer thickness. We can select an optimal thickness of moisture barrier layer by considering both the material dissolution as well as $Na^+$ penetration.

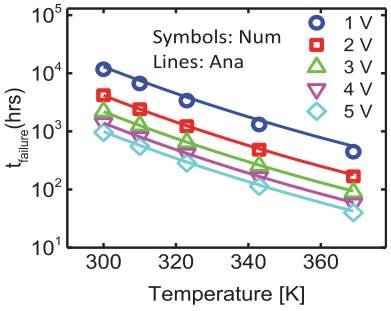


Fig. 5. Phase plot of back-gate MOSFET failure time as a function of temperature with sweeping $V_0$.

Next, we are going to utilize our model to map the back-gate implantable MOSFET failure time from the high-temperature soaking test back to their normal operation temperature. Fig. 5 shows a phase plot of $V_0$ and $T$ dependent failure time ($t_{\text{failure}}$) of back-gate MOSFET implantable device. The symbols are from our numerical simulation, while the lines are calculated from our analytical model, derived by combining (9) and Arrhenius equation to relate $t_{\text{failure}}$, $T$, and $V_0$

$$\ln\ (t_{\text{failure}}) = \frac{E_A}{kT} - \ln\left(\frac{\kappa\epsilon_0 D_0}{kTqh}V_0^2\right) + \text{Constant} \qquad (20)$$

where $D_0$ is the pre-exponential factor and $E_A$ is the activation energy.

In this particular case, we choose $t_{\text{failure}}$ to correspond to $\Delta V_{\text{th}} = 1$ V, related to the surface $Na^+$ density of, $Q_{s,\text{th}}/q \sim 3\times10^{15}$ m$^{-2}$ [see Fig. 3(C)]. Several observations can be made from the phase plot. First, the numerical and analytical results both support the trend that lifetime is reduced at higher temperature due to the enhanced $Na^+$ mobility. Second, high external bias $V_0$ accelerates the $Na^+$ drift process and shortens the MOSFET failure time. We note that while the match between analytical and numerical results are good, they are not exact, especially at low $V_0$. This is because our analytical model presumed ion diffusion to be unimportant compared to ion drift. This is a poor approximation at very low $V_0$. As a result, the failure time from the numerical simulation is slightly shorter than the analytical one at low bias ($V_0 = 1$ V). At higher bias, drift dominates diffusion, and the difference disappears.

From the failure time phase plot, we can simply map the failure time in high-temperature soaking test back to the normal operation temperature device failure time under different external bias voltage profiles.

## V. Conclusion

The stability of MOSFET-based electronic components in WIE systems is of great interest. Ion penetration is one of

TABLE I
LIST OF PARAMETERS IN THE SIMULATION

| Figure, Plot | Parameters |
|---|---|
| 2, B-D | $D = 6.53 \times 10^{-21} m^2/s$ , $T = 37°C$ |
| 3, B | $L = 20\mu m, W = 300\mu m, t_{ox} = 40\ nm, t_{Si} = 100\ nm, V_{ds} = 1V,$ $N_{D,Source/Drain} = 10^{19} cm^{-3}$ |
| 3, C-D | $Q_{ch} = 7.8 \times 10^{8}\ m^{-3}$ |
| 3, E | $D = 6.53 \times 10^{-21} m^2/s$ , $T = 37°C$ |
| 3, F | $D = 1.05 \times 10^{-19}\ m^2/s, r_{dis} = 90\ nm/day, T = 96°C$ |
| 4 B-F | $SiO_2 : D = 6.53 \times 10^{-21} m^2/s, T = 37°C$ $SiN_x : D = 4.94 \times 10^{-25} m^2/s, T = 37°C$ |
| 5 | $D_0 = 2.29 \times 10^{-12} m^2/s, E_A = 7.43 \times 10^{-20} J$ |

the most significant problems that degrades the device performance. The design of proper encapsulation layer requires systematic theoretical analysis. In this paper, we have developed numerical and analytical frameworks for lifetime prediction of MOSFET-based components in WIE systems. More generally, the modeling framework can be used to solve ion penetration problems in a broad range of electrochemical applications. The predictions are validated by accelerated soaking experiment. The model suggests optimum design given in the multiple design parameters (such as encapsulation thickness, ion diffusivity in an encapsulation material, temperature, and external voltage bias and encapsulation layer dissolution). Our analysis suggests that a bi-layer or tri-layer encapsulation may be essential for multiobjective protection. Since this paper focuses on the design of encapsulants as ion/moisture barrier, we have compared the blocking effectiveness of inorganic encapsulants. For *in vivo* applications, however, a layer of organic material (such as parylene C) must be added to the encapsulant stack to satisfy the biocompatibility requirements between body tissue and the WIE systems.

## APPENDIX

See Table I.

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