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Materials and fabrication sequences for water soluble silicon integrated circuits at the 90 nm node

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Tungsten interconnects in silicon integrated circuits built at the 90 nm node with releasable configurations on silicon on insulator wafers serve as the basis for advanced forms of water-soluble electronics. These physically transient systems have potential uses in applications that range from temporary biomedical implants to zero-waste environmental sensors. Systematic experimental studies and modeling efforts reveal essential aspects of electrical performance in field effect transistors and complementary ring oscillators with as many as 499 stages. Accelerated tests reveal timescales for dissolution of the various constituent materials, including tungsten, silicon, and silicon dioxide. The results demonstrate that silicon complementary metal-oxide-semiconductor circuits formed with tungsten interconnects in foundry-compatible fabrication processes can serve as a path to high performance, mass-produced transient electronic systems. © *2015 AIP Publishing LLC*.
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Transient electronics represents an emerging technology whose key characteristic is that its active elements physically disappear, completely or selectively, at controlled rates and/or programmed times.[1,2] Such behavior is markedly different from that of traditional electronics, where the long-standing engineering design goal has been to maximize reliability and timescales for stable operation by avoiding any physical change in the constituent materials. Classes of transient electronics that can dissolve in ground water or biofluids to yield environmentally and biologically benign end products are particularly important due to their potential to eliminate hazardous electronic waste streams associated with consumer electronics and to enable temporary biomedical devices with active diagnostic or therapeutic function.[1,3,4] Although organic electronic materials can be considered for such applications,[5–7] silicon nanomaterials, in general,[8,9] and nanomembranes, in particular, are appealing because they offer both high performance characteristics and alignment with the deep base of engineering and scientific knowledge associated with the established electronics industry.

An enabling recent observation in this context is that semiconductor-grade monocrystalline silicon can undergo hydrolysis at low but significant rates (5–90 nm/day) in physiological conditions,[1,2,10] to yield water-soluble, biocompatible reaction products (i.e., silicic acid).[11,12] Additional results show that silicon dioxide, silicon nitride, and magnesium oxide can also slowly dissolve by hydrolysis, thereby providing attractive choices for dielectric materials.[1,13,14] Thin films of metals such as magnesium (Mg), zinc (Zn), molybdenum (Mo), and tungsten (W) represent options for electrodes and electrical interconnects.[15–19] Combining these materials on bioresorbable substrates (e.g., PLGA, silk)[5,20] using the techniques of transfer printing[21,22] yields fully transient semiconductor devices of various types, ranging from transistors and diodes, to solar cells, photodetectors, radio frequency energy harvesters, temperature and pH sensors, degradable batteries, and many others.[1,22–24] Circuits are also possible although existing examples involve modest/low levels of integration, limited by the capabilities of the processing tools used in existing research demonstrations. Further advances in the technology rely critically on an ability to leverage the manufacturing infrastructure that exists for silicon digital integrated circuits. The present work focuses on materials, device, and circuit aspects of transient silicon complementary metal-oxide-semiconductor (CMOS) circuits that use silicon dioxide (SiO_2) and tungsten as the dielectric and interconnect materials, respectively, in foundry-compatible processing sequences. Systematic studies and modeling efforts reveal the dissolution characteristics of the key materials as well as the performance properties and degradation profiles of devices and integrated circuits, including 499 stage CMOS ring oscillators.

The fabrication exploits a modified CMOS process with 8-in. silicon on insulator wafers (SOI; 40 nm device silicon and 200 nm buried oxide) and projection mode photolithographic tools capable of reaching the 90 nm design node. A key modification is the use of W, which is known to undergo hydrolysis in aqueous solutions at physiological conditions,[10] not only for its traditional role in vias but also for all interconnect metallization. Here, after electrical testing of transistors and ring oscillators fabricated in the usual way, the first level of aluminum (Al) was removed by chemical-mechanical planarization (CMP) to leave the interlayer dielectric and the W via plugs. Chemical vapor deposition

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(CVD) formed films of W that were photolithographically patterned with the same mask used for the Al and a tetrafluoromethane (CF_4) based etch process (Centura®, Applied Materials). A top-view optical micrograph of a typical test die formed in this way appears in Figure 1(a). This example includes various devices (resistors, capacitors, transistors, and ring oscillators). Figure 1(b) presents a corresponding cross sectional schematic illustration of a representative structure that includes one layer of interconnect W metal. Here, the interlayer dielectric is SiO_2 (0.25 and 1 μm for the two layers used here) deposited by plasma-enhanced chemical vapor deposition (PECVD). The top layer SiO_2 above the metal pads was etched open to enable measurement, in a process termed "pad cut." Thermally grown SiO_2 (10 nm) serves as the gate dielectric. Elimination of the handle substrate of the SOI wafer involved first bonding it face down (Waferbond® Temporary Bonding Material, Brewer Science Inc.) on another temporary wafer. Precision wafer grinding to a thickness of 75 μm followed by deep silicon reactive ion etching completed the process.[25] The temporary wafer can be cleaved or diced into chips, such that the remaining (0.6 μm thick) circuit layer with transistors and interconnects can be released with a solvent that removes the bonding material. In this format, the chips are mechanically flexible and can be transfer printed to a biodegradable substrate; Figure 1(c) shows the case of silk fibroin (silk thickness $\sim$60 μm).

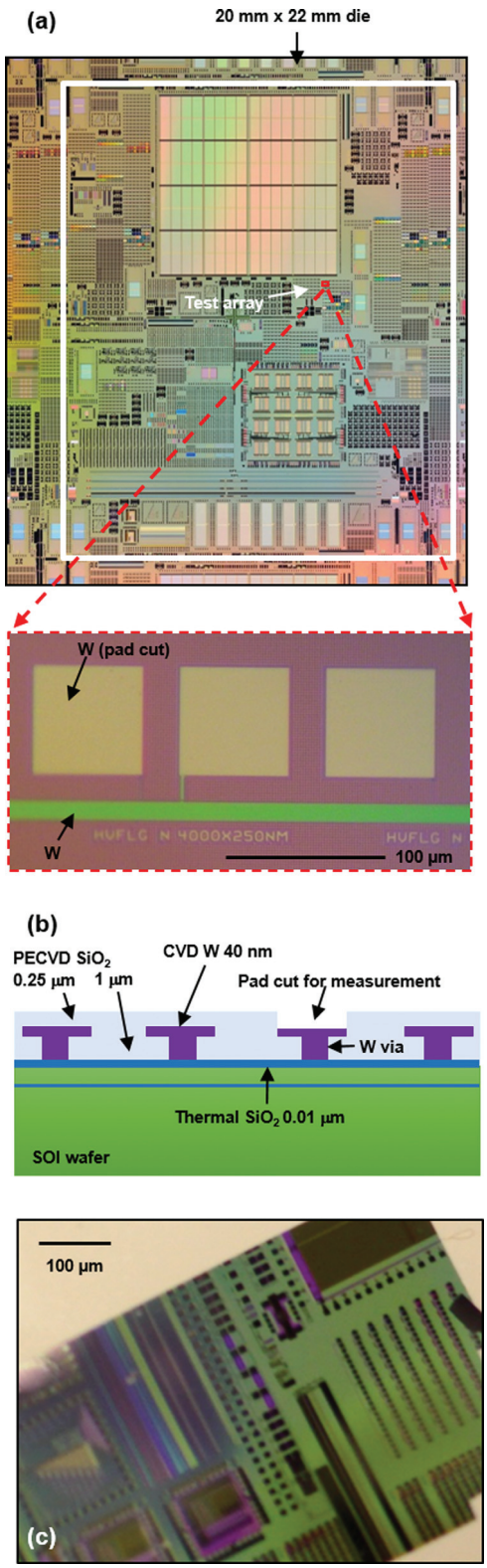

FIG. 1. (a) Top view optical micrograph of a typical CMOS die with W interconnect metallization formed on an SOI wafer, with magnified view of a selected region to illustrate the W metallization; (b) schematic cross-sectional illustration of the various layers in such a die; and (c) image of the segment of this die after removal of the handle wafer and transfer to a flexible substrate of silk fibroin.

The CVD W reacts with water to form WO_x.[15] Figure 2(a) presents a sequence of scanning electron microscope (SEM) images of the evolution of surface microstructure of a uniform W film (200 nm) at various times of immersion in deionized (DI) water at room temperature. As dissolution proceeds, the thickness decreases and a textured, microporous surface develops. Loss of electrical continuity (resistance increased by a factor of 40) in the W serpentine traces occurs after 12 days.[15] Disappearance of the material altogether requires $\sim$4 weeks of immersion. The resistivity 1560 nΩ m evaluated using processed test structures with 40 nm thickness is comparable to that of CVD deposited W films with similar thickness, although higher than that of bulk W (52.8 nΩ m), due to known effects in enhanced surface and grain boundary scattering.[26,27] This value also exceeds that for copper (Cu) and Al thin films, whose values are $\sim$25 and 34 nΩ m, respectively.[28] Process modifications will allow the use of thicker films of W.

Electromagnetic simulations summarized in Figures 2(b) and 2(c) reveal the effects of interconnect resistance on pulsed signal transmission. As shown in Figure 2(b), the model consists of a transmission line for signal propagation through a trace centered between two grounded conductors, each with 100 nm spacing and 1 mm length. Cases considered include lines with heights of 220 nm, 115 nm, and 200 nm for Cu, Al, and W, respectively. The signal emerges from a low-impedance source and the resulting signal appears at the output of a receiving gate. The influence of increased metal resistance is most prominent for high-speed signals propagation on long wires; turn-to-turn capacitances have large effects on propagation delay under these circumstances. Varying the input pulse width allows determination of the minimum pulse width needed to obtain full amplitude signal at the output of the receiving gate. The simulated results of Cu, Al, and W appear in Figure 2(c). As expected, the W lines exhibit slower rise and fall times and higher propagation delays than those of Cu and Al. The results suggest, however, that clock frequencies >500 MHz can be

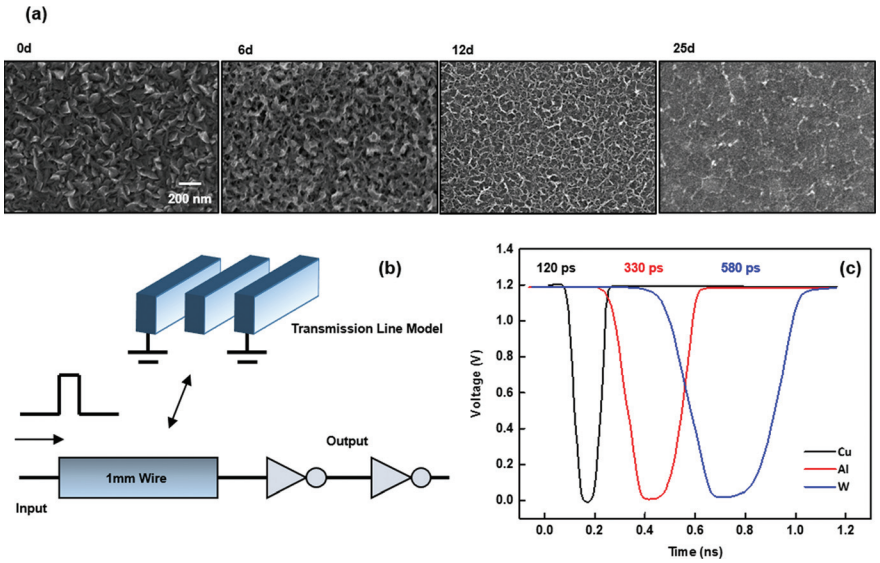

FIG. 2. (a) Images showing the evolution of the microstructure of W interconnects due to immersion in DI water, immediately after immersion (0 day), and after 6, 12, and 25 days; (b) schematic illustration of the transmission line model; and (c) simulated pulsed signal outputs for cases of different interconnect metals and thicknesses.

achieved using the W approach reported here. Increased resistance can also lead to significant power drops across distribution wiring in large, high-power integrated circuits. Simulation results compare the voltage distributions for Al and W wiring across a 5×5 mm chip with an array of 0.1 μA current sources that load the power grid at 1 V. The grid consists of 1-μm-wide horizontal traces and 5-μm-wide vertical traces both with a 100–μm pitch. The results suggest that although the W case shows higher voltage drop (0.01 V) than Al (0.001 V), the differences are small and manageable through appropriate circuit design techniques.

The performance of n- and p-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) with different gate lengths (90 nm, 110 nm, 150 nm, and 300 nm) and W metallization appear in Figures 3(a) and 3(b). Here, the drain current is normalized for a 2 μm gate width. The on/off ratios are $>10^5$ for all cases; the threshold voltages are $\sim$0.4 V and ~ -0.5 V for n-MOSFETs and p-MOSFETs, respectively. The peak transconductances are 0.03–0.1 mS/μm (n-MOSFET) and 0.02–0.05 mS/μm (p-MOSFET); and the subthreshold swings are 75–90 mV/decade (n-MOSFET) and 85–100 mV/decade (p-MOSFET). Figure 3(c) illustrates a $\sim$20-MHz waveform measured from a ring oscillator that incorporates 499 stages formed with W interconnects between similar types of W-based MOSFETs. This oscillation frequency corresponds to a gate delay of $\sim$50 ps. Otherwise, identical circuits that use Al instead of W have gate delays of $\sim$25 ps. Although the square wave does not saturate due to the series resistance of the W output lines, the gate delay time and frequency compare favorably to similar circuits built with Al interconnects.

The principal unique feature of this type of CMOS technology is that all of the constituent electronic materials can dissolve by hydrolysis. Detailed studies of dissolution behaviors of silicon, silicon dioxide and W appear elsewhere.[2,13,15] For the circuits reported here, dissolution of SiO_2 represents rate limiting step due to its significant thickness ($\sim$1.25 μm) and slow rate ($\sim$1 nm/day for PECVD SiO_2 and $\sim$0.1 nm/day for thermal SiO_2 at 37 °C in bovine serum (Sigma-Aldrich) at pH 7.4).[13] Estimated times to dissolve the various materials in the circuits presented here, in pH 7.4 solutions

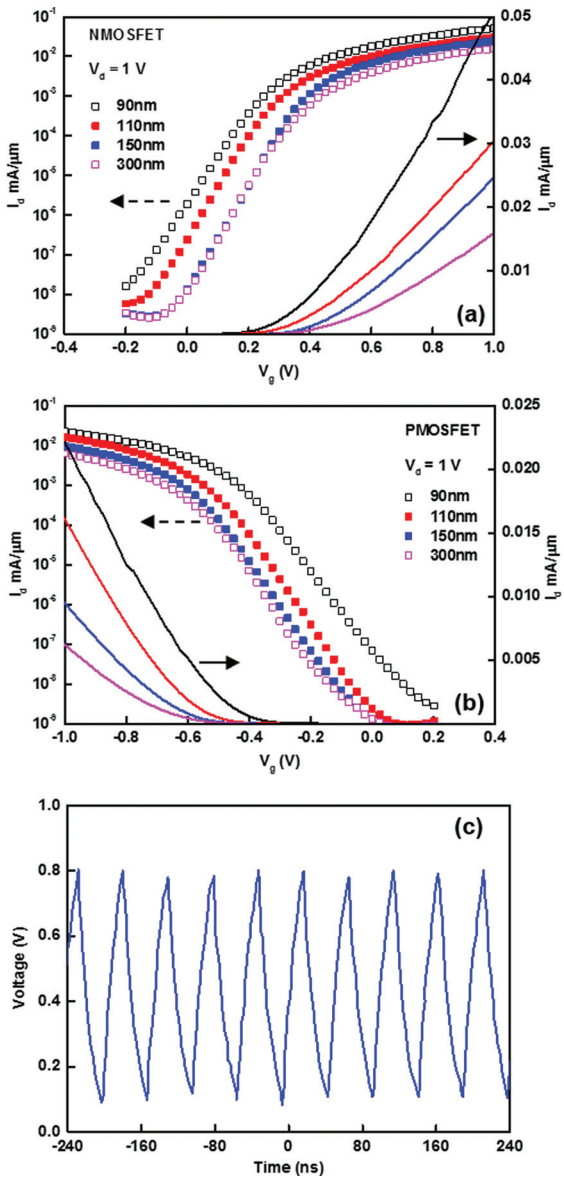

FIG. 3. (a) Current-voltage characteristics of a representative transient n-MOSFET, where I_d is the drain current and V_g is the gate voltage, for a drain bias, V_d, of 1 V; (b) current-voltage characteristics of a representative p-MOSFET; and (c) output voltage recorded from a 499 stage CMOS ring oscillator.

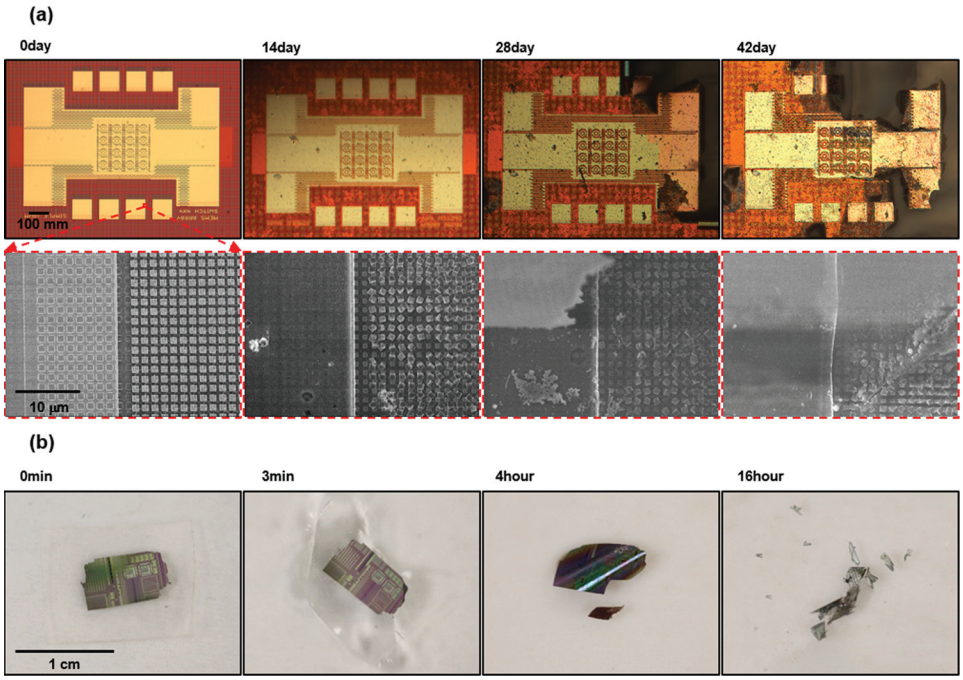

FIG. 4. (a) Optical and SEM micrographs of selected regions of a transient CMOS die at various times during accelerated dissolution tests conducted by immersion in phosphate buffered saline at 70 °C and pH 10, immediately after immersion (0 day), and after 14, 28, and 42 days; (b) optical images of dissolution of an ultrathin transient CMOS die on a silk substrate at various times after immersion in a similar solution, immediately after immersion (0 min), and after 3 min, 4 and 16 h.

at 37 °C are: 3 months for the thermal SiO_2 gate dielectric, and 3 years for the PECVD SiO_2 interlayer dielectric in bovine serum; 1 week for the W interconnect, 2–6 months for the W via plugs, and 3 months for the doped device Si in phosphate buffered saline. We note that these rates can depend strongly on the concentration and type of ions in the solution (e.g., dissolution rates for Si and SiO_2 in bovine serum are at least ten times higher than those in standard phosphate buffered saline solutions),[10,13] and on details such as the extent of flow and agitation of the liquid. In addition, the deposition methods can strongly affect the dissolution times. Reducing the thickness of the interlayer dielectric to ~100 nm should allow its dissolution in bovine serum within ~3 months. Alternatively, similar dissolution times can be achieved by use of SiO_2 deposited by electron-beam evaporation, which has a dissolution rate that is up to 100 times faster than that associated with SiO_2 formed by PECVD.[13] As described subsequently, dissolution of the circuits does not strictly follow a layer-by-layer mode, but instead can involve mechanical fracture during the dissolution, thereby further decreasing the time for degradation.

Accelerated tests of circuits in phosphate buffered saline pH 10 at 70 °C allow rapid evaluation of the structural variations with time. Optical and SEM images appear in Figure 4(a). The W dissolves first followed by gradual dissolution of PECVD SiO_2. Simultaneously, the solution appears to penetrate through the overlying layers to initiate hydrolysis of the device Si in some locations. This behavior leads to non-uniform dissolution instead of a layer-by-layer mode, as shown in Figure 4(a). For ultrathin circuits transferred to thin silk substrates, immersion in phosphate buffered saline pH 10 at 70 °C leads to rapid dissolution of the silk, which leads to fracture and disintegration of the mechanically fragile circuit elements (Figure 4(b)). Chemically and mechanically engineering the substrates clearly provide additional means for controlling the rates of transience in operation of these types of systems. The addition of encapsulation materials can ensure a desired functional lifetime.

In summary, this work establishes materials and processing routes for transient electronics in the context of modern CMOS-compatible materials and processing techniques. The essential advances are in the development of methods for using W as interconnect metallization and for thinning and transferring processed die to transient substrates. The outcomes are highly relevant to the use of transient electronics in advanced applications.

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