

Recent Progress in Obtaining Semiconducting Single-Walled Carbon Nanotubes for Transistor Applications

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High purity semiconducting single-walled carbon nanotubes (s-SWCNTs) with a narrow diameter distribution are required for high-performance transistors. Achieving this goal is extremely challenging because the as-grown material contains mixtures of s-SWCNTs and metallic- (m-) SWCNTs with wide diameter distributions, typically inadequate for integrated circuits. Since 2000, numerous *ex situ* methods have been proposed to improve the purity of the s-SWCNTs. The majority of these techniques fail to maintain the quality and integrity of the s-SWCNTs with a few notable exceptions. Here, the progress in realizing high purity s-SWCNTs in as-grown and post-processed materials is highlighted. A comparison of transistor parameters (such as on/off ratio and field-effect mobility) obtained from test structures establishes the effectiveness of various methods and suggests opportunities for future improvements.

1. Introduction

Single-walled carbon nanotubes (SWCNTs) are tubular cylinders of carbon atoms, whose discovery in 1993^[1] inspired much research on their synthesis and electronic/optoelectronic device applications. A SWCNT can either exhibit metallic or semiconducting properties, depending on the arrangement of constituent carbon atoms. Metallic SWCNTs (m-SWCNTs) have no bandgap; their high conductivity creates potential for use as conductors,^[2–5] power cables,^[2,3] interconnects,^[4–9] field emitters,^[2,10,11] batteries,^[12–16] and super-capacitors.^[17–19] Semiconducting SWCNTs (s-SWCNTs), on the other hand, have variable bandgaps (defined by their diameter), high mobili-

ties, and large surface to volume ratios; promising potential applications are in digital electronics,^[20–28] radio-frequency electronics,^[29–33] flexible electronics,^[32,34–36] optoelectronics,^[37,38] sensors,^[39–42] and photovoltaics.^[43–47] This article focuses on electronics and sensing applications of s-SWCNTs, where transistors act as the basic building block. The s-SWCNTs in transistors offer exceptionally high mobilities^[48,49] in the thinnest possible conduction path for excellent electrostatic control.^[25,26] An efficient injection of electrons and holes into s-SWCNTs is possible using metal contacts that have appropriate work functions^[50–55] when used with suitable gate dielectrics.^[25,56] Appropriate surface treatments and materials choices enable the operation of s-SWCNTs with

small hysteresis in the current–voltage characteristics.^[57–60] These collective capabilities allow the fabrication of relatively complex digital electronic systems including microprocessors,^[28] where aligned arrays of s-SWCNTs bridge the source and drain contacts of each constituent transistor to maximize performance. Random networks of s-SWCNTs can serve as alternatives for aligned array s-SWCNTs with envisioned uses in low-performance, flexible electronics,^[34,61,62] and sensor^[42,63] applications. All transistor applications of s-SWCNTs, however, require further improvements in density, purity, and doping, and in the reduction of current–voltage hysteresis and performance variability. Several notable developments in improving the density,^[27,64,65] hysteresis,^[57–60,66–68] doping,^[69–75] and variability^[76–82] of SWCNTs have appeared in recent literature. This review article focuses on achieving high purity of s-SWCNTs needed to ensure high current modulation in transistors for most electronics applications (e.g., digital electronics require transistors with $\geq 10^4$ on-current to off-current ratio or on/off ratio).^[28,83,84]

Selective growth of s-SWCNTs by chemical vapor deposition (CVD), the most widely used technique for carbon nanotube (CNT) synthesis,^[85–93] is extremely challenging. The chiral index (n, m) of the SWCNTs determines the semiconducting (with $\text{mod}(n-m, 3) = 1, 2$) or metallic (with $\text{mod}(n-m, 3) = 0$) nature. On a statistical basis, therefore, two-thirds of synthesized SWCNTs would be semiconducting and the rest (one-third) would be metallic,^[94,95] unless the synthesis uses novel catalysts,^[96–101] engineered catalyst supports,^[98,100,102–106] or specialized carbon feedstock.^[107–109] In spite of much effort, *in situ* growth techniques cannot still produce s-SWCNTs at the required level of purity ($>99.99\%$, as needed to fabricate

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transistors with $>10^4$ on/off ratio based on aligned arrays of s-SWCNTs as the channel).^[83] The ex situ removal of m-SWCNTs via post-processing, therefore, remains the only viable route to high purity s-SWCNTs. Recent review articles on such ex situ schemes^[87,110–112] (including those that discuss post-processing, along with other aspects of SWCNT electronics)^[85,89,113,114] focus on the utility of selective chemistry of SWCNTs (based on their chiral index) in different solutions to obtain different types of mono-disperse SWCNTs. These articles discuss methods for selective in situ growth of s-SWCNTs as supplementary to solution-based post-processing methods, while techniques such as electrical breakdown of m-SWCNTs^[83,115] and selective chemical etching,^[116] etc., are deemed impractical and/or ineffective. Recent research shows, however, successful use of electrical breakdown in nanoscale transistors,^[64,117] even in large systems such as microprocessors.^[28] In addition, we have recently presented ex situ strategies that exploit nanoscale thermocapillary flows (thermocapillary-enabled purification; TcEP)^[118–121] as a form of thermal lithography for complete removal of m-SWCNTs. This article summarizes both selective, in situ growth and ex situ, post-processing methods in the specific context of enabled electronic properties such as on/off ratio and charge transport characteristics. The methods discussed here are listed in **Figure 1**, with specific identifiers to corresponding sections. Section 2 presents the required electronic properties for different transistor applications. Section 3 reviews CVD synthesis techniques with in situ modifications that improve the population of s-SWCNTs and compares the on/off ratios and charge transport properties of transistors made with such SWCNTs. Section 4 summarizes ex situ, post-processing methods with emphasis on the nature and scalability of their operation and electronic properties of transistors made with post-processed SWCNTs. A summary for in situ (Figure 9, Table 1) and ex situ (Figure 25, Table 2) methods allows easy comparisons.

2. Transistors with SWCNTs: Application Challenges

The SWCNTs that define the channel of a transistor may be aligned parallel to the channel (aligned arrays of SWCNTs; **Figure 2a**) or distributed randomly in a network configuration (**Figure 2b**). Aligned arrays of SWCNTs have the potential to replace crystalline channel materials (e.g., silicon, InGaAs) in digital, analog, and radio frequency (RF) electronics; random networks of SWCNTs, on the other hand, may replace amorphous silicon and organic materials in flexible electronics and flat panel displays. In addition, SWCNTs can also be used in novel applications, such as transparent electronics, biosensors, and chemical sensors.

In digital electronics, silicon-based transistors operate with an on-current of $\approx \text{mA}$ per μm width of the device and an on-current (I_{ON}) to off-current (I_{OFF}) ratio of $>10^4$.^[28,84,122,123] Specifically, I_{ON} and I_{OFF} are defined as the maximum and minimum drain current I_{D} , respectively, during the sweep of gate to source voltage V_{GS} by keeping a fixed drain to source voltage V_{DS} . To achieve the desired I_{ON} and $I_{\text{ON}}/I_{\text{OFF}}$, one needs aligned arrays of s-SWCNTs as the channel



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at densities, $N_{\text{S}} \geq 100$ per μm (defined as the number of SWCNTs per unit width of the transistor) and also needs a field-effect mobility ($\mu_{\text{FE}} \approx \partial I_{\text{D}} / \partial V_{\text{GS}}|_{\text{max}}$) comparable to that of silicon ($\approx 500\text{--}1500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$).^[84,122,124] In this case, even a few m-SWCNTs (with density N_{M}) can degrade the purity of s-SWCNTs, defined as $N_{\text{S}}/(N_{\text{S}} + N_{\text{M}})$, and reduce $I_{\text{ON}}/I_{\text{OFF}}$ significantly (see **Figure 2c**), as follows.^[22,83,107,108] In a transistor with aligned arrays of SWCNTs as the channel,

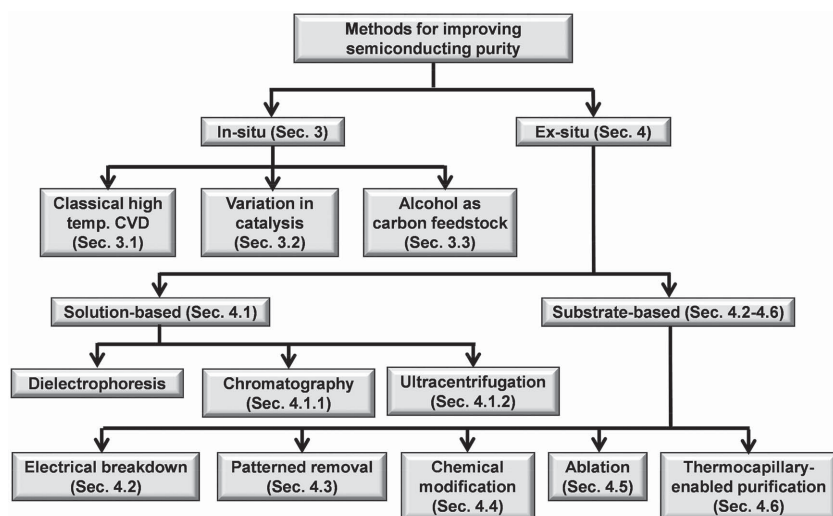


Figure 1. A categorized list of methods reviewed in this article with specific identifiers to corresponding sections.

$I_{ON} = N_M I_{ON,M} + N_S I_{ON,S}$ and $I_{OFF} = N_M I_{OFF,M} + N_S I_{OFF,S}$, where $I_{ON,S/M}$ and $I_{OFF,S/M}$ represent the maximum and minimum I_D , on average, for s-/m-SWCNTs. If we assume $I_{ON,S} \approx I_{ON,M}$, $I_{ON,M} = I_{OFF,M}$, and $I_{OFF,S} \approx 0$, the purity of s-SWCNTs can be related to average I_{ON}/I_{OFF} using the following equation:

$$\frac{1}{\frac{I_{ON}}{I_{OFF}}|_{avg}} = 1 - \frac{\text{Purity in \%}}{100} \quad (\text{for aligned arrays}) \quad (1)$$

Equation (1) suggests that transistors with aligned arrays of SWCNTs as the channel will have $I_{ON}/I_{OFF}|_{avg} = 3$ for a s-SWCNT purity of 66.67% (2/3), $I_{ON}/I_{OFF}|_{avg} = 10$ for a purity of 90%, $I_{ON}/I_{OFF}|_{avg} = 100$ for a purity of 99%, and so

on. In real applications, the purity must significantly exceed these estimated values to ensure that all the transistors have I_{ON}/I_{OFF} above a targeted level.

Aligned arrays of s-SWCNTs with high density and purity are also desirable for analog and RF electronics. These applications demand transistors with a wide range of L_{CH} .^[125] Moreover, high μ_{FE} and I_{ON}/I_{OFF} are necessary to ensure large current gain (short-circuit gain cut-off frequency, f_T) and power gain (maximum oscillation frequency, f_{max}).^[126,127] Note that if broadband performance (defined by f_T) is the only metric for a specific application, then materials such as a mixture of s- and m-SWCNTs as the channel of a transistor with device properties such as low I_{ON}/I_{OFF} and high μ_{FE} may perform adequately.^[126,128,129]

Applications such as flexible electronics and displays do not demand materials with high μ_{FE} ; therefore, amorphous silicon or organic semiconductors with $\mu_{FE} \approx 0.5\text{--}3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are often sufficient for these applications.^[130–132] Similarly, metal oxides (such as ZnO, indium-doped tin oxide (ITO), In_2O_3 , and SnO_2) used in transparent electronics are characterized by $\mu_{FE} \approx 10\text{--}50 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$,^[132] which is significantly lower than the value for crystalline silicon. Biosensors or chemical sensors use transistors as transducers, but parameters such as μ_{FE} and I_{ON}/I_{OFF} are not critical for their performance.^[133–135] Though the signal of a sensor does not depend on μ_{FE} , the signal-to-noise ratio does. These applications, therefore, have somewhat relaxed requirements on the purity, density, and alignment of s-SWCNTs within the channel.

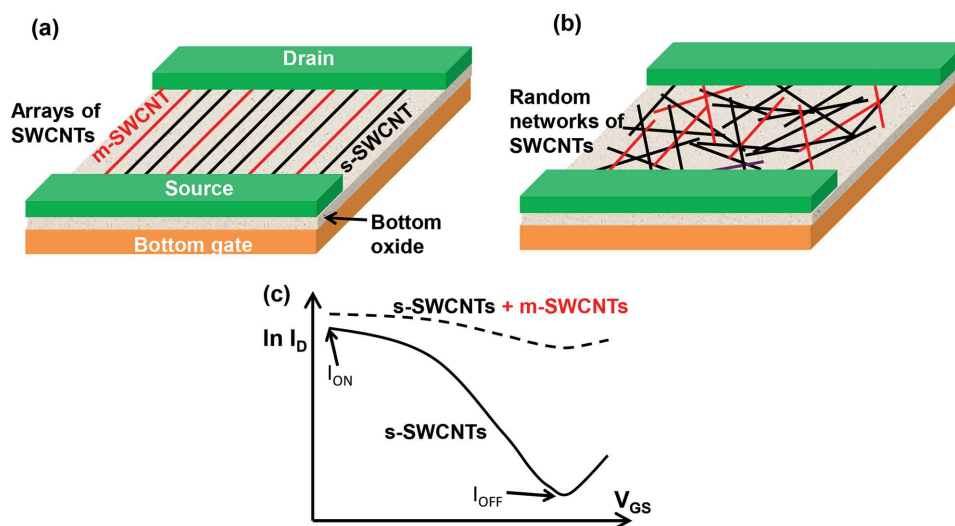


Figure 2. Schematic illustrations of bottom-gated transistors that use a) aligned arrays of SWCNTs and b) random networks of SWCNTs as the channel. c) Typical transfer characteristics (drain current I_D as a function of gate-to-source voltage V_{GS}) of a SWCNT-based transistor in semilog-y-scale. High modulation of I_D via V_{GS} is generally desired for such a transistor, which can be obtained using s-SWCNTs as the channel (solid line). The modulation of I_D is monitored using the ratio of on-current (I_{ON}) and off-current (I_{OFF}) marked in this figure as the maximum and minimum I_D in the characteristics. Presence of m-SWCNTs in the channel can reduce current modulation and hence the I_{ON}/I_{OFF} ratio (dashed line).

3. SWCNT Synthesis, the s-SWCNT Purity, and Electronic Properties

CVD is the most popular method to synthesize SWCNTs on planar substrates^[85,87–90,93,96,110,113,114,136,137] and it produces SWCNTs in a simpler, cost-effective, and cleaner (i.e., with fewer impurities) way compared to arc discharge^[138] and laser ablation.^[139] For a discussion on laser-ablation and arc-discharge methods, see refs. [85,87–90,96,136]. **Figure 3a** shows a schematic illustration of a CVD system for the synthesis of SWCNTs from hydrocarbons or alcohol, or carbon monoxide (CO) as the carbon feedstock, argon or helium as the carrier gas, and hydrogen as the reducing agent (which also prevents carbide formation).^[140,141] These gas mixtures react at temperatures ranging from 350–1200 °C to form SWCNTs on the substrate. Nanoparticles of metals, such as Fe, Co, Ni, and their compounds, act as nucleation sites or catalysts for

SWCNTs and play a crucial role in defining their type and size. In some cases, short s-SWCNT segments having a particular chiral index are also used as catalysts.^[97,142–144] These “cloning” approaches result in s-SWCNTs with the same chiral indexes as the seeds, although at densities that are insignificant for meaningful applications.

Metal catalysts are often formed using dewetting processes in nm-scale thin films of metals on insulating substrates (top row of Figure 3b).^[22,33,104,107,109,145,146] In other cases, preformed catalysts dispersed in solution can be deposited on a substrate (via drop-cast or spin-coating; bottom row of Figure 3b).^[34,108,145,147–149] Both strategies yield catalysts of different shapes and sizes (Figure 3c–d) after subsequent annealing at high temperature either in H₂ or Ar or He or ambient air, or in their mixtures. The diameter of the catalyst varies with the film preparation,^[79,150–152] the annealing conditions (duration, temperature),^[150,153–156] and the catalyst

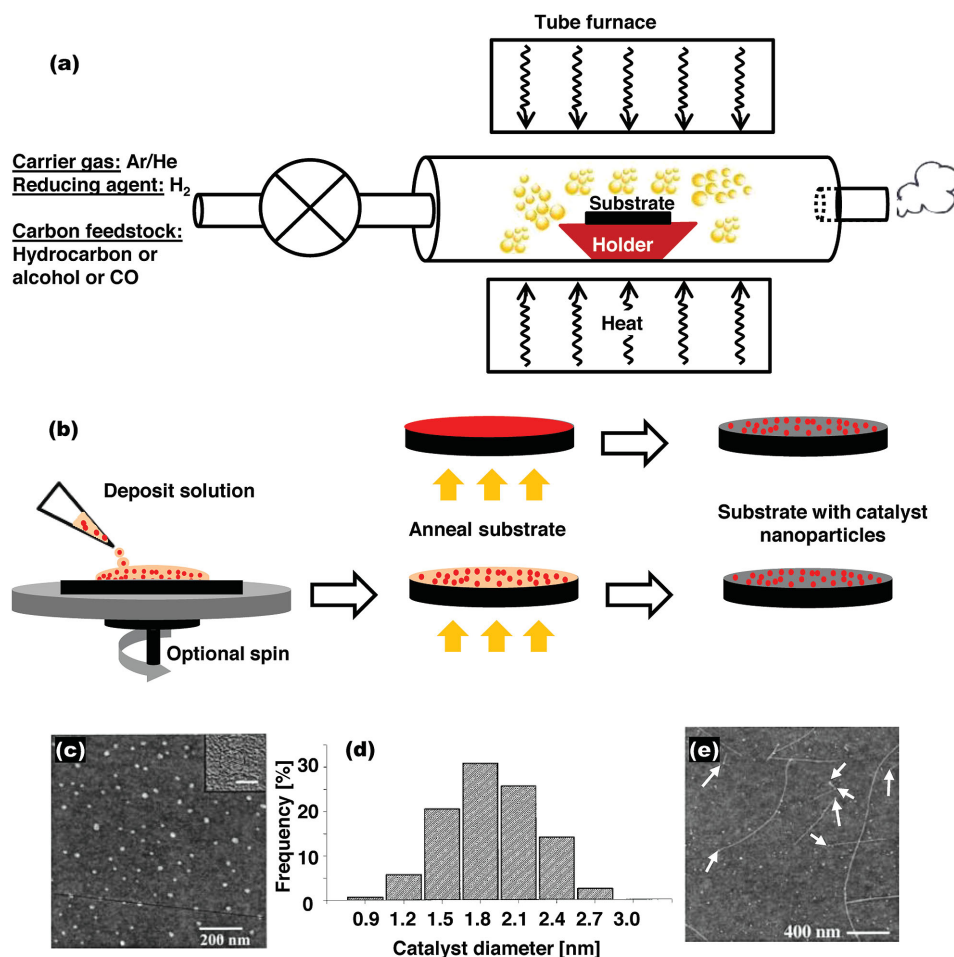


Figure 3. a) A schematic representation of the CVD process used to synthesize SWCNTs on a substrate by heating a mixture of carbon feedstock, H₂, and carrier gas (Ar, He) at high temperature inside a tube furnace. b) Schematic representation of the formation of nanoparticles as catalysts for SWCNT growth via thin-film metal deposition (top) and spin-coating or drop-casting (bottom). Thin-film deposition uses high-temperature annealing to form nanoparticles. Drop-casting method uses preformed nanoparticles in a solution (with or without spin-coating) to obtain a thin coating. Subsequent high-temperature annealing removes the solvent and leaves nanoparticles on the substrate. c) Atomic force microscopy (AFM) image of iron oxide nanoparticles obtained by drop-casting ferritin solution on SiO₂ and then annealing the solution in air at 800 °C. d) The diameter distribution of iron oxide nanoparticles imaged in Figure 3c. e) AFM imaging of SWCNTs grown from iron oxide catalysts of Figure 3c. The arrows point to the ends of SWCNTs that attach to nanoparticles. c–e) Reproduced with permission.^[151] Copyright 2001, American Chemical Society.

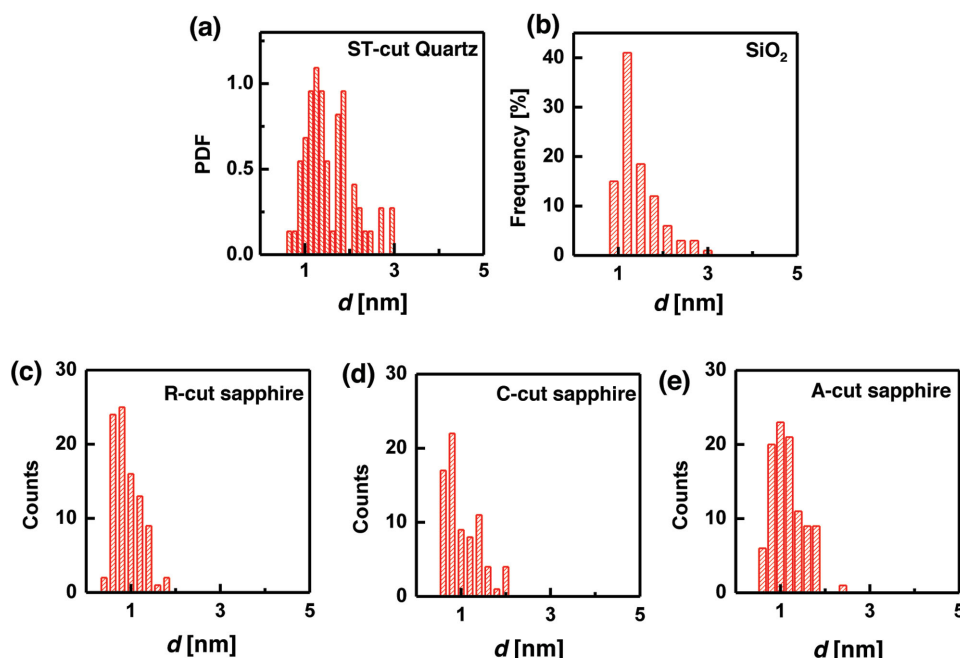


Figure 4. The diameter (d) distribution of SWCNTs grown a) on ST-cut quartz using Fe thin-film as catalyst and ethanol vapor as the carbon feedstock,^[79] b) on SiO₂ using drop-casted ferritin as catalyst and methane as the carbon feedstock,^[151] c) on R-cut, d) on C-cut, and e) on A-cut sapphire using Fe (obtained from thermal decomposition of Fe(CO)₅ in the presence of oleic acid) as catalyst and methane as the carbon feedstock.^[152] ST-cut quartz substrate have surfaces at a 42°45' angle with the Y-plane; R-, C-, and A-cut sapphire substrates have (1–102), (0001), and (11–20) surfaces, respectively. a) Reproduced with permission.^[79] Copyright 2012, AIP. b) Reproduced with permission.^[151] Copyright 2001, American Chemical Society. c–e) Reproduced with permission.^[152] Copyright 2005, Elsevier.

supports or substrates.^[153,154,157,158] After formation, catalysts exposed to a suitable flow of carbon feedstock diluted with H₂ and/or Ar yield SWCNTs. The catalytic efficiency is typically low, as many catalyst particles do not yield any SWCNT (see Figure 3d). An SWCNT attaches to a catalyst during growth. As a result, the size and shape of the catalyst dictate the diameter and influence the chiral index of the corresponding SWCNT.^[98,100,102,103,105,110,155,159,160] The chemical kinetics of SWCNT growth measured in situ^[161–165] can be analyzed either by atomistic computational approaches^[166–169] or by solving sets of first-order differential equations.^[165,170,171] These models capture different aspects of growth as a function of temperature, catalyst, gas pressure, and composition.

3.1. Properties of SWCNTs in Conventional High-Temperature CVD

3.1.1. CVD Growth of SWCNTs

Figure 4 shows the diameter (d) distribution of SWCNTs grown on amorphous (SiO₂) and crystalline (quartz, sapphire) substrates using Fe nanoparticles as catalyst at a temperature ≥ 900 °C.^[79,151,152] The distributions have minimum values in the range of 0.5–0.7 nm, set by the energetics^[172,173]

and the smallest size of the fullerene cap^[174] that initiate the growth. The range of the distribution, on the other hand, depends on the catalyst type, catalyst support, and growth conditions, as discussed later. Growth on amorphous substrates yields random networks of SWCNTs (Figure 5a), whereas growth on crystalline substrates such as quartz^[22,175] or sapphire^[176–178] yields aligned arrays of SWCNTs (Figure 5b). The crystal orientations^[146] or step-edges^[177,179] on the substrates lead to alignment, with the best alignment of >99.9% (measured using scanning electron microscopy) achieved with growth on stable temperature (ST)-cut quartz.^[22,180]

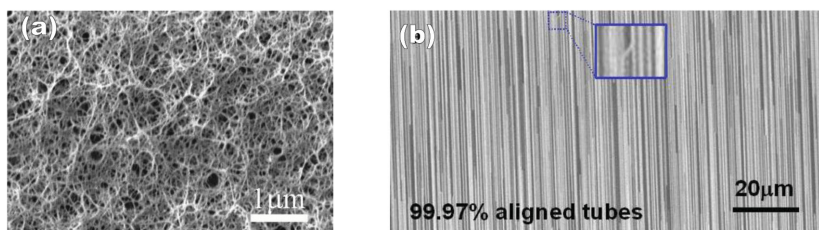


Figure 5. a) Scanning electron microscopy (SEM) image of networks of SWCNTs grown on SiO₂ using spin-coated Fe/Co-based solutions as the precursor to catalyst particles and ethanol vapor as the carbon feedstock. Reproduced with permission.^[181] Copyright 2006 Wiley-VCH. b) SEM image of horizontally-aligned SWCNTs grown on ST-cut quartz using a Fe thin-film as a precursor to catalyst particles and ethanol vapor as the carbon feedstock.^[22] The inset (inside the blue rectangle) shows a magnified area where a single SWCNT is misaligned. Reproduced with permission.^[22] Copyright 2007, Macmillan.

3.1.2. Electronic Characterization of Aligned Arrays of SWCNTs

Transistors can be fabricated in either top-, bottom-, or dual-gate configuration to measure the electronic properties of SWCNTs. Figure 6a shows a schematic illustration of a dual-gate transistor and Figure 6b shows an SEM image of a top-gated transistor (before dielectric and gate formation). Both approaches use aligned arrays of SWCNTs as the channel, Pd as source and drain contacts, and SiO₂ or high- κ (i.e., high dielectric constant) oxides as gate dielectrics. Use of Pd as source/drain contact allows hole injection into SWCNTs and typically yields p-type behavior for the transistor. Electron conduction in SWCNTs requires the use of Ca, Sc, or Er source/drain contacts,^[53–55] and/or electrostatic doping with high- κ oxides.^[25,56] Figure 6c plots

transfer characteristics (I_D as a function of V_{GS}) for top-gated aligned-array SWCNT transistors having different channel lengths (L_{CH}). The $I_{ON}/I_{OFF} \approx 2$ –5 (with $I_{ON}/I_{OFF} |_{avg} \approx 3$) for these transistors suggest the presence of 66.67% s-SWCNTs (with the rest m-SWCNTs), as per Equation (1). The transfer characteristics also allow extraction of charge transport parameters of s-SWCNTs such as μ_{FE} using the following equation:

$$\mu_{FE} = \frac{L_{CH}}{WC_G V_{DS}} \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{\max} \quad (2)$$

In Equation (2), W is the width of the transistor and C_G is the gate capacitance. As with the purity in Equation (1), this

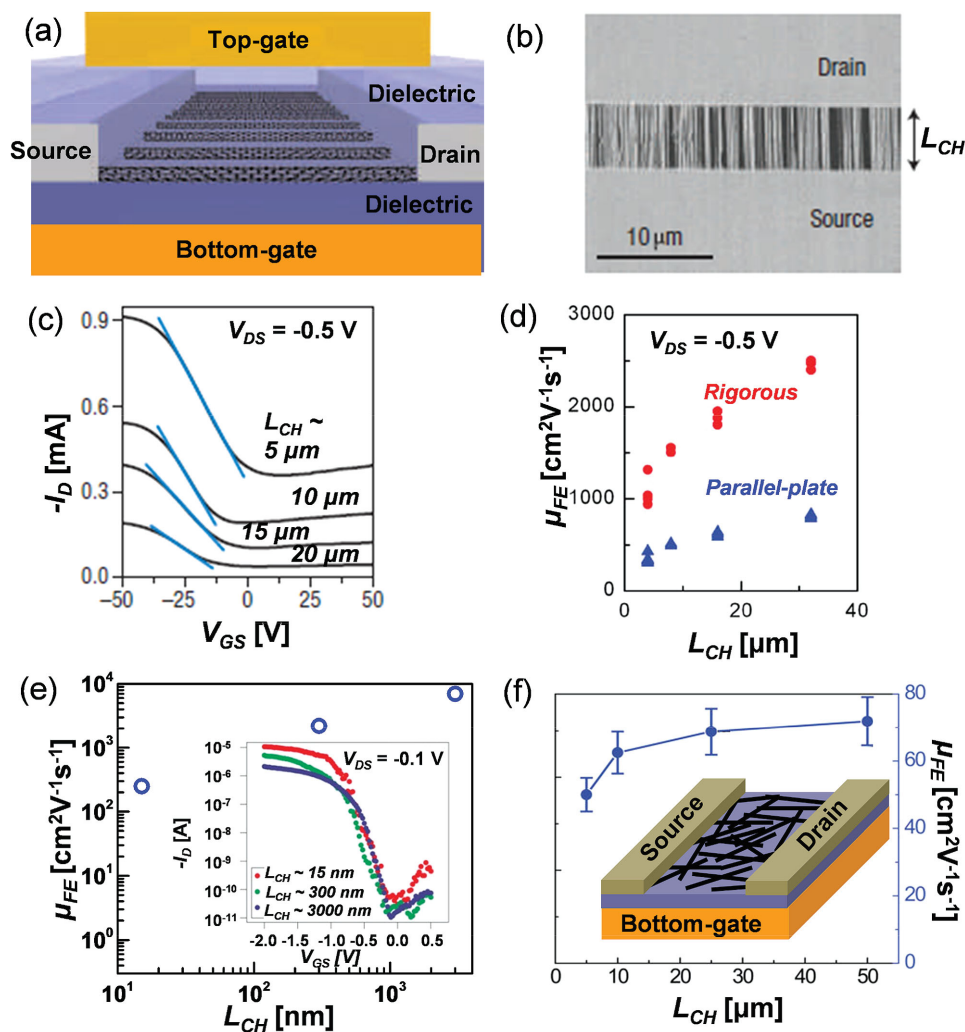


Figure 6. a) Schematic illustration of a dual-gated transistor that incorporates horizontally aligned arrays of SWCNTs as the channel. b) SEM image of the channel region of a top-gated transistor collected before the deposition of a gate dielectric (SU-8; thickness, $T_{GD} \approx 1.5 \mu\text{m}$) and a gate of Ti (1 nm)/Au (20 nm). The channel length (L_{CH}) for this device is $\approx 5 \mu\text{m}$. c) Transfer characteristics measured from four representative transistors with different L_{CH} and a fixed width, $W \approx 200 \mu\text{m}$. a–c) Reproduced with permission.^[22] Copyright 2007, Macmillan. d) Field-effect mobility (μ_{FE}) for transistors with different L_{CH} .^[22,85] Reproduced with permission.^[85] Copyright 2009, Wiley-VCH. Here, μ_{FE} is calculated using Equation (2), where $(\partial I_D / \partial V_{GS})|_{\max}$ is the maximum slope of the linear regions of the transfer curves (blue lines in panel (c)); blue triangles correspond to results that use a parallel-plate approximation for C_G ; red circles correspond to rigorous calculations of C_G .^[182] e) Plot of estimated μ_{FE} vs L_{CH} for nanoscale transistors; inset: transfer characteristics of the corresponding transistors used for μ_{FE} calculation. Inset: Reproduced with permission.^[24] Copyright 2010, Macmillan. f) Calculated μ_{FE} at different L_{CH} for transistors formed using random networks of SWCNTs as the channel.^[85] Reproduced with permission.^[85] Copyright 2009, Wiley-VCH.

approach to calculate μ_{FE} also presumes negligible current modulation for the m-SWCNTs. When C_G is calculated using a parallel-plate model (valid for transistors with thick gate dielectric and/or with high density of s-SWCNTs as the channel^[182]), μ_{FE} is $\approx 1000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $L_{CH} \approx 30 \text{ }\mu\text{m}$ (Figure 6d). A proper calculation of C_G accounts for s-SWCNT density and the associated fringing field effects^[22,182] and suggests $\mu_{FE} > 1000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $L_{CH} > 300 \text{ nm}$ (Figure 6d,e). Irrespective of the methods used to calculate C_G , the extracted μ_{FE} decreases with decreasing L_{CH} due to effects associated with parasitic contact resistances at the metal–s-SWCNT interfaces, which can dominate over the channel resistance at small L_{CH} .^[24,50,52,85]

3.1.3. Electronic Characterization of Randomly Oriented SWCNTs

Current–voltage measurements on transistors built using random networks of SWCNTs as the channel and with

rigorous calculation of C_G suggests $\mu_{FE} \approx 70 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for large L_{CH} (Figure 6 f)– a significantly lower value compared to that in transistors with aligned arrays of SWCNTs as the channel. The L_{CH} dependence of μ_{FE} in Figure 6f arises from the effects of parasitic resistances at the metal–s-SWCNT contacts, as discussed previously, and at the SWCNT–SWCNT junctions.^[183] Transistors with network SWCNTs also show an I_{ON}/I_{OFF} ratio that varies widely (contrary to a small variation in $I_{ON}/I_{OFF} \approx 2$ –5 for transistors with aligned arrays of SWCNTs) from 10^0 – 10^1 in transistors with high density ($>35 \text{ }\mu\text{m}^{-2}$) SWCNTs to 10^3 – 10^5 in transistors with low density SWCNTs.^[34,184,185] The lack of current percolation from source to drain through m-SWCNTs results in a high I_{ON}/I_{OFF} ratio in low density network transistors.^[184] Table 1 summarizes these electrical parameters, along with growth conditions and s-SWCNT purity, and compares them to values obtained with improved SWCNT synthesis methods discussed later.

Table 1. Summary of growth, s-SWCNT purity, and transistor parameters obtained using various growth strategies.

Growth process	Catalyst/Support	Carbon feedstock (Growth pure)	Growth temp. [°C]	s-SWCNT purity			Transistor parameters (having multiple SWCNTs)			Refs.
				Test method ^{a)}	Purity	Major chiralities	I_{ON}/I_{OFF}	μ_{FE} [$\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$]	Configuration	
Laser ablation	–	–	–	Electrical	$\approx 30\%$	–	–	–	–	[145]
Laser ablation	–	–	–	PL + AFM	$\approx 55\%$	–	–	–	–	[191]
HiPco	Fe(CO) ₅ /Gas phase	CO (1–10 atm)	1200	Electrical	≈ 61 – 63%	–	<5	0.5–1	Random network	[190,191]
CVD	Fe/Quartz	Ethanol (1 atm)	925	Raman	$\approx 64\%$	–	2–5	$\approx 2500^b$	Aligned array	[22]
CVD	Fe/SiO ₂	Ethanol (1 atm)	900–925	–	–	–	2–10	$\approx 70^b$	Random network	[60,85]
CW CVD	Co/MgO	CO (1 atm)	500	PL + ED + Raman	$\approx 90\%$	(6,5)	–	–	–	[102]
CVD	Co,Mn/silica	CO (5.8 atm)	600	PL + Raman	$\approx 93\%$	(6,5)	–	–	–	[98]
CVD (CoMoCAT)	Co,Mo/Silica	CO (5 atm)	750	PL + AFM	$\approx 92\%$	(6,5), (7,5)	–	–	–	[80,105]
CVD	Co/Silica	CO (6 atm)	800	–	–	(9,8)	10^1 – 10^5 ^{c)}	≈ 1	Random network	[100]
CVD (Commercial CoMoCAT)	Co,Mo/Silica	CO (1–10 atm)	850	PL + AFM	$\approx 52\%$	(7,6), (8,7), (6,6), (7,7)	≈ 3	$\approx 30^b$	Random network	[185,188] [189,191]
Low-P PECVD	Fe/SiO ₂	CH ₄ (0.5 Torr)	600	Electrical	$\approx 89\%$	–	–	–	–	[145]
Low-P PECVD	Fe/Al ₂ O ₃	C ₂ H ₂ (30 mTorr)	750	Raman	$\approx 96\%$	(7,5), (7,6), (8,4)	$\approx 10^2$ ^{c)}	≈ 10	Random network	[104]
CVD	Fe ₂ O ₃ /SiO ₂	CH ₄ (1 atm)	900	Electrical	$\approx 67\%$	–	–	–	–	[145]
CVD	Fe/Quartz	Ethanol (1 atm)	900	Electrical	$\approx 67\%$	–	1–10	$\approx 1500^b$	Aligned array	[107]
CVD	Fe/Quartz	IPA (1 atm)	900	Electrical	$\approx 87\%$	–	2–100	$\approx 1700^b$	Aligned array	[107]
CVD	Co/Quartz	IPA (1 atm)	800	Electrical	$\approx 85\%$	–	–	–	–	[109]
CVD	Co/Quartz	2-butanol (1 atm)	800	Electrical	$\approx 70\%$	–	–	–	–	[109]
CVD	Co/Quartz	CH ₄ (1 atm)	864	Electrical	$\approx 32\%$	–	–	–	–	[109]
CVD	Cu/Quartz	Ethanol + Methanol (1 atm)	900	I_{ON}/I_{OFF}	$\approx 95\%$	–	≈ 20	–	Aligned array	[108]

List of abbreviations: chemical vapor deposition (CVD), cold-wall CVD (CW CVD), plasma enhanced CVD (PECVD), photoluminescence (PL), electron diffraction (ED).

^{a)}The purity determination for the “electrical” method uses I_D – V_{GS} measurements on transistors having a few SWCNTs as the channel.^[145] The purity determination for the “ I_{ON}/I_{OFF} ” method uses Equation (1). ^{b)}These mobility numbers use rigorous C_G calculations that consider the density of s-SWCNTs.^[22,182] ^{c)}A high I_{ON}/I_{OFF} ratio can arise from the lack of percolation through m-SWCNTs in the channel, as expected for SWCNT density $< 35 \text{ }\mu\text{m}^{-2}$, $L_{CH}/W > 5$, and $W/L_{SWCNT} < 1.25$.^[184]

3.2. Properties of SWCNTs Grown Using Heterogeneous Catalysis

The I_{ON}/I_{OFF} ratio in transistors made with aligned arrays of SWCNTs or with high density random networks can be improved through the use of heterogeneous catalysis for SWCNT growth. Control in the composition, shape, and size of the metal catalysts available using heterogeneous catalysis enables the synthesis of improved purity of s-SWCNTs with a narrowed diameter distribution. In general, heterogeneous catalysis requires the use of active oxide supports such as silica (SiO_x), alumina (AlO_x), and magnesium oxide (MgO) that have a high porosity, surface area, and basicity.^[96,102,104,153,158,186–189] These properties ensure strong interactions with the catalyst and hence enhanced dispersion and stability of the catalyst during growth.

Among different metal catalysts used for selective growth of s-SWCNTs, Co forms catalysts with uniform size and shape on supports such as MgO ^[102,189] and silica.^[98,100,103,105,189] These Co catalysts yield SWCNTs with a few chiral indices and with s-SWCNT purity of $\geq 90\%$, when synthesized below a temperature threshold with a flow of CO as the carbon feedstock. (SWCNT synthesis with CO uses high pressure for conversion of CO to active carbon via the Boudouard reaction.^[190]) The temperature threshold to maintain the catalyst size/shape and hence the high purity in s-SWCNTs depends on the catalyst support. A MgO support interacts strongly with the catalyst, forms anchoring sites for the Co catalysts, and allows growth of (6,5)-SWCNTs at 500 °C using CO after calcination of the Co catalysts at 1000 °C.^[102] Figure 7a shows a chiral index map of SWCNTs obtained from electron diffraction analysis, which suggests semiconducting properties for 51 out of 57 SWCNTs. The tight diameter distribution (Figure 7b) and the dominance of the single chiral index (6,5) in the photoluminescence (PL) spectra (Figure 7c) and transmission electron microscopy confirm the high degree of control afforded by this approach. Silica supports, on the other hand, have low interaction with Co and, therefore, must be mixed with Mo to increase the stability of the catalyst. This Co/Mo mixture is reduced at 500 °C in a H_2 ambient and then used to synthesize high purity (CoMoCAT) s-SWCNTs at 750 °C with chiral indices (6,5) and (7,5).^[103,105,189] The dominance of these indices are confirmed using PL measurements (Figure 7d) and a s-SWCNT purity of $\approx 92\%$ is detected using PL and AFM topography of SWCNTs placed on mica slides.^[191] (In one case, Mn in the catalyst support stabilizes the size of Co catalysts during H_2 reduction at 700 °C and then growth at 600 °C; the process results in growth of (6,5) SWCNTs.^[98] In another case, a special type of porous silica (TUD-1) ensures the stability of Co catalysts without the use of Mo. After reduction at ≈ 500 °C and growth at 800 °C, these catalysts yield (9,8) SWCNTs.^[100]

An increase in the temperature beyond the values discussed above randomizes the catalyst size, favors formation of diverse range of SWCNTs, and results in SWCNTs with reduced s-SWCNT purity.^[98,100,103,105,110,159,160,188,191] Figure 7e plots similar trends for SWCNT growth, for which a Co catalyst on silica supports is stabilized at 600 °C in the presence of Mn, thereby resulting in the formation of $\approx 93\%$ s-SWCNTs. An increase

in growth temperature up to 800 °C reduces the s-SWCNT purity to $\approx 61\%$. Similar to Co, the Fe-based catalysts mostly used with silica or alumina supports yield $\approx 90\%$ s-SWCNTs at a lower growth temperature of $\approx 600\text{--}750$ °C.^[104,145] The s-SWCNT purity reduces towards the ideal $\approx 67\%$ (2/3) limit at a higher growth temperature and/or for a longer growth time.^[22,34,99,104,107,148,181]

Transistor characterization is generally difficult for SWCNTs formed from heterogeneous catalysis. A few studies use transistors with random networks of as-grown SWCNTs as the channel.^[100,104,185] Transistors made with dense SWCNTs (density $\approx 60 \mu\text{m}^{-2}$; unpurified, commercial-grade CoMoCAT SWCNTs; s-SWCNT purity $\approx 52\%$)^[191] show low I_{ON}/I_{OFF} ratios (≈ 3) and μ_{FE} values ($\approx 30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$),^[185] whereas transistors made with sparse SWCNTs (density $\leq 20 \mu\text{m}^{-2}$,^[100,104] s-SWCNT purity $\approx 96\%$)^[104] show high I_{ON}/I_{OFF} ratios ($\approx 10^1\text{--}10^5$).^[100,104,185] As percolation dictates the channel conduction for these networked SWCNT transistors,^[34,184,185] a systematic trend in the I_{ON}/I_{OFF} ratio with variation in s-SWCNT purity cannot be established from these studies. Fabrication of network transistors having channels with similar SWCNT densities, or alignment of SWCNTs in the channel area will be needed to understand the extent of s-SWCNT purity enabled by heterogeneous catalysis.

3.3. Properties of SWCNTs Grown Using Alcohol as the Carbon Feedstock

As discussed in the last section, carbon feedstocks such as hydrocarbons and CO cannot yield a high purity of s-SWCNTs at growth temperatures of 800–900 °C. Recent studies, however, suggest that s-SWCNT purity at these temperatures can be improved by using alcohol vapor as the feedstock. Alcohol vapor was primarily introduced to reduce the growth temperature (which was above 1000 °C at that time) relative to that needed for other carbon feedstocks and also to minimize the formation of amorphous carbon and soot.^[192] Subsequent studies suggested that high s-SWCNTs purity can result from growth either with alcohols having larger molecules such as isopropyl alcohol (IPA)^[107,109] and 2-butanol,^[109] or with a mixture of alcohols having smaller molecules such as an ethanol–methanol mixture. Use of IPA, in particular, can yield $\approx 87\%$ s-SWCNT even at ≈ 900 °C,^[107] as confirmed using electrical measurements on transistors built using individual, isolated SWCNTs where 33 out of 38 transistors exhibited $I_{ON}/I_{OFF} > 10$ (Figure 8). This purity is significantly higher than the $\approx 64\text{--}67\%$ s-SWCNTs and $I_{ON}/I_{OFF} \approx 2\text{--}5$ obtained using ethanol.^[22,34,60,107] Similar electrical measurements for SWCNTs, which are grown using 2-butanol and an ethanol–methanol mixture (Figure 9),^[108] show $\approx 70\text{--}95\%$ s-SWCNT purity. A mass spectroscopy analysis at the outlet of the CVD reactor suggests higher water to hydrocarbon ratios for the growth with IPA compared to ethanol, thereby clarified the origin of improved purity.^[107] In support of this observation, a controlled level of water exposure during growth induces selective etching of m-SWCNTs,^[147,149,193] thereby increasing the yield of s-SWCNTs. Additional details on this in situ water-assisted etching of m-SWCNTs appear in Section 4.4.

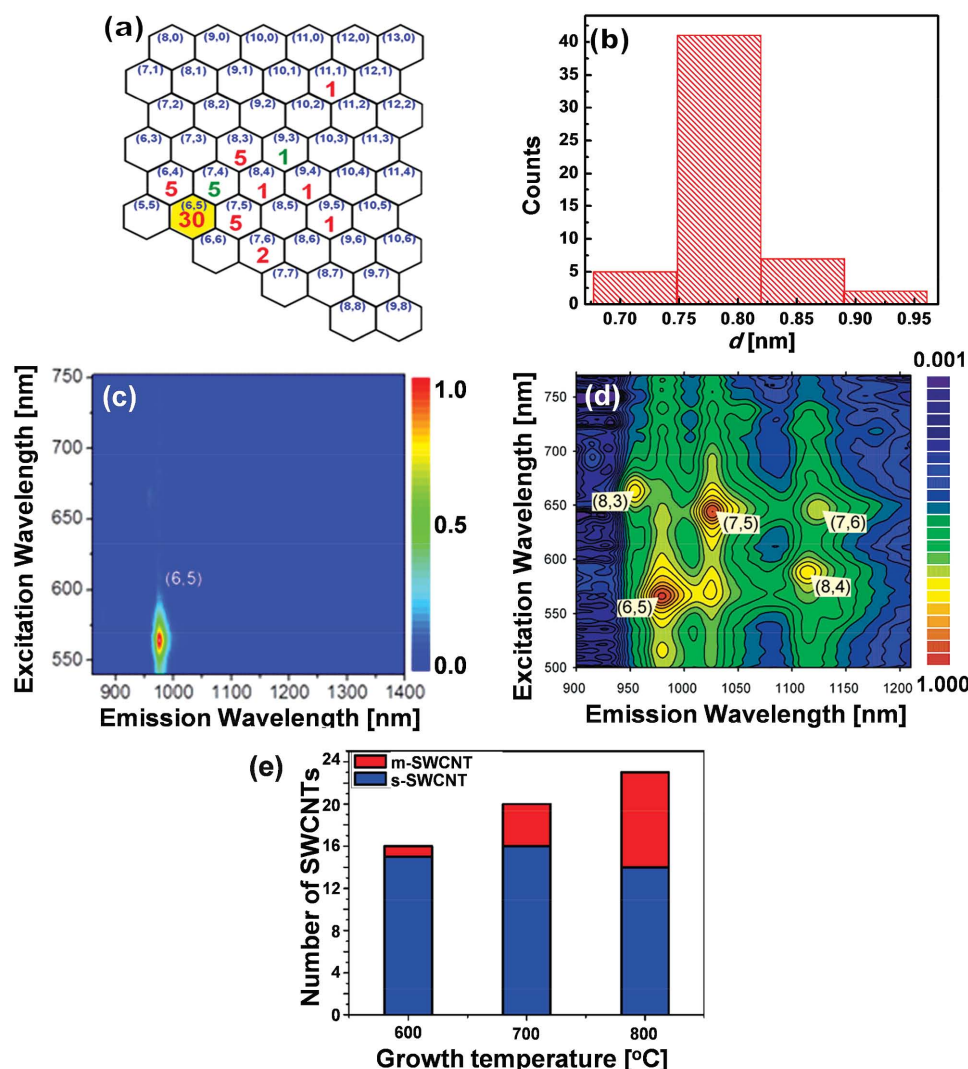


Figure 7. a) Chiral index map, b) distribution of d , and c) photoluminescence (PL) contour plot of SWCNTs grown using Co catalyst on porous MgO in a CVD process at 500 °C with CO as the carbon feedstock. a–c) Reproduced with permission.^[102] Copyright 2013, Macmillan. Figure 7a,b is obtained from electron diffraction analysis of 57 SWCNTs. In (a), the occurrence of SWCNTs with the chiral index (n, m) is labeled in its corresponding hexagonal cell (red for s-SWCNTs and green for m-SWCNTs). The PL contour plot in (c) shows a high chirality selectivity of (6, 5) s-SWCNTs. d) PL contour plot of CoMoCAT SWCNTs grown using Co catalysts stabilized with Mo on silica suggests dominant presence of (6,5) and (7,5) s-SWCNTs. The catalysts are annealed in H_2 ambient at 500 °C and then used to grow SWCNT at 750 °C, 5 atm using CO as the carbon feedstock. Reproduced with permission.^[105] Copyright 2003, American Chemical Society. e) Number of m- and s-SWCNTs grown at different temperatures using a Co catalyst stabilized with Mn on silica and CO (5.8 atm) as the carbon feedstock. The SWCNT types are identified using PL and Raman spectroscopy. Reproduced with permission.^[98] Copyright 2010, American Chemical Society.

3.4. Summary of s-SWCNT Growth Results

Studies of heterogeneous catalysis for SWCNT growth across a wide range of catalyst supports, metal catalysts, temperatures, pressures, and carbon feedstocks have identified conditions for growing $\approx 90\%$ s-SWCNTs. Table 1 summarizes the growth conditions and electrical parameters for several of the best results. Figure 9 plots s-SWCNT purity as a function of growth temperature for a wide range of growth conditions. These results suggest that growth below 800 °C with hydrocarbon and CO as the carbon feedstock yields SWCNTs with semiconducting purity that exceed the 66.67% (2/3) value expected for a random growth process. One direction that emerged from these studies

is the synthesis of SWCNTs at minimum temperatures (350 °C is the lowest reported SWCNT growth temperature)^[194] by use of plasmas to decompose the feedstock^[104,145,194,195] and without the high temperature annealing steps generally used to prepare the catalysts. High temperature annealing and growth reduce control over heterogeneous catalysis and lead to SWCNTs with mixed purities and wide diameter distributions. Use of alcohol as the carbon feedstock, however, enables good s-SWCNT purity even at temperatures of 800–900 °C possibly due to the role of OH radicals from the alcohol decomposition in the removal of m-SWCNTs and small diameter s-SWCNTs.^[107,108] The process, therefore, is expected to have low catalytic efficiency and also may lead to substrates with large diameter s-SWCNTs (as for

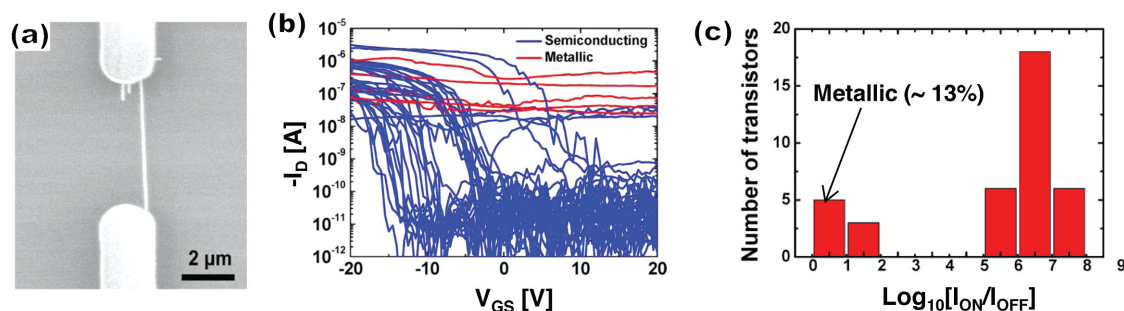


Figure 8. a) SEM image of a transistor with a single SWCNT (grown on quartz in a standard CVD at 900 °C using Fe as catalyst and isopropyl alcohol vapor as the carbon feedstock) bridging source and drain contacts. b) Transfer characteristics of 38 of such transistors; the red traces represent those with a single m-SWCNT; the blue traces represent those with a single s-SWCNT. c) Distribution of $I_{\text{ON}}/I_{\text{OFF}}$ among the 38 transistors of (b) showing that 33 of them ($\approx 87\%$) have $I_{\text{ON}}/I_{\text{OFF}} > 10$ and $\approx 80\%$ have $I_{\text{ON}}/I_{\text{OFF}} > 100$. Reproduced with permission.^[107] Copyright 2012, American Chemical Society.

the growth with water vapor,^[149] discussed later) undesirable for transistor applications due to their low bandgaps. Additional exploration of the vast parameter space for heterogeneous catalysis either via Edisonian or computer-controlled^[196] approaches and an improved understanding of the relevant processes (at the atomic level and then scaled up to transistors) from an experimental and computational point of view will be essential to determine optimum conditions for reliable and reproducible synthesis of s-SWCNTs.

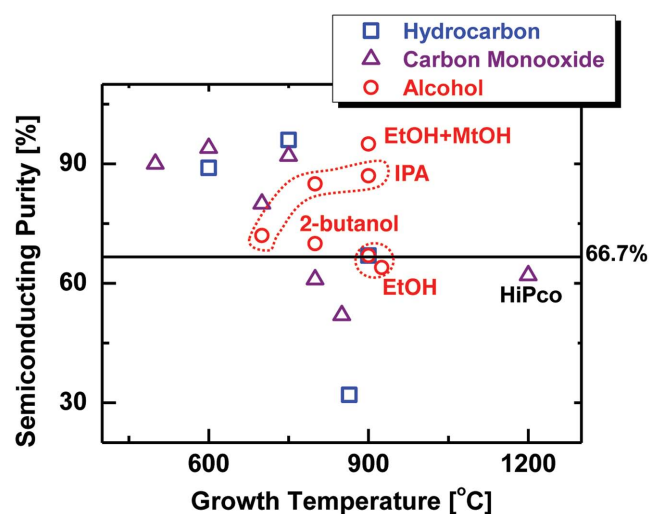


Figure 9. Semiconducting (or s-SWCNT) purity in SWCNTs synthesized using a wide range of CVD conditions at different temperatures and carbon feedstock. The growth conditions for each of these methods appear in Table 1. The theoretically expected purity of $\approx 66.67\%$ is also indicated by the horizontal line. SWCNTs formed with hydrocarbons as the carbon feedstock use data from plasma enhanced CVD (PECVD) growth at 600 °C using CH_4 ^[145] and at 750 °C using C_2H_2 ,^[104] regular CVD growth at 864 °C using CH_4 ^[109] and at 900 °C using CH_4 .^[148] SWCNTs formed with carbon monoxide as the carbon feedstock use data from cold-wall CVD growth at 500 °C^[102] and regular CVD growth at 600 °C, 700 °C, 800 °C,^[98] 750 °C,^[105,191] 850 °C,^[188,189,191] and 1200 °C.^[145,190,191] SWCNTs grown with alcohols as the carbon feedstock use data for ethanol and methanol mixture (EtOH+MeOH) at 900 °C,^[108] IPA at 700–900 °C,^[109] and 900 °C,^[107] 2-butanol at 800 °C,^[109] and EtOH at 900 °C,^[107] and 925 °C.^[22]

4. Ex Situ Methods for Enhancing the Purity of s-SWCNTs

As none of the in situ techniques produce nanotubes with electronic-grade s-SWCNT purity of $>99.99\%$, various post-processing methods have been proposed to improve s-SWCNT purity in ensembles of SWCNTs and hence to increase $I_{\text{ON}}/I_{\text{OFF}}$ ratios in transistors made with them. These methods either separate m-SWCNTs in solution and then disperse the remaining s-SWCNTs on substrates (solution-based purity enhancement) or chemically remove and modify the m-SWCNTs grown on substrates as a mixture (substrate-based purity enhancement). Among the solution-based methods reviewed in ref. [87], those based on density-gradient ultracentrifugation^[197] are most commonly used for transistor applications that require high $I_{\text{ON}}/I_{\text{OFF}}$ ratios. The substrate-based methods, on the other hand, remove and modify m-SWCNTs (locally or along its length) by heating them optically or electrically or by selective chemical reaction. For transistors with network SWCNTs, instead of selective removal of m-SWCNTs, a general removal of SWCNTs in patterned areas within the channel can also increase the $I_{\text{ON}}/I_{\text{OFF}}$ ratio. The processing details for each of these methods and the electronic properties of the remaining s-SWCNTs are reviewed below.

4.1. Solution-Based s-SWCNT Sorting

Selective chemical functionalization of SWCNTs based on their electronic type and diameter has inspired the development of solution-based SWCNT sorting techniques.^[87,112,198,199] The s-SWCNTs can be self-sorted as random networks on dielectric surfaces treated with (3-Aminopropyl)triethoxysilane (APTES),^[200] which show selective absorption towards s-SWCNTs.^[200,201] Transistors fabricated with these network s-SWCNTs have $I_{\text{ON}}/I_{\text{OFF}} \approx 10^0\text{--}10^6$ ($\approx 95\%$ of the devices have $I_{\text{ON}}/I_{\text{OFF}} > 10^2$) and $\mu_{\text{FE}} \approx 0.5\text{--}6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[200] Among other methods, non-covalent functionalization of SWCNTs in solution and subsequent placement under the influence of an electric field,^[202,203] in a chromatography column,^[204–213] or a centrifuge,^[197,198,214–222] enable the separation of different types of SWCNTs. The electric field based approach to SWCNT sorting uses a variable frequency AC electric field to separate

m-SWCNTs in solution.^[202,203] The high dielectric constants of the m-SWCNTs compared to that of the solvent, which either can be sodium dodecyl sulfate (SDS) or sodium dodecylbenzene sulfonate (SDBS), ensure a positive dielectrophoretic force for the m-SWCNTs and align them between the electrodes used to apply the electric field. The s-SWCNTs, along with some m-SWCNTs, remain in solution with unknown purity. Many attempts have been made to improve the s-SWCNT purity using dielectrophoretic sorting.^[87,111] However, none has resulted in transistor demonstrations. (In spite of its ineffectiveness in SWCNT sorting, dielectrophoresis is routinely used to align sorted s-SWCNTs from solution placed in between two electrodes.^[223–225]) In the following, we discuss the chromatography- (Section 4.1.1) and centrifugation-(Section 4.1.2) based SWCNT sorting techniques. The transistor results using sorted SWCNTs obtained from these two methods are discussed separately in Section 4.1.3.

4.1.1. Chromatography

Two types of chromatography techniques have been used to sort SWCNTs. In ion-exchange chromatography (IEX), SWCNTs mixed in a DNA solution are injected into an exchange column containing anions that are thought to bind to the negatively charged phosphate groups of DNA.^[207,208] The m-SWCNTs have carriers near the Fermi level and are easily polarized by these same phosphate groups. DNA-wrapped m-SWCNTs, therefore, have no net charge and only weakly interact with the anions in the exchange column. They exit the column with the flow of a low concentration NaSCN solution. By comparison, s-SWCNTs are difficult to polarize and hence, DNA-wrapped s-SWCNTs have an effective negative charge, enhanced attraction to the anions, and require a higher NaSCN concentration for their extraction from the column. Recent advances in the IEX technique with optimizations of the DNA construct and the choice of anion yield SWCNT solutions with 60–90% purity and specific chiral angles.^[210] The implication of these purity improvements in transistor parameters is yet to be studied.

In gel chromatography, SWCNTs dispersed in aqueous solutions of SDS pass either through a single column^[204–206,212,213] or through a series of columns^[211] containing allyl dextran-based size-exclusion gel that interacts specifically with s-SWCNTs based on their diameter d .^[211] As illustrated in **Figure 10a,b**, the single column version inserts the m- and s-SWCNTs into the column and can only achieve SWCNT-type selectivity with up to 99.9% s-SWCNTs after three iterations^[213] using a continuous flow of SDS (and sometimes sodium cholate (SC))^[212]. The m-SWCNTs are first eluted from the column, as they have less interaction with the gel, followed by the s-SWCNTs. The multi-column version, on the other hand, can achieve diameter-selectivity for the s-SWCNTs in addition to type-selectivity. The s-SWCNTs with smaller d have higher interaction with the gel and are collected in the upper column, while those with gradually increasing d are collected downstream in the subsequent columns. The solution collected from the bottom-most column contains all m-SWCNTs and some s-SWCNTs (with $d > 1.4$ nm) that show no interaction with the gel, presumably because of complete SDS coatings.

4.1.2. Ultracentrifugation

The basic technique was pioneered by Svedberg in the 1920s and is now widely used in biology and life science.^[227] In the past decade, ultracentrifugation has also been studied for sorting s-SWCNTs.^[198,214–222,228] The choice of polymers such as poly(9,9-dioctylfluorene) (PFO) and its compounds, poly(9,9-dioctylfluorene-*alt*-(1,4-benzo-2,10,3-thiadiazole) (F8BT), regioregular poly(3-alkylthiophene) (rr-P3AT), regioregular poly(3-dodecylthiophene) (rr-P3DDT), poly(dithiafulvalene-fluorene-*co-m*-thiophene) (pDTGG-mT), etc. are critical for dispersion of the s-SWCNTs in a manner that allows them to appear selectively as supernatant after ultracentrifugation. Raman analysis (radial breathing modes, RBMs) confirms enrichment of s-SWCNTs in the supernatant (**Figure 10c,d**).

In comparison with classical ultracentrifugation techniques, sorting of s- and m-SWCNTs is possible using density-gradient ultracentrifugation (DGU)^[197] to yield s-SWCNT purity of up to $\approx 99.9\%$.^[229] This technique disperses as-grown SWCNTs, obtained from CoMoCAT^[188,230] or laser ablation^[139] processes that synthesize SWCNTs with a few chiral indices, in solutions containing surfactants such as SC, SDS, or their combinations. The dispersion unbundles the SWCNTs and encapsulates them with surfactants. The dispersed SWCNTs are remixed with iodixanol and inserted at an isopycnic region (region with same density) using a syringe needle inside a density gradient made with layers of iodixanol and SC mixtures at different concentrations (**Figure 10e**). After ultracentrifugation, the surfactant-wrapped SWCNTs populate different regions of the centrifuge tube according to their buoyant density. SWCNTs with smaller d , having a lower density, populate the upper part of the tube, while larger diameter SWCNTs and their bundles with higher density populate the lower part (**Figure 10f**). With a suitable choice of starting SWCNT (CoMoCAT) and surfactants (a mixture of SC and SDS), it is possible to extract s- and m-SWCNTs from different regions of the centrifuge tube (**Figure 10g**). The s-SWCNT purity after DGU varies from 90% to 99.9% depending on the number of successive iterations.^[197,229]

4.1.3. Transistor Properties: Solution-Based Sorting

Gel Chromatography: Transistors containing high density, short ($\approx \mu\text{m}$) aligned s-SWCNTs (purity $\approx 99\%$ after column chromatography) as the channel exhibit higher $I_{\text{ON}}/I_{\text{OFF}}$ ratios for larger L_{CH}/W ratios (**Figure 11a,b**),^[27] consistent with the percolation theory.^[27,34,184] For $L_{\text{CH}} \approx 100$ nm, only a few devices (10–20%) yield $I_{\text{ON}}/I_{\text{OFF}} > 10^2$, as trace amounts of short, aligned m-SWCNTs (with purity $\approx 1\%$) bridge the source and drain contacts. This observation confirms the need for $>99.99\%$ purity for high-performance electronics with $L_{\text{CH}} \ll 100$ nm. The extracted values of $\mu_{\text{FE}} \approx 16\text{--}27$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ for these transistors (**Figure 11b**) suggest a small increase with decreasing L_{CH} , as more s-SWCNTs directly bridge the source and drain contacts. These values of μ_{FE} are comparable to those obtained for transistors with pristine SWCNT networks (**Figure 6 f**); however, the variation in the degree of alignment of the SWCNTs (i.e., higher alignment for transistors in

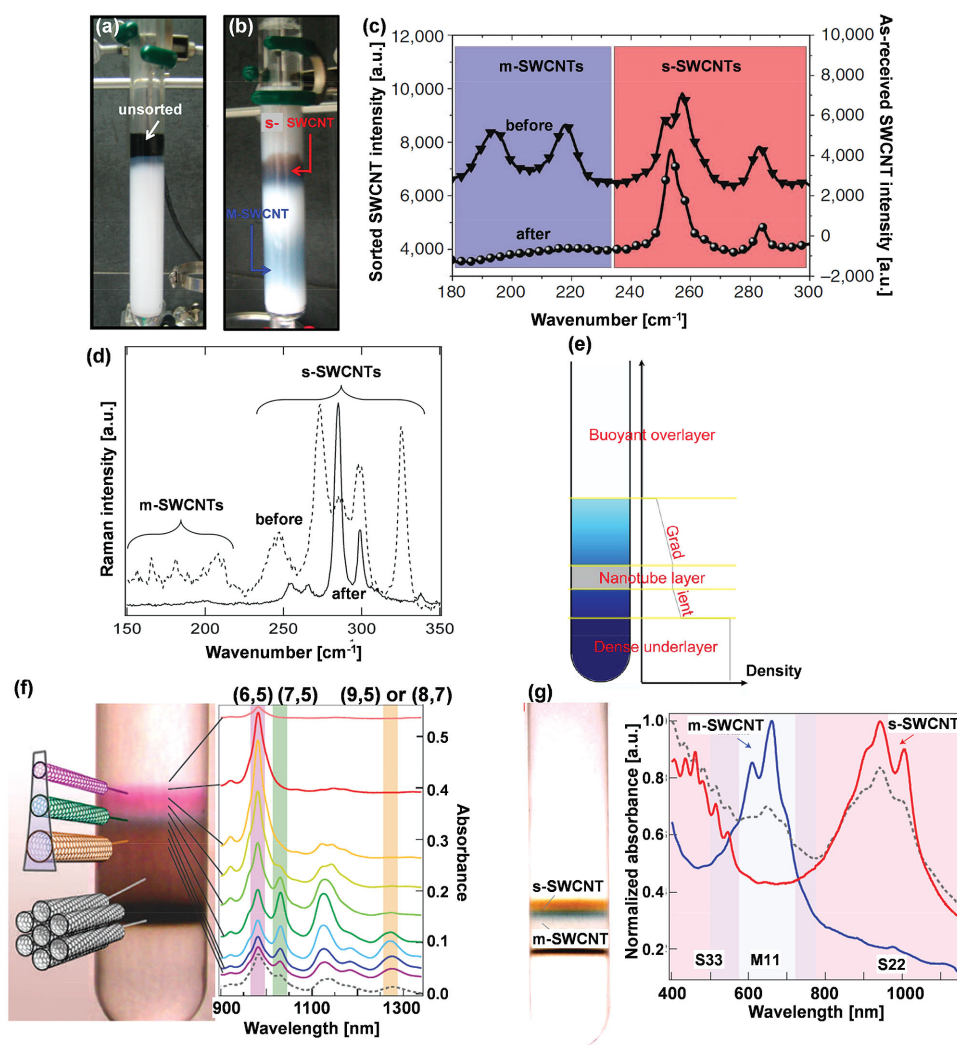


Figure 10. Optical images of a column a) before and b) after gel chromatography using a continuous flow of aqueous 1% SDS solution. The s-SWCNTs move slowly in the column compared to the m-SWCNTs. After certain durations of SDS flow, two distinct bands appear at the top and bottom of the column in (b) that correspond to s- and m-SWCNTs, respectively. a, b) Reproduced with permission.^[213] Copyright 2013, American Chemical Society. Radial breathing mode (RBM) Raman spectra taken using 633 nm excitation before (as-received) and after (supernatant) SWCNT sorting via ultracentrifugation with c) rr-P3DDT and d) a PFO-compound^[198,226] as the solvent. The spectrum obtained for the supernatant has no m-SWCNT signals. c) Reproduced with permission.^[216] Copyright 2011, Macmillan. d) Reproduced with permission.^[198] Copyright 2014, American Chemical Society. e) Schematic illustration of SWCNT placement before density-gradient ultracentrifugation (DGU). A linear gradient of iodixanol is formed in between a dense underlayer and a buoyant overlayer. SWCNTs dispersed in surfactant solution are inserted inside the gradient at an isopycnic region. f) Optical image of SC-encapsulated CoMoCAT SWCNTs after DGU shows colored bands along the gradient. Nanotube bundles, aggregates, and insoluble material sediment form the lower part of the gradient, while SWCNTs of different d form the upper part of the gradient. The absorbance spectra on the right indicate SWCNTs with increasing d , having smaller bandgap and higher wavelength of absorption, are more concentrated at larger densities near the bottom of the gradient. SWCNTs with chiral indices (6,5), (7,5), and (9,5)/(8,7) are concentrated at different regions of the gradient. g) Optical image of laser ablation grown SWCNTs separated in a co-surfactant solution (1:4 SDS/SC). The top (orange) and bottom (green) band correspond to regions of highly enriched s-SWCNTs and m-SWCNTs, respectively. The absorbance spectra for these two bands are shown on the right. M11, S22, and S33 correspond to first-order metallic, second-, and third-order semiconducting optical transitions (see Figure 21). e–g) Reproduced with permission.^[197] Copyright 2006, Macmillan.

Figure 11b compared to those in Figure 6f) prevent quantitative conclusions.

Transistors containing single s-SWCNT as the channel with $L_{CH} \approx 100$ nm using SWCNTs obtained from single-column multiple-cycle gel chromatography exhibit $\mu_{FE} \approx 20$ cm² V⁻¹ s⁻¹ (average values, with a maximum of ≈ 80 cm² V⁻¹ s⁻¹).^[213] Similar measurements on different sets of transistors with $L_{CH} \approx 200$ nm yield $\mu_{FE} \approx 40$ –150 cm² V⁻¹ s⁻¹.^[231] In

comparison, transistors that use pristine, as-grown s-SWCNTs and similar L_{CH} exhibit significantly higher μ_{FE} (Figure 6e), thereby suggesting the potential for improving such solution-based approaches.

Ultracentrifugation: Transistors made with s-SWCNTs purified by ultracentrifugation with purity ≈ 94 –99% and then deposited in random networks as the channel exhibit a range of $I_{ON}/I_{OFF} \approx 10^1$ – 10^5 (Figure 11c,d), depending on the purity,

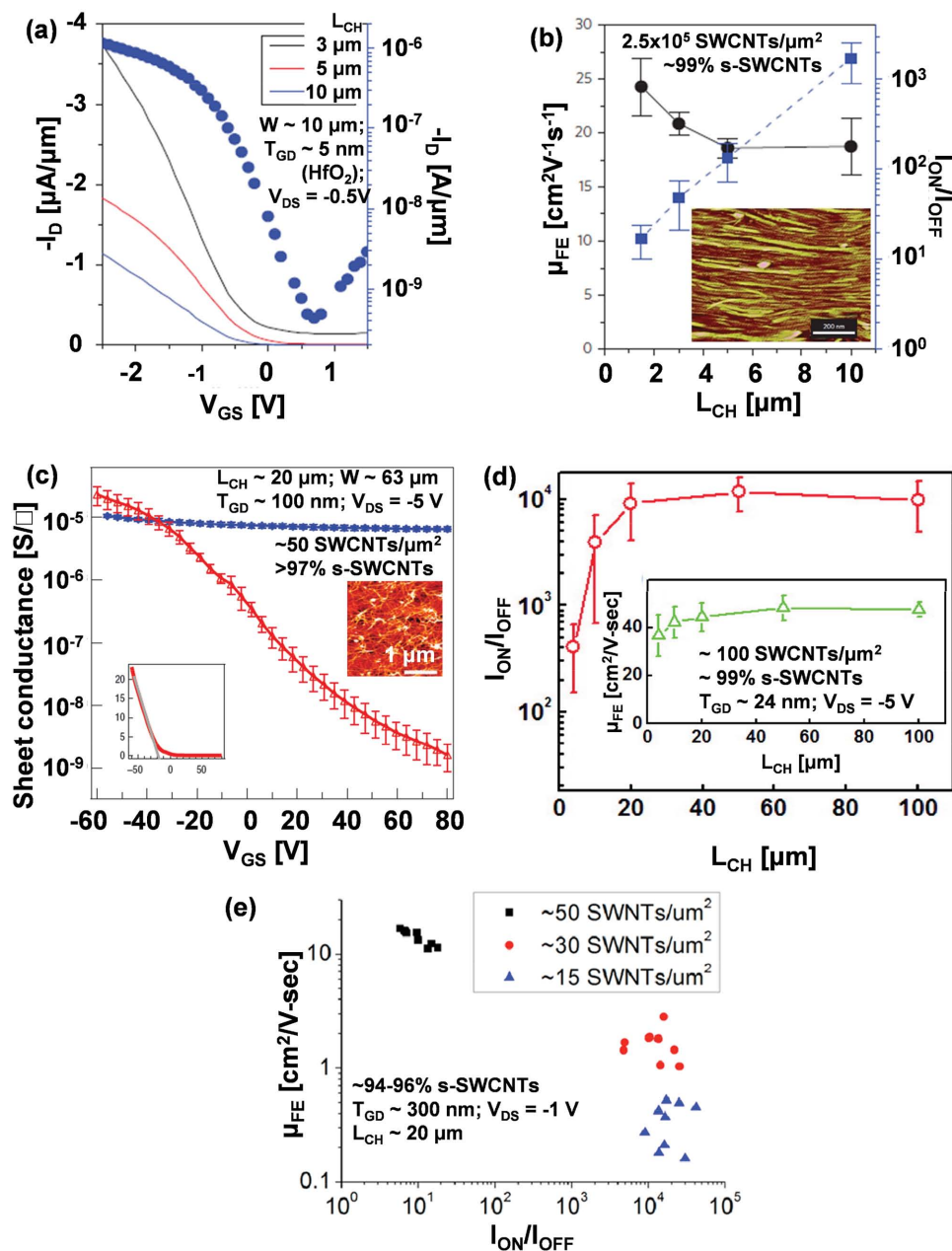


Figure 11. a) Transfer characteristics and b) calculated μ_{FE} and I_{ON}/I_{OFF} ratios for transistors with a high density of chromatography-sorted, short-length ($\approx \mu\text{m}$) aligned SWCNTs as the channel. The inset of (b) shows AFM image of the channel area. In (a), the transfer characteristics are plotted in a linear scale (left axis) for different L_{CH} and in a logarithmic scale (right axis, blue dots) for $L_{CH} = 10$ μm . a,b) Reproduced with permission.^[27] Copyright 2013, Macmillan. c) Sheet conductance vs V_{GS} characteristics of two transistors fabricated using networks of DGU-sorted s-SWCNT (red) and m-SWCNT (blue) as the channel. Insets show s-SWCNT characteristics in linear scale (bottom-left) and an representative AFM image of the SWCNT network used as the channel for transistors (top-right). The maximum slope of the linear scale plot allows calculation of $\mu_{FE} \approx 20$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. Reproduced with permission.^[197] Copyright 2006, Macmillan. d) The variation in the I_{ON}/I_{OFF} ratio and μ_{FE} (inset) with L_{CH} for transistors made using DGU-sorted s-SWCNTs as the channel. Reproduced with permission.^[32] Copyright 2012, American Chemical Society. e) Calculated μ_{FE} and I_{ON}/I_{OFF} for transistors that use pDFFF-mT sorted SWCNT networks as the channel. Increase in SWCNT densities (with ≈ 94 – 96% s-SWCNTs) increases μ_{FE} , but reduces the I_{ON}/I_{OFF} ratio. Reproduced with permission.^[222] Copyright 2013, American Chemical Society.

density, alignment, and length of the sorted s-SWCNTs and the device dimensions.^[32,126,197,216,217,220,222,223] Following the percolation theory,^[34,184] these transistors show higher I_{ON}/I_{OFF} ratios for larger purities and L_{CH}/W ratios, and for smaller densities and W/L_{SWCNT} ratios, where L_{SWCNT} is the average length of

SWCNTs. The extracted values of μ_{FE} for the sorted s-SWCNTs ranges from 1–50 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ in transistors with $L_{CH} \approx 1$ –100 μm (Figure 11d,e),^[81,216,217,220,222,223,228,232] even after SWCNT alignment using dielectrophoresis^[223] and self-assembly.^[228] Though consideration of contact effects suggests intrinsic mobilities of

$\approx 200\text{--}300\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ for any L_{CH} ,^[81] these values are significantly lower than μ_{FE} of $>1000\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ obtained in transistors with pristine SWCNTs as the channel (Figure 6d,e).

Improvements in mobility and s-SWCNT purity remain the key focus for electronic applications of solution-based sorting methods. The presence of residual surfactants and defects,^[81,116] high resistance tube-tube junctions,^[27,34] and short SWCNT lengths^[27,233] are presumed origins for low intrinsic mobilities in solution-sorted s-SWCNTs. Additional contributions from contact resistances will also require consideration.

4.2. Electrical Breakdown of m-SWCNTs

The first demonstration of substrate-based m-SWCNT removal employed selective electrical breakdown of m-SWCNTs using transistors with multiple SWCNTs as the channel.^[115] During this process, the s-SWCNTs in a p-type transistor (that allows hole conduction) are electrostatically turned-off using positive V_{GS} in a bottom-gated device geometry. An application of high V_{DS} then induces Joule heating selectively in the m-SWCNTs and raises their temperatures significantly.^[234–240] Once the temperature reaches T_{BD} (breakdown temperature) $\approx 600\text{ }^{\circ}\text{C}$, the m-SWCNTs are oxidized and are broken down near the center of the channel.^[117,235,241] Heat dissipation into the contacts limits the temperature near source and drain^[235,242] and does not allow breakdown in those regions. The application of electrical breakdown on transistors with both m- and s-SWCNTs (Figure 12a) increases the $I_{\text{ON}}/I_{\text{OFF}}$ ratio from $\approx 10^1$ to $>10^3$ (Figure 12b,c).

Electrical breakdown cannot selectively remove m-SWCNTs in transistors with random networks of SWCNTs. For these transistors, heat conduction within neighboring SWCNTs raises their temperature and causes correlated breakdown of a set of m- and s-SWCNTs across the width of the transistor.^[243] The process, however, is effective for transistors with aligned arrays of SWCNTs. For these transistors, electrical breakdown at a gradually increasing V_{DS} causes corresponding increases in $I_{\text{ON}}/I_{\text{OFF}}$ (Figure 13a), as the m-SWCNTs with higher conductivities are broken first followed gradually by the ones with lower conductivities.^[83] For these transistors (and also for transistors with a single m-SWCNT), the voltage V_{BD} required to induce breakdown varies linearly with L_{CH} for $L_{\text{CH}} > 1\text{ }\mu\text{m}$.^[117,234,236] In this regime, $V_{\text{BD}} = g(T_{\text{BD}} - T_0)L_{\text{CH}}/I_{\text{BD}}$ (Figure 13b), where I_{BD} is the breakdown current for a single m-SWCNT ($\approx 20\text{ }\mu\text{A}$ ^[244]), g is the thermal coupling coefficient for the m-SWCNT/dielectric interface and $T_0 = 300\text{ K}$.^[236] For $L_{\text{CH}} < 1\text{ }\mu\text{m}$, the “hot-phonon” effect reduces the current in the m-SWCNTs and increases V_{BD} above the linear asymptote,^[236] as observed in the measured V_{BD} vs. L_{CH} for transistors with different gate dielectrics (Figure 13b,c).^[117,234,236] Like V_{BD} , the

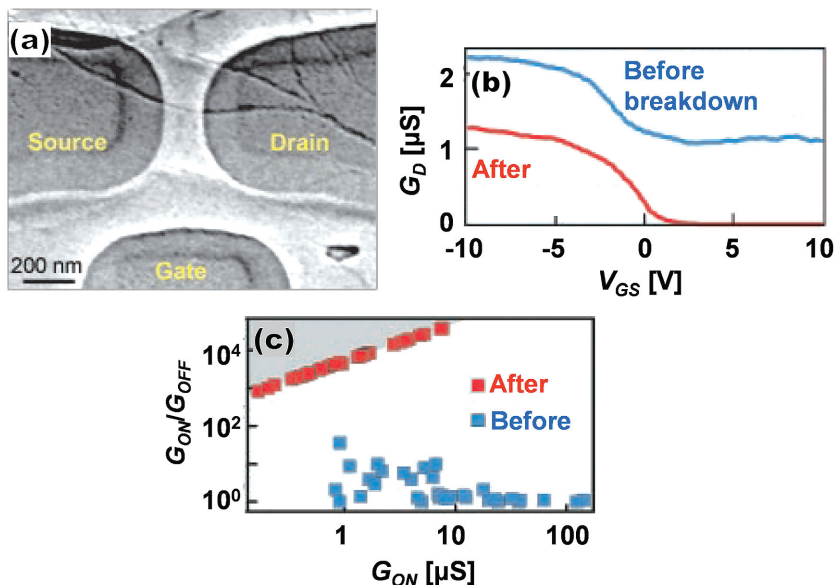


Figure 12. a) SEM image of a transistor, in which a few SWCNTs bridge source and drain contacts. b) Conductance ($G_{\text{D}} \equiv \partial I_{\text{D}}/\partial V_{\text{DS}}$) modulation as a function of V_{GS} in a transistor like the one in (a) before and after removal of m-SWCNTs from the channel using electrical breakdown. c) Plot of $G_{\text{ON}}/G_{\text{OFF}}$ vs G_{ON} before and after electrical breakdown for a set of transistors. Here, $G_{\text{ON}} \equiv G_{\text{D}}@V_{\text{GS}} = -10\text{ V}$ and $G_{\text{OFF}} \equiv G_{\text{D}}@V_{\text{GS}} = 10\text{ V}$. Reproduced with permission.^[115] Copyright 2001, American Association for the Advancement of Science (AAAS).

power required to induce breakdown P_{BD} also shows a nonlinear trend for $L_{\text{CH}} < 1\text{ }\mu\text{m}$. For $L_{\text{CH}} > 1\text{ }\mu\text{m}$, P_{BD} increases linearly at $0.1\text{ mW }\mu\text{m}^{-1}$ with an increase in L_{CH} (Figure 13d). One can explain the nonlinearity of the P_{BD} variation with L_{CH} for $L_{\text{CH}} < 1\text{ }\mu\text{m}$ by solving the heat equation for the m-SWCNTs after considering contributions from the thermal resistances at the m-SWCNT/source-drain contacts.^[234] In transistors with high density of aligned arrays of SWCNTs as the channel and with $T_{\text{GD}} > 1/N_{\text{SWCNT}}$, where N_{SWCNT} is the number of SWCNTs per unit width of the transistor, a breakdown in one SWCNT can propagate to neighboring ones.^[245,246] The use of $T_{\text{GD}} < 1/N_{\text{SWCNT}}$ avoids such correlated breakdown (Figure 13e)^[245] and enables the application of electrical breakdown even with $N_{\text{SWCNT}} \approx 100\text{ }\mu\text{m}^{-1}$.^[64]

The location and size ($\approx 20\text{--}300\text{ nm}$) of the breakdown for this m-SWCNT removal method varies randomly,^[241,247] which limits the ability to define device and circuits with source/drain contacts at predefined locations.^[83,117] Along with this fundamental disadvantage, breakdown also requires SWCNT heating at powers of $\approx 0.1\text{ mW }\mu\text{m}^{-1}$ for $L_{\text{CH}} > 1\text{ }\mu\text{m}$; this value increases for smaller L_{CH} (Figure 13d). Such high powers induce conduction in the s-SWCNTs with large d via band-to-band tunneling^[119,248] and results in their removal via electrical breakdown.^[83,249] Breakdown can also cause avalanche effects^[250] and subsequent failure in gate dielectrics with significant heat sinking at the contacts.^[234] All these effects in combination degrade the performance of transistors fabricated with the remaining s-SWCNTs. The extracted μ_{FE} is $\approx 350\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ for $L_{\text{CH}} \approx 1\text{ }\mu\text{m}$ transistors with low density SWCNTs,^[83] whereas the value is $\approx 75\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ for $L_{\text{CH}} \approx 400\text{ nm}$ transistors with high density SWCNTs,^[64] both of which are lower than the pristine values (Figure 6d,e).

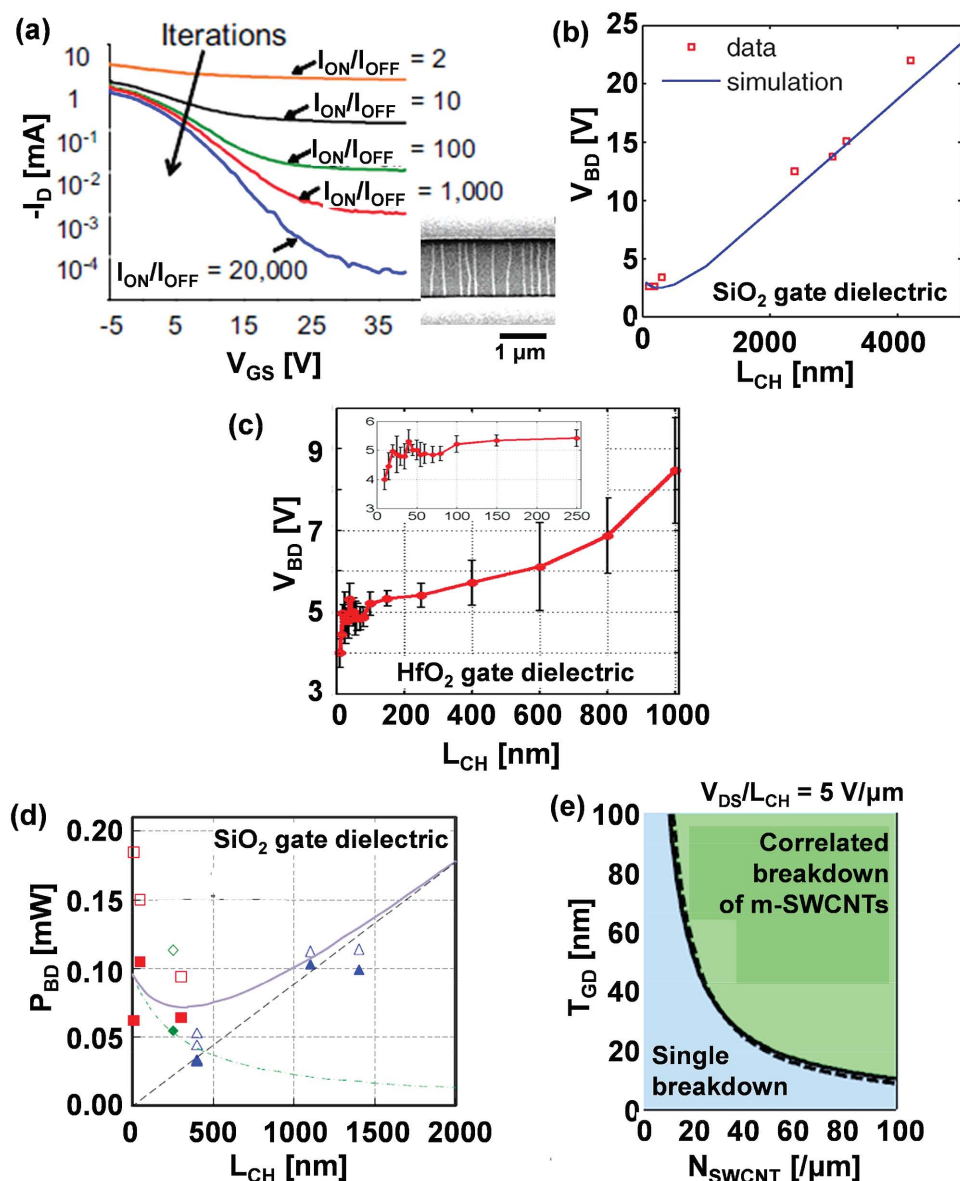


Figure 13. a) Transfer characteristics obtained after successive iterations of electrical breakdown using a gradually increasing V_{DS} in a transistor that uses aligned arrays of SWCNTs. Inset: SEM image of the channel area. Panel (a) is replotted using information from ref. [83]. Breakdown voltage (V_{BD}) as a function of L_{CH} for m-SWCNTs in a transistor configuration made on b) SiO_2 ^[236] and c) HfO_2 ^[117] gate dielectric. Panel (b) is reproduced with permission.^[236] Copyright 2007, IEEE. Panel (c) is reproduced with permission.^[117] Copyright 2013, American Chemical Society. Inset of (c): Fluctuations in measured V_{BD} for smaller L_{CH} . d) Power (P_{BD}) required to induce electrical breakdown for different L_{CH} . Reproduced with permission.^[234] Copyright 2008, IOP. e) Simulated design criteria to avoid correlated breakdown (i.e., propagation of breakdown from one m-SWCNT to a neighboring one) in terms of T_{GD} and number of SWCNTs per unit width (N_{SWCNT}) for an applied electric field of $5 \text{ V } \mu\text{m}^{-1}$ across the m-SWCNTs. The breakdown electric field used in simulation is calculated using $P_{BD} \approx 0.1 \text{ mW } \mu\text{m}^{-1}$ (d) and $I_{BD} \approx 20 \text{ } \mu\text{A}$. The figure is replotted using data from ref. [244].

4.3. Patterned Removal of SWCNTs from Random Networks of SWCNTs

In transistors that use random networks of SWCNTs, the I_{ON}/I_{OFF} ratios can be increased by introducing thin, parallel striped patterns of SWCNTs along the channel length.^[34,184] This lithographic patterning of the SWCNT network can increase its percolation threshold to levels beyond the density of the m-SWCNTs in the device, thereby eliminating current conduction purely through the m-SWCNT pathways. **Figure 14a–d**

schematically illustrates this concept, where the introduction of thin stripes with width W_S in a transistor with m-SWCNT density D_M greater than the percolation threshold density D_P before striping removes conduction through m-SWCNTs. Striping, therefore, modifies the percolation threshold of the SWCNT network to D_P' and increases I_{ON}/I_{OFF} to various levels (10^1 – 10^4) depending on W_S (Figure 14e) and L_{CH} (Figure 14f). A detailed theoretical model based on stick percolation theory identifies that ratios such as L_{CH}/W_S , W_S/L_{SWCNT} (**Figure 15a,b**; where L_{SWCNT} is the average length of SWCNTs) and SWCNT

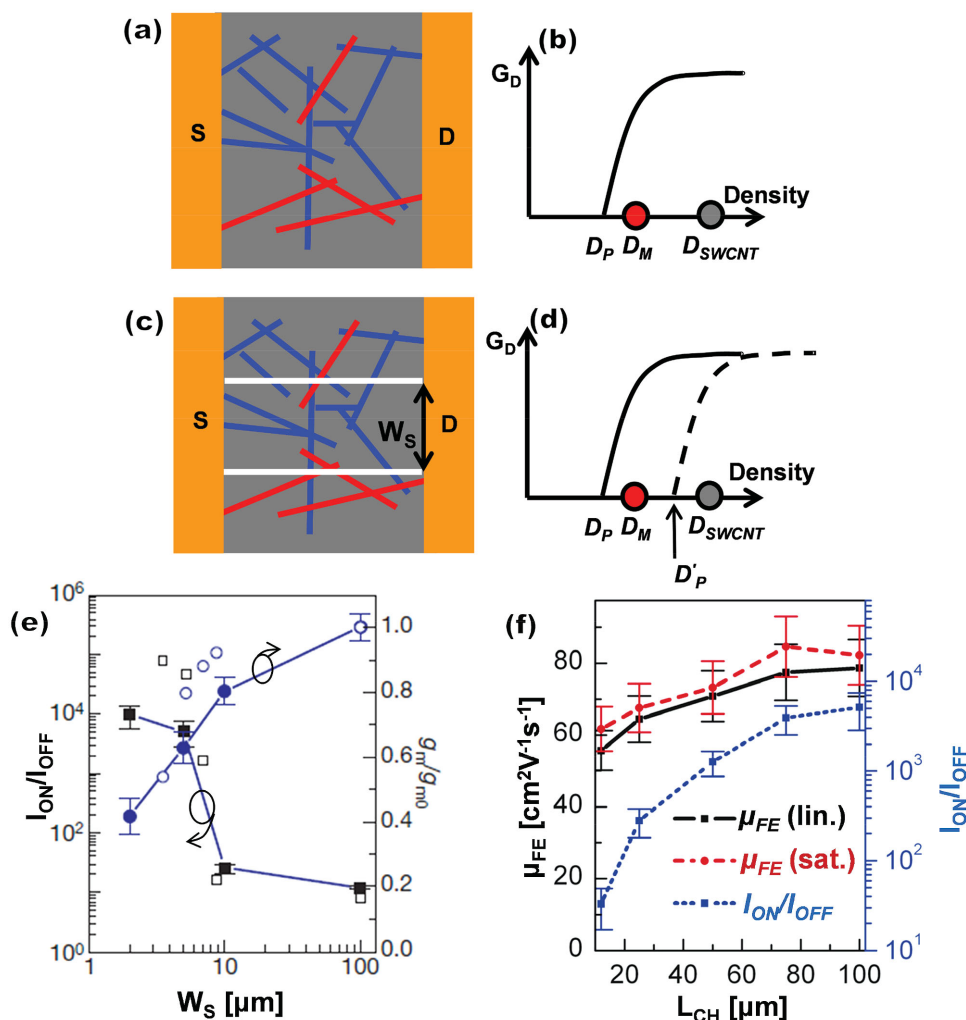


Figure 14. Schematic illustrations of conduction paths and plots of G_D vs SWCNT density (D_{SWCNT}) a,b) before and c,d) after striping in a transistor with random networks of SWCNTs as the channel. The blue and red lines in (a,c) represent s- and m-SWCNTs, respectively. In (a,b), both D_{SWCNT} and m-SWCNT density (D_M) are higher than the percolation threshold density (D_P) and, hence, all of the SWCNTs contribute to G_D . Introduction of striping (width W_S) defines a new percolation threshold density (D'_P) in panel (c,d) and breaks conduction through the m-SWCNTs. a-d) Reproduced with permission.^[184] Copyright 2009, Springer. e) The measured (filled) and simulated (open) variations of the $I_{\text{ON}}/I_{\text{OFF}}$ ratio and normalized transconductance (g_m/g_{m0} , where g_{m0} represents the response without strips) with W_S in transistors with $L_{\text{CH}} \approx 100 \mu\text{m}$ and networked SWCNTs as the channel. f) Variations in μ_{FE} and $I_{\text{ON}}/I_{\text{OFF}}$ with L_{CH} in transistors with $W_S \approx 5 \mu\text{m}$. Here, μ_{FE} is calculated in linear (lin.) and saturation (sat.) regions using $V_{\text{DS}} = -0.2 \text{ V}$ and -2 V , respectively. e,f) Reproduced with permission.^[34] Copyright 2008, Macmillan.

density (Figure 15c,d) are controlling factors of $I_{\text{ON}}/I_{\text{OFF}}$. A reduction in conduction through the SWCNT network (monitored using electrical parameter maximum transconductance, $g_m = \partial I_D / \partial V_{\text{GS}}|_{\text{max}}$ in Figure 14e) is an obvious consequence of striping due to the elimination of source to drain conduction through the m-SWCNTs. The reduction in conduction can be controlled at various levels and minimized up to 40–60% by adjusting the widths of the regions where SWCNTs are removed down to sub- μm level.^[34] A similar current reduction is typical for any post-processing scheme,^[83,119,120] which suggests that striping is a good technique to exclusively remove conduction through m-SWCNTs without compromising the performance of s-SWCNTs in networked transistors.

In addition to patterned striping of SWCNT networks, removal of SWCNTs from patterned holes also increases

$I_{\text{ON}}/I_{\text{OFF}}$ in associated transistors.^[251,252] The process here involves creation of nanoscale holes via electron-beam (e-beam) lithography within the SWCNT network (Figure 16a,b) made with presorted SWCNTs with $\approx 90\%$ s-SWCNT purity and shows increase in $I_{\text{ON}}/I_{\text{OFF}}$ from 10^2 to 10^6 (Figure 16c,d) with a significant reduction in I_{ON} (Figure 16e) with increasing hole density. Though a detailed theoretical analysis is lacking for these transistors, removal of current percolation paths through m-SWCNTs using nanoscale holes is the likely origin of $I_{\text{ON}}/I_{\text{OFF}}$ increase for this case.^[252] Overall, patterned removal of SWCNTs offers a simple and effective way to increase the $I_{\text{ON}}/I_{\text{OFF}}$ ratio in transistors with networked SWCNTs as the channel. Improvement of this method can be aimed at limiting the loss of conduction by optimizing the areas of SWCNT removal.

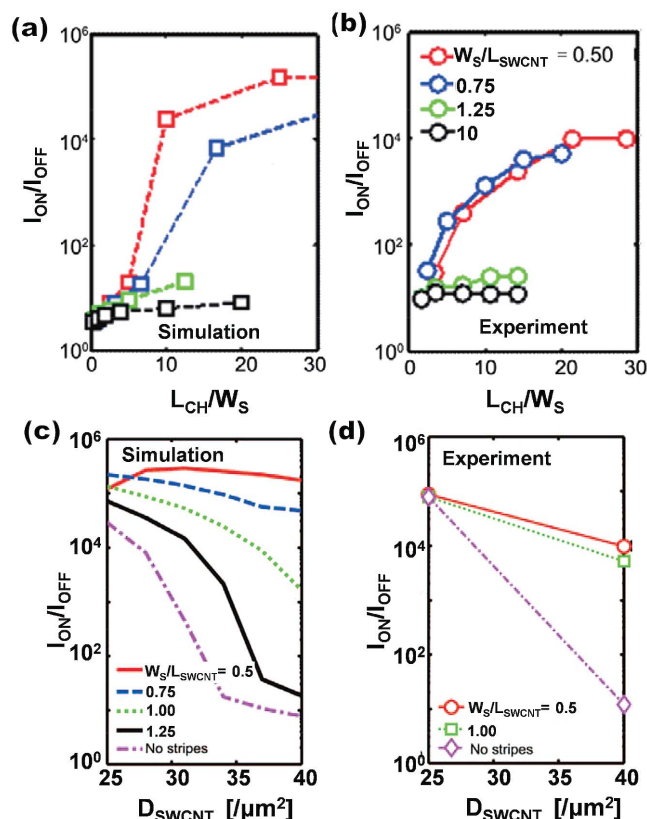


Figure 15. a,c) Simulated and b,d) measured variations of the I_{ON}/I_{OFF} ratio vs L_{CH}/W_S (for $D_{SWCNT} \approx 40 \mu\text{m}^{-2}$) and as a function of D_{SWCNT} (for $L_{CH}/L_{SWCNT} \approx 25$) for various values of W_S/L_{SWCNT} in transistors with networked SWCNTs as the channel. Here, L_{SWCNT} is the average length of SWCNT in the network. Reproduced with permission.^[184] Copyright 2009, Springer.

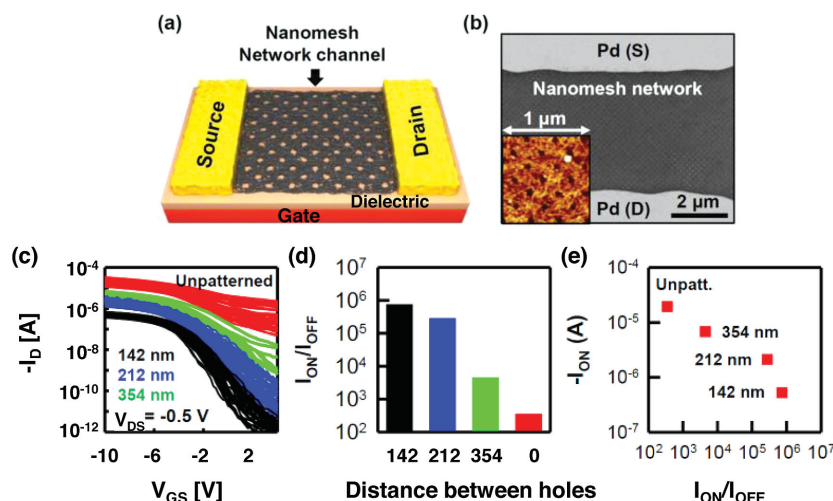


Figure 16. a) Schematic illustration of a bottom-gated transistor with a nanomesh SWCNT network as the channel. b) SEM and AFM (inset) images of the device show ≈ 50 nm diameter holes where SWCNTs have been removed using e-beam lithography and O_2 plasma. The average distance between the holes is ≈ 212 nm. c) Transfer characteristics and d,e) I_{ON}/I_{OFF} ratios for various distances between the holes (142 nm, 212 nm, and 354 nm) are compared with transistors with unpatterned SWCNT network as the channel. $W = 3 \mu\text{m}$ and $L_{CH} = 4 \mu\text{m}$ for all the devices. Reproduced with permission.^[251] Copyright 2014, Springer.

4.4. Selective Chemical Modification of m-SWCNTs

Among the postprocessing methods to improve I_{ON}/I_{OFF} , selective chemical etching offers, in principle, the simplest and the most scalable way to remove m-SWCNTs from as-grown substrates. The challenge, however, is to find a chemical compound that exclusively reacts with the m-SWCNTs. A diazonium reagent (aqueous solution of 4-bromobenzenediazonium tetrafluoroborate with $\text{pH} = 10$) was among the first compounds to be explored for this purpose.^[253,254] For this method, a substrate with as-grown SWCNTs is immersed in the reagent. The proposed reaction of the reagent with a SWCNT requires electron transfer from the SWCNT to the molecules (Figure 17a,b), which is most probable for m-SWCNTs due to adequate charge carriers near the Fermi level.^[254] The reaction eliminates conduction in the m-SWCNTs, thereby allowing the fabrication of transistors with large I_{ON}/I_{OFF} ratios (Figure 17c). The concentration of the solution and the duration of stirring, however, are critical to avoid undesired reactions with the s-SWCNTs. The s-SWCNTs are mostly p-type due to surface-bound hydroxyl groups^[57,59,60,255] and have sufficient charge carriers near the Fermi level. These carriers potentially induce chemical reactions between the s-SWCNTs and the reagents for long duration stirring particularly at high concentrations. The proposed reaction of SWCNTs with the diazonium reagents presumes an availability of electrons as charge carriers.^[254] The role of holes and density of states, in general, during the reaction remains unclear. These reactions with the s-SWCNTs result in devices with low I_{ON} .^[253] This loss of selectivity in chemical reaction suggests uncontrollable removal/damage of s-SWCNTs even at the most optimized condition, as is evident from the extracted $\mu_{FE} \approx 5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in Figure 17c for the transistor with $L_{CH} \approx 5 \mu\text{m}$ (curve D).

Methane plasma has also been studied for selective etching of m-SWCNTs over a narrow diameter range of 1.4–2 nm.^[116] Figure 18a illustrates the process where transistors with a few SWCNTs as the channel are exposed to methane plasma at 400 °C followed by 600 °C annealing in vacuum. The methane plasma selectively etches m-SWCNTs at multiple locations along their length and increases I_{ON}/I_{OFF} from $\approx 10^1$ to $>10^3$ (Figure 18b). Conduction in transistors containing only s-SWCNTs is also affected during the plasma treatment (Figure 18c), as also evident from the extracted $\mu_{FE} \approx 100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (more than an order of magnitude less than that in as-grown substrates; Figure 6e) for $L_{CH} \approx 300$ nm in the associated devices. A detailed study of 244 transistors containing a few (≈ 1 –3) SWCNTs suggests that the plasma treatment is effective for SWCNTs with d in between 1.4 nm and 2.0 nm. For $d < 1.4$ nm, all the SWCNTs are affected, while the process is ineffective for $d > 2$ nm SWCNTs (Figure 18d). Similar to the reactions between the diazonium reagent and m-SWCNTs,^[254] an abundance of delocalized electronic

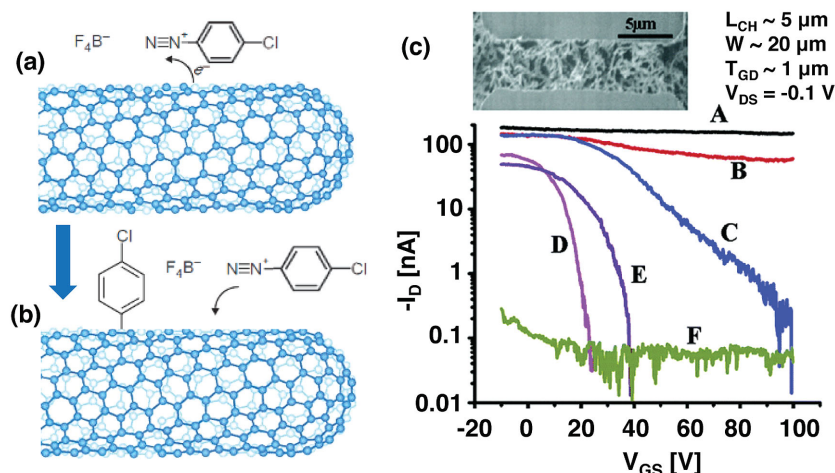


Figure 17. a) Proposed reaction of diazonium reagents with a SWCNT. The reagents extract electrons from the SWCNT and form a stable C–C bond at its surface. The extent of electron transfer depends on the availability of charged carriers near the Fermi level and hence is more probable for m-SWCNTs. b) The functionalized SWCNT forms a radical cation and can further receive electrons from neighboring SWCNTs or react with fluoride or diazonium salts. a,b) Replotted using information from ref. [254]. c) Transfer characteristics of a transistor (SEM image is shown at the top) before (A) and after diazonium reagent treatments (B–F). The curves (B,C) are after first and second reactions with $5.3 \times 10^{-13} \text{ M}$ solution, (D–F) are after third, fourth, and fifth reactions with $3.7 \times 10^{-3} \text{ M}$ solution, respectively. c) Reproduced with permission.^[253] Copyright 2004, American Chemical Society.

states in the m-SWCNTs^[256] explains their enhanced chemical reactivity with the methane plasma. The loss of selectivity for $d < 1.4 \text{ nm}$ SWCNTs apparently arises from the higher radius of curvature and higher strain in the C–C bond of SWCNTs that leads to enhanced chemical reactivity.^[257,258] The absence of etching for $d > 2 \text{ nm}$ SWCNTs remains unexplained. In the future, the effectiveness of this approach will require a tighter diameter distribution (with $d \approx 1.4\text{--}2 \text{ nm}$) of the as-grown SWCNTs and a better selectivity for m-SWCNT etching without affecting the s-SWCNTs. In a recent paper, hydrogen is used as an in situ etchant for the m-SWCNTs.^[259] The process yields $\approx 93\%$ s-SWCNTs and $I_{\text{ON}}/I_{\text{OFF}} > 10^4$, $\mu_{\text{FE}} \approx 10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $L_{\text{CH}} \approx 100 \mu\text{m}$ transistors that use network SWCNTs as the channel. The extracted μ_{FE} is an order of magnitude lower than the pristine values (Figure 6f).

A few recent studies suggest the effectiveness of using oxidants such as water vapor to selectively etch m-SWCNTs from substrates with horizontally aligned SWCNTs.^[147,149,193] Figure 19 shows an example of this approach on a substrate with a few s-SWCNTs (and 90% m-SWCNTs). The entire catalyst area (stripes at the top of Figure 19a) and all m-SWCNTs are removed after $\approx 6000 \text{ ppm}$ water treatment at 750°C (Figure 19c). Availability of electronic states near the Fermi level and a higher enthalpy change during the reaction of m-SWCNTs with hydroxyl groups explain this preferential etching.^[108,193,260] A transistor made with water treated SWCNTs shows $I_{\text{ON}}/I_{\text{OFF}} \approx 3000$ (Figure 19e). The low I_{ON} in this transistor might be due to the low concentration ($\approx 10\%$) of s-SWCNTs on the pristine substrate and also due to the damage to some of the s-SWCNTs during water treatment.^[193] In some cases, a trace amount of oxygen, a stronger oxidant than water, suggests

selective etching of m-SWCNTs.^[261] In other cases, the catalyst support in the form of ceria, which contains active oxygen, enables growth of $\approx 95\%$ s-SWCNTs, $I_{\text{ON}}/I_{\text{OFF}} \approx 15$, and $\mu_{\text{FE}} \approx 1000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $L_{\text{CH}} \approx 1 \mu\text{m}$ transistors that use arrays of SWCNTs as the channel.^[106]

As opposed to ex situ removal of m-SWCNTs using water vapor at $\approx 6000 \text{ ppm}$, in situ etching of m-SWCNTs can occur at much lower water concentrations.^[149] The effectiveness of this process requires SWCNT growth at a low rate, achieved by using a controlled flow of Ar through the ethanol bubbler, to ensure prolonged proximity of SWCNTs to catalysts and, hence, an enhanced possibility of m-SWCNT etching with the water vapor.^[147,149,262–264] Transistors made with SWCNTs synthesized using $\approx 307 \text{ ppm}$ water vapor show moderate $I_{\text{ON}}/I_{\text{OFF}} = 10^1\text{--}10^2$ (Figure 20a–c).^[149] One interesting feature of water-assisted growth is revealed at increased concentrations of the carbon feedstock; in this case, the increase in water concentration leads to increases in SWCNT density, along with an improved $I_{\text{ON}}/I_{\text{OFF}}$ (Figure 20d,e). Increase in water

concentration beyond an optimum value ($\approx 508 \text{ ppm}$), however, etches all the SWCNTs with no selectivity, reduces the SWCNT density and the $I_{\text{ON}}/I_{\text{OFF}}$ ratio (Figure 20f). Even for the optimum water concentration of $\approx 508 \text{ ppm}$, SWCNTs with $d < 1\text{--}1.5 \text{ nm}$ are etched with no selectivity.^[147,193] High local strain due to increased curvature in the small d SWCNTs explains such non-selective etching.^[257,258] High local strain is also present in random SWCNTs near the catalyst area of aligned arrays of SWCNTs,^[22,108,123,147] which inspired the use of multiple-cycle growth with intermittent water treatment in Ar ambient to remove random SWCNTs from the quartz substrate and increase the density of SWCNTs from 1–2 per μm to ≈ 10 per μm .^[147] The diameter of SWCNTs grown in this manner, however, increases after multiple cycles due to coarsening of catalyst sizes via Ostwald ripening.^[147,154,156,157] Use of substrates, such as alumina, silica, or MgO that have higher catalytic activity to limit the sizes of the catalysts may become useful to avoid this coarsening. Overall, the applicability of chemical etching of m-SWCNTs with specific chemicals requires improvement in selectivity towards m-SWCNTs across broad ranges in diameter without affecting the s-SWCNTs.

4.5. Optical Excitation and Ablation of m-SWCNTs

Optical absorption in SWCNTs depends on the energy separation between different Van Hove singularities in the density of states–energy diagrams of SWCNTs (Figure 21a).^[265,266] The magnitude of this energy separation depends on the type and diameter of SWCNTs (Figure 21b; Kataura plot),^[265] a property that is routinely used in Raman spectroscopy^[267] and PL^[268,269]

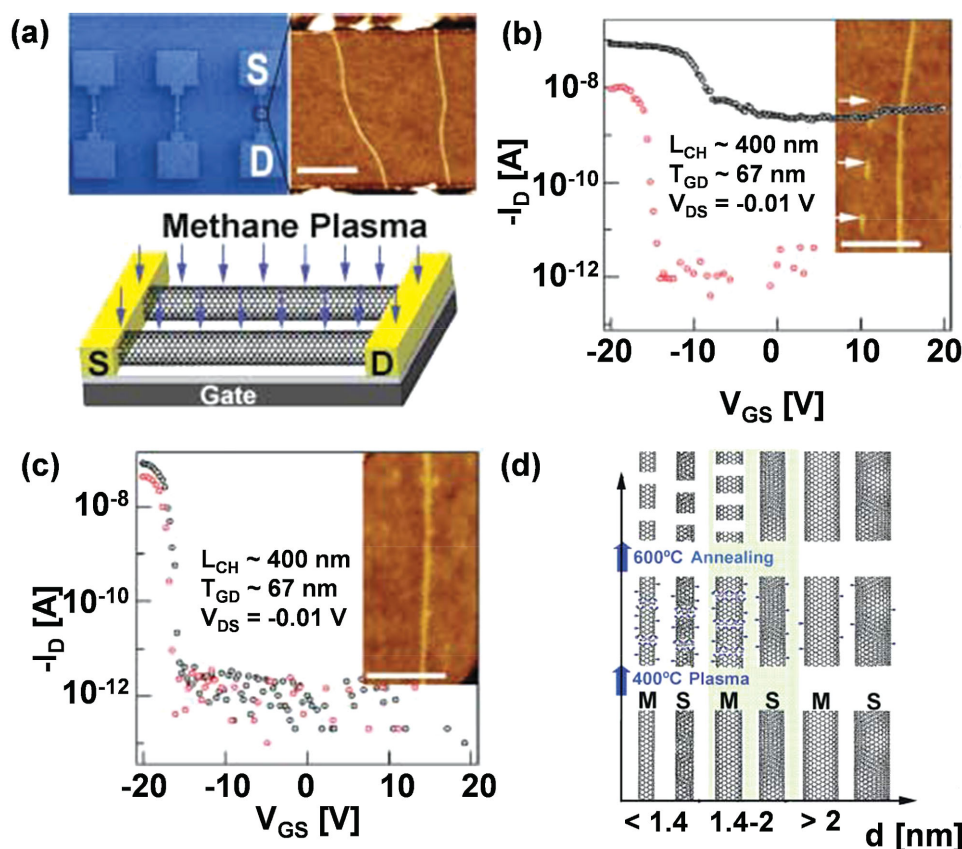


Figure 18. Etching of m-SWCNTs using methane plasma. a) SEM (top left) and AFM images (top right) of transistors containing a few SWCNTs as the channel. Schematic illustration of the methane plasma treatment is shown at the bottom. Transfer characteristics of transistors containing b) one m- and one s-SWCNT and c) one s-SWCNT before (black circle) and after (red circle) plasma treatment. Insets in (b,c) show AFM images (scale bar = 100 nm) of each device after the plasma treatment. White arrows in (b) highlights the etched m-SWCNT in the device. d) Schematic illustrations of the effect on m- and s-SWCNTs of different d during plasma treatment. Reproduced with permission.^[116] Copyright 2006, AAAS.

to identify SWCNTs. A few recent attempts have also explored the selective optical absorption of m-SWCNTs to induce heating at levels sufficient to induce oxidation and ablation.^[270–272] As per Figure 21b, optical excitation at energies < 0.4 eV (i.e., wavelength $\lambda > 3$ μ m) should selectively excite most of the m-SWCNTs. Ablating these m-SWCNTs by heating them up to temperatures necessary for oxidation in air (≈ 600 °C) requires electrical powers of ≈ 0.1 mW μ m^{−1} (assuming SWCNTs are placed on a silicon substrate with a ≈ 200 nm thick thermal oxide).^[235] This corresponds to an equivalent optical intensity of ≈ 0.1 MW mm^{−2} for ablation; the calculation assumes perfect absorption (i.e., infinite absorption coefficient) and a diameter $d = 1$ nm for the SWCNTs.

SWCNT ablation experiments via irradiation of the substrate with $\lambda = 2$ μ m pulsed laser suggests removal of m-SWCNTs at an optical intensity of ≈ 1.8 MW mm^{−2}.^[272] This is an order of magnitude higher than the electrical equivalence of ≈ 0.1 MW mm^{−2} calculated above, presumably because of the finite absorption coefficient for SWCNTs,^[273–275] dissimilarities in heat dissipation under DC electrical stress,^[235] and pulsed optical excitation.^[272] The process implemented on transistors with low density of SWCNTs yields insignificant improvement

in the I_{ON}/I_{OFF} ratio. This may appear to contradict the Kataura plot (Figure 21b), which suggests selective ablation for $\lambda > 3$ μ m. Our recent experiments with optical excitation of m-SWCNTs also suggest loss of selectivity at higher optical intensities for $\lambda > 2.5$ μ m.^[118,120] These results indicate that the Kataura plot is not the only factor that defines the optical selectivity of m- and s-SWCNTs. Consideration of optical excitation due to the presence of free carriers from unintentional doping^[57,59,60,255] may also be important. The removal of this doping may improve selectivity for the ablation process.

Other studies used in situ UV ($\lambda \approx 200$ –400 nm) radiation^[271] and ex situ xenon-lamp ($\lambda \approx 0.18$ –11 μ m) irradiation^[270] to selectively remove m-SWCNTs. The irradiation intensity of ≈ 75 –80 mW cm^{−2} was smaller than the calculated electrical equivalence presumably because of the use of heated substrate during irradiation. Transistors made with aligned arrays of SWCNTs suggest the possibility of increasing I_{ON}/I_{OFF} up to 10^3 with $\mu_{FE} \approx 180$ cm² V^{−1} s^{−1} (for $L_{CH} \approx 3$ μ m) after 45 min Xe irradiation. These UV and Xe irradiations are expected to excite a range of s-SWCNTs (according to Figure 21b) in addition to m-SWCNTs. Additional work will be needed to confirm and refine these results as well as to

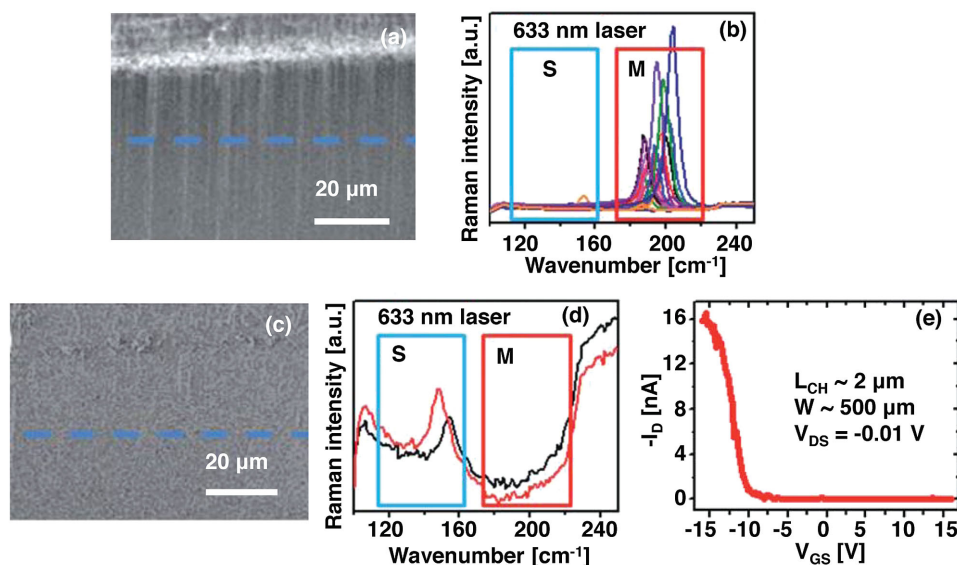


Figure 19. a) SEM image and b) Raman analysis (RBMs) of aligned arrays of SWCNTs before water treatment. c,d) The same after 6000 ppm water treatment at 750 °C. Raman analysis suggests complete removal of m-SWCNTs in the red rectangle marked with M. e) Transfer characteristics of a transistor fabricated with aligned-array SWCNTs suggests $I_{\text{ON}}/I_{\text{OFF}} \approx 3000$ after water treatment. Adapted with permission.^[193] Copyright 2011, Royal Society of Chemistry.

explore the underlying chemical and physical mechanisms behind the process.

4.6. Thermocapillary-Enabled Purification

Thermocapillary-enabled purification (TcEP) is a very recent technique that offers exceptional effectiveness for selective removal of m-SWCNTs from as-grown substrates with horizontally aligned arrays of SWCNTs. The process involves three steps (**Figure 22a**): 1) formation of a molecular resist layer on a substrate with SWCNTs, 2) selective, but mild heating of m-SWCNTs to pattern co-located openings in the resist by thermocapillary (Tc) flow, and 3) etching of m-SWCNTs through these patterns using an O₂ plasma. The choice of a molecular resist such as α,α,α' -tris(4-hydroxyphenyl)-1-ethyl-4-isopropylbenzene is critical to the process to ensure narrow patterns at the positions of the m-SWCNTs and to protect the s-SWCNTs against damage during O₂ plasma etching.^[119] The heating of the m-SWCNTs induces Tc flow in the resist (henceforth called a Tc resist) and forms trenches at the locations of the m-SWCNTs (**Figure 22b**). The widths (W_{Tc}) and depths (H_{Tc}) of the trenches can be controlled by the extent (duration, input power) of m-SWCNT heating, the substrate temperature,^[119,276] and the viscosity of the resist.^[276] In general, a Tc resist heated to an optimum temperature forms complete trenches (i.e., throughout the thickness) with a W_{Tc} that decreases from the top to the bottom of the trench (**Figure 22c**). Simulation of the process of trench formation using the one-dimensional lubrication equation captures the experimental trends (**Figure 22d**) and suggests that the trench results from sharp gradients in temperature and at rates that increase with decreasing viscosity or increasing temperature coefficient of surface tension. The geometry of the trenches follow the positions of the

m-SWCNTs (**Figure 22b**), thereby enabling selective removal of the m-SWCNTs using O₂ plasma without causing any damage to s-SWCNTs, which remain masked by the Tc resist. The removal of Tc resist using acetone leaves a highly pure array of s-SWCNTs.

A critical aspect of the TcEP process is selective heating of m-SWCNTs. This selective heating is currently achieved using electrical^[119,121] or electromagnetic^[118,120] excitation. The electrical excitation of m-SWCNTs uses two metal contacts connected at the two ends of the SWCNTs and involves elimination of conduction through the s-SWCNTs by application of a positive V_{GS} in partial-gate transistor geometry (**Figure 23a**)^[119] or by use of interdigitated contacts made with Ti^[121] or metals having similar workfunctions (**Figure 23b**). The partial-gate geometry is beneficial over conventional full-gate geometry for the TcEP process as full-gate geometry allows conduction via band-to-band tunneling near the cathode end in some of the s-SWCNTs with large d .^[119,248] The second option eliminates the complexity associated with the partial-gate structure and relies on contacts with workfunction near the mid-bandgap of s-SWCNTs instead, thereby resulting in high Schottky barriers that block electron and hole injection into s-SWCNTs and hence ensure good selectivity for the TcEP process.^[121]

The electromagnetic approach to heat m-SWCNTs uses microwave irradiation with direct-contact (**Figure 23c**) or removable (**Figure 23d**) metallic dipole antennas^[120] or uses infrared ($\lambda = 2.5 \mu\text{m}$) laser light (**Figure 23e**).^[118] The dipole antennas enable use of desktop microwave ovens by amplifying the microwave fields to compensate for the small absorption cross-section $\approx 10^{-5}$ – 10^{-4} of the m-SWCNTs.^[274] Antennas (**Figure 23 c,d**) with $<100 \mu\text{m}$ gaps between the antenna arms show an induced electric field across the antenna arms strong enough to yield significant current injection from the arms

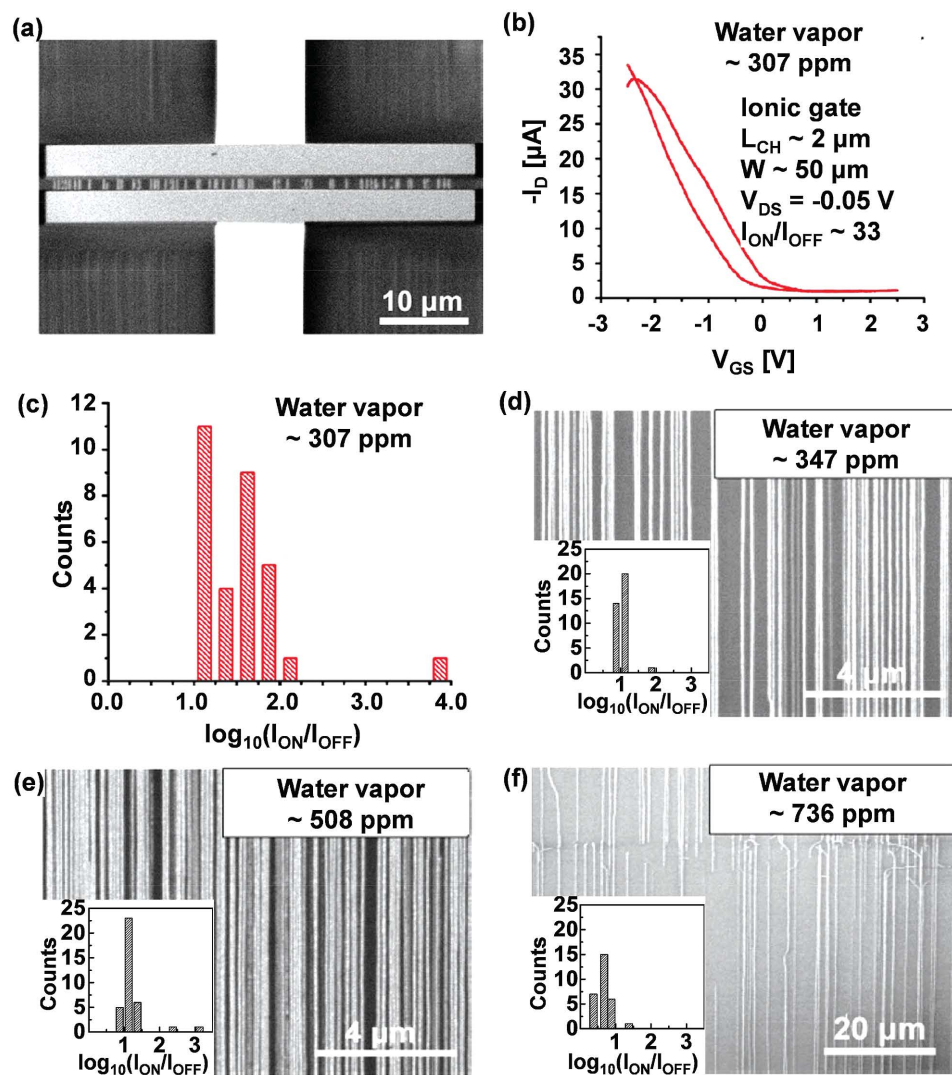


Figure 20. a) SEM image, b) transfer characteristics, and c) distribution of $I_{\text{ON}}/I_{\text{OFF}}$ ratios in transistors made with aligned arrays of SWCNTs grown on a Y-cut quartz substrate using Cu catalyst, ethanol vapor as the carbon feedstock, and 307 ppm water vapor as the m-SWCNT etchant. d,e) SEM images of SWCNTs on as-grown substrates and $I_{\text{ON}}/I_{\text{OFF}}$ distributions (insets) of associated transistors made using various concentrations of water vapor at a higher concentration of the carbon feedstock compared to that used in (a–c). The SWCNT density and $I_{\text{ON}}/I_{\text{OFF}}$ ratios increase with an increase in water vapor from ≈ 347 ppm to ≈ 508 ppm and then both decrease for ≈ 736 ppm water vapor. Reproduced with permission.^[149] Copyright 2012, American Chemical Society.

into the m-SWCNTs.^[120] When these antennas are in direct contact with the SWCNTs (Figure 23c) and are made with metals, such as Ti, Mo, or Al that have work functions near the mid-bandgap of s-SWCNTs, current flow through the s-SWCNTs is insignificant due to the presence of Schottky barriers at the metal/s-SWCNT interfaces. This direct-contact microwave-based TcEP process, therefore, exclusively creates Tc flows and, therefore, trenches at the m-SWCNTs. The results indicate s-SWCNT purity of $>99.9925\%$, limited only by the statistics of the measurement. As there is no experimental indication that any of the m-SWCNTs remain in any of the cumulative sets of studies on TcEP, it is likely that the purity is even much closer to 100%.

The contactless TcEP is a more scalable process for the removal of m-SWCNTs. The microwave-based contactless

process uses removable antenna printed on a glass substrate, which is separated from the substrate coated with Tc-resist using poly(dimethylsiloxane) (PDMS) micropillars (Figure 23d). Subsequent microwave irradiation leads to trench formation on m-SWCNTs and also on $\approx 40\%$ of the s-SWCNTs, as it does not have the metal/s-SWCNT Schottky barrier.^[120] The laser-based contactless process uses $\lambda = 2.5 \mu\text{m}$ laser light, which is raster scanned over a wide area. Laser irradiation forms trenches on m-SWCNTs and also on $\approx 15\%$ of the s-SWCNTs.^[118] The choice of laser wavelength for this process is inspired by the Kataura plot of Figure 21b that suggests insignificant absorption of laser light by the s-SWCNTs at that wavelength. The TcEP process also excludes use of pulsed laser sources with <5 ns pulse width for the 25 nm thick Tc resist.^[118]

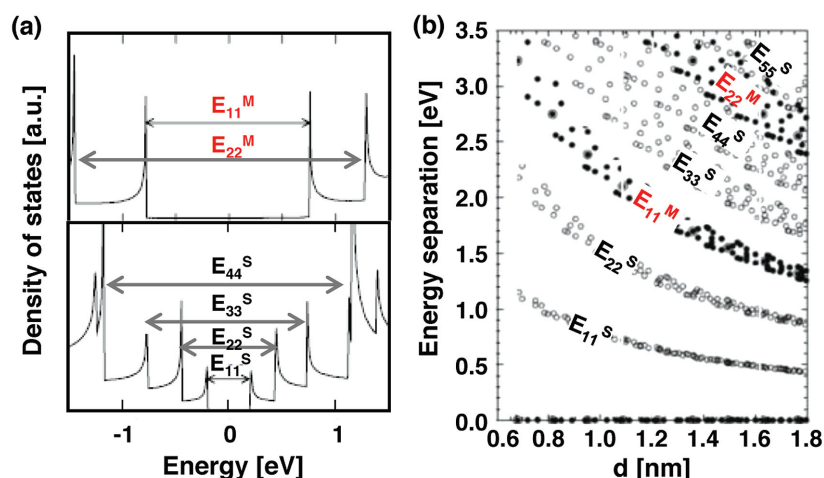


Figure 21. a) Density of states vs energy plot obtained using a tight binding model for an armchair (10,10) m-SWCNT (top) and a zigzag (22,0) s-SWCNT. Energy separations between different Van Hove singularities are marked using $E_{ij}^{S/M}$ for the i -th Van Hove singularities in s- or m-SWCNTs. Reproduced with permission.^[266] Copyright 2003, IOP and Deutsche Physikalische Gesellschaft. b) "Kataura" plot of energy separation vs d for different types of SWCNTs. Reproduced with permission.^[265] Copyright 1999, Elsevier.

After completion of the TcEP process, transistors made with the remaining s-SWCNTs show $I_{ON}/I_{OFF} \approx 10^3$ – 10^6 , which is a significant improvement over the values $\approx 10^0$ – 10^1 obtained before m-SWCNT removal (Figure 24a,b), and an average $\mu_{FE} \approx 1700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (Figure 24c,d) comparable to that obtained in pristine s-SWCNTs (Figure 6d). Transistors also show good current saturation at large V_{DS} (Figure 24e). All of these properties suggest that the process completely removes m-SWCNTs and preserves the quality of the s-SWCNTs. A critical advantage

of TcEP over the extensively used electrical breakdown technique^[28,64,83,117] is its ability to completely remove m-SWCNTs over a wide area, which allows fabrication of arbitrary dimension transistors within that area.^[119,120] Moreover, TcEP requires much lower SWCNT heating with an input power of ≈ 0.01 – $0.02 \text{ mW } \mu\text{m}^{-1}$, compared to electrical breakdown that requires $\approx 0.1 \text{ mW } \mu\text{m}^{-1}$ or higher.^[83,123,234] This reduces the occurrence of avalanche effects and gate dielectric failure for the TcEP process.^[250]

An important limitation of the TcEP process arises from the value of W_{TC} . Recent experimental demonstrations^[118–120] involve a Tc resist with ≈ 25 – 35 nm thickness and $W_{TC} \approx 200$ – 300 nm , which limits the effectiveness of arrays that have densities of larger than 3–5 m-SWCNTs per μm (corresponding to 9–15 SWCNTs per μm for arrays that have 1/3 m-SWCNTs and 2/3 s-SWCNTs). The limitation can be relaxed by using arrays grown with enhanced s-SWCNT purity^[98,100,102,103,107–109] or by reducing the thickness of the Tc resist to enable reductions in W_{TC} (as W_{TC} scales with the thickness of the Tc resist).^[119,276]

4.7. Summary of Post-Processing

Table 2 summarizes the general requirements, type of preserved SWCNTs, and key transistor parameters (I_{ON}/I_{OFF} and

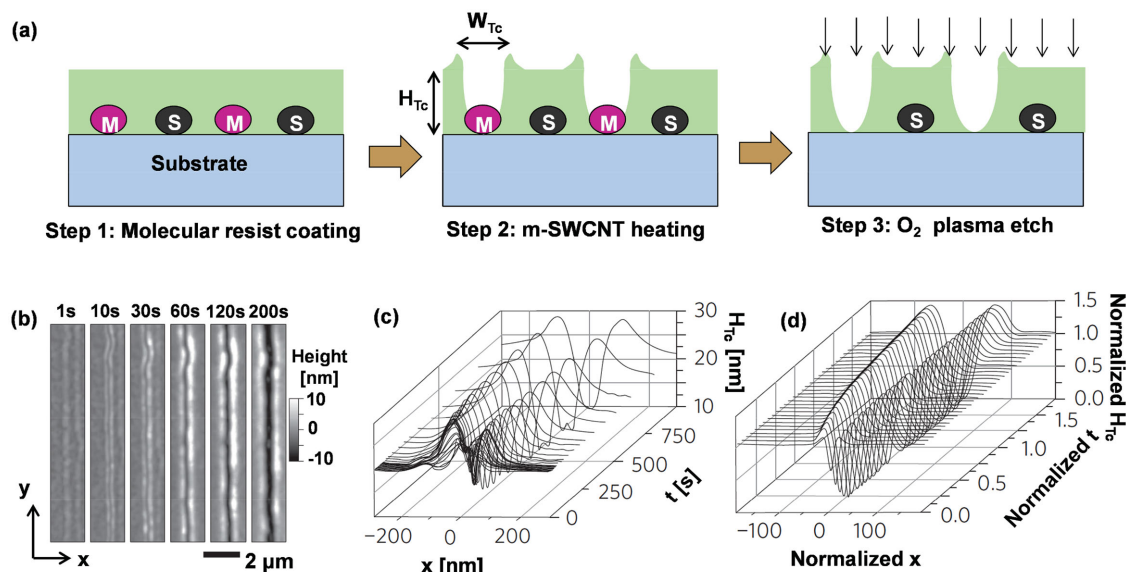


Figure 22. a) Schematic illustration of the three steps in the TcEP process for selective removal of the m-SWCNTs. Heating of the m-SWCNTs induces Tc flow in the resist and creates trenches of width W_{TC} and depth H_{TC} . b) Temporal evolution of AFM topographies of the surface of the resist (thickness $\approx 25 \text{ nm}$) coated on top of a m-SWCNT. Here, the m-SWCNT is Joule heated by applying an electric field of $0.66 \text{ V } \mu\text{m}^{-1}$ along its length through electrodes connected to its ends. c) Averaged (along the length of a m-SWCNT, y) cross-sectional profiles along x extracted from AFM measurements like those shown in (b). d) Theoretical simulation of normalized profiles of the resist as a function of normalized x qualitatively captures the experimental trends in (c). b–d) Adapted with permission.^[119] Copyright 2013, Macmillan.

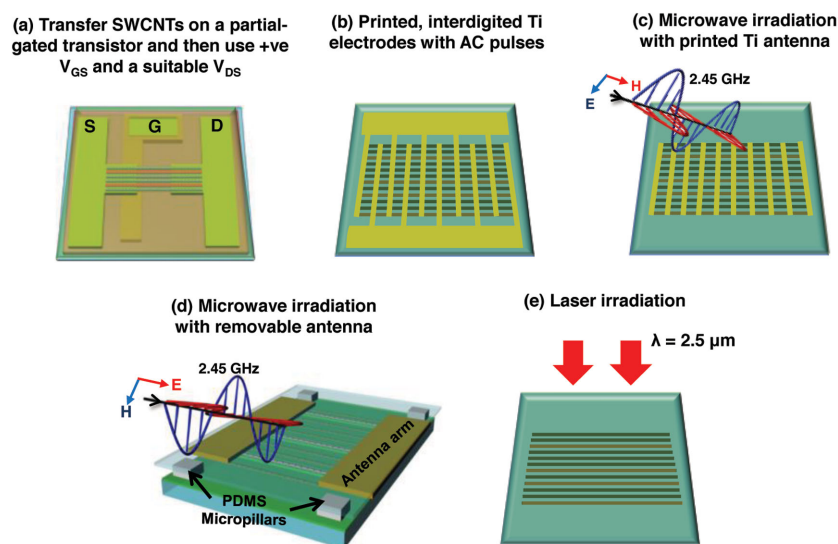


Figure 23. Five different ways of heating m-SWCNTs (brown ones in the figures) for the TCeP process. The heating can be done by a) transferring SWCNTs on a partial-gate transistor and then applying positive V_{GS} and a suitable V_{DS} ,^[119] b) applying AC pulses across interdigitated Ti electrodes,^[121] c) using lithographically defined Ti antennas and microwave irradiation,^[120] d) using removable antennas and microwave irradiation,^[120] and e) using infrared light.^[118] The removable antenna in (d) is printed on a glass substrate and is separated from the substrate coated with the resist on top of SWCNTs using poly(dimethylsiloxane) (PDMS) micropillars. Laser exposure in (e) uses pulsed laser with $\lambda = 2.5 \mu\text{m}$, pulse width = 10 ns, repetition rate = 1 kHz and is raster scanned over a wide area.

μ_{FE}) for the post-processing methods discussed above. Three of the main features—preserved s-SWCNTs, lowest I_{ON}/I_{OFF} , and lowest μ_{FE} —for different methods appear as a spider chart in Figure 25. Transistor parameters in this figure are obtained from devices that use aligned arrays of SWCNTs as the channel, except for results from the patterned removal method where random networks of SWCNTs are used. Moreover, the values of μ_{FE} are compared below by considering their dependence on L_{CH} (Figure 6d–f). Maximizing all the three parameters of the spider chart in Figure 25 in a simple, scalable process represents the main goal for any post-processing method.

Solution-based sorting methods, more specifically DGU^[197] and chromatography^[27,213], can yield suspensions of s-SWCNT to purities of up to 99.9%.^[229] These approaches can process several grams of material in a single batch for deposition and alignment into arrays using techniques such as dielectrophoresis^[223–225] and Langmuir–Schaefer.^[27] For high performance and analog applications, solution-based sorting will require improvements in μ_{FE} and on the length of s-SWCNTs after processing. For low-performance applications such as bendable integrated circuits,^[34,36] conformal tactile sensors,^[63] display electronics,^[37,277,278] and biological and chemical sensing,^[40,42,279] sorted s-SWCNTs can be arranged in random networks to ensure high I_{ON}/I_{OFF} ratios. A competitor for solution-based sorting in these random network applications is the patterned removal method,^[34,184,251,252] as it offers a simpler way to increase the I_{ON}/I_{OFF} ratio with a better μ_{FE} .

Among other methods of post-processing, selective chemical etching^[116,147,149,193,253] and ablation^[270–272] of m-SWCNTs are attractive for large-scale implementation, but they require improved control of the selectivity. In their current forms,

many s-SWCNTs are either removed or partly damaged during the process. Transistors fabricated with the residual s-SWCNTs generally show low μ_{FE} . The method that grows SWCNT on ceria catalyst supports^[106] removes m-SWCNTs via chemical etching, but demands further studies to ensure its repeatability and scalability.

Electrical breakdown, another method for selective chemical etching of m-SWCNTs, results in transistors with a better μ_{FE} compared to the solution-based sorting methods. This method yields transistors with values of μ_{FE} that are lower, compared to those obtained using TCeP. However, as the apparent values of μ_{FE} can vary with L_{CH} due to contact effects (Figure 6d,e), the intrinsic mobilities of the s-SWCNTs for these methods may be similar. A detailed characterization of contact resistance and intrinsic mobility will allow improved comparison between these methods and will reveal any degradation of the s-SWCNTs induced by the processing. In addition, the breakdown method only allows the development of devices and circuits with source/drain contacts at a predefined location, thereby limiting its scalability.^[110]

Although recent work demonstrates the applicability of electrical breakdown for removal of m-SWCNTs in nanoscale transistors,^[64,117,249] mitigating origins of low μ_{FE} with improved scalability should be the topic of future research.

TCeP is a recent method that can completely remove all the m-SWCNTs from aligned arrays of SWCNTs.^[118–121] The method yields transistors with the highest μ_{FE} , similar to the value obtained for transistors with as-grown s-SWCNTs. The process maintains the integrity of the s-SWCNTs and, therefore, offers promise for all forms of SWCNT-based electronics. Experimental demonstration of this approach offers high-quality s-SWCNTs with purity arbitrarily close to 100%, when the m-SWCNTs are heated using electrical contacts either for current injection^[119–121] or for amplification of electromagnetic signals.^[120] The noncontact based implementation^[118,120] preserves as much as $\approx 85\%$ of the s-SWCNTs in the case of the laser-induced process.^[118] Improved s-SWCNT preservation requires reduction in the conductivity of these s-SWCNTs via elimination of unintentional doping,^[57,255] which is also important for the practical use of s-SWCNTs in electronic circuits with a reduced hysteresis.

For the substrate-based sorting methods, except for the patterned removal of SWCNTs, the elimination of m-SWCNTs can increase the variability in the density of the aligned arrays with potential adverse effect on device-to-device repeatability in their properties. These and other undesirable effects might potentially be addressed through advanced circuit designs.^[82]

5. Conclusions and Outlook

This paper summarizes significant, recent progresses toward obtaining substrates with high purity of s-SWCNTs. As-grown

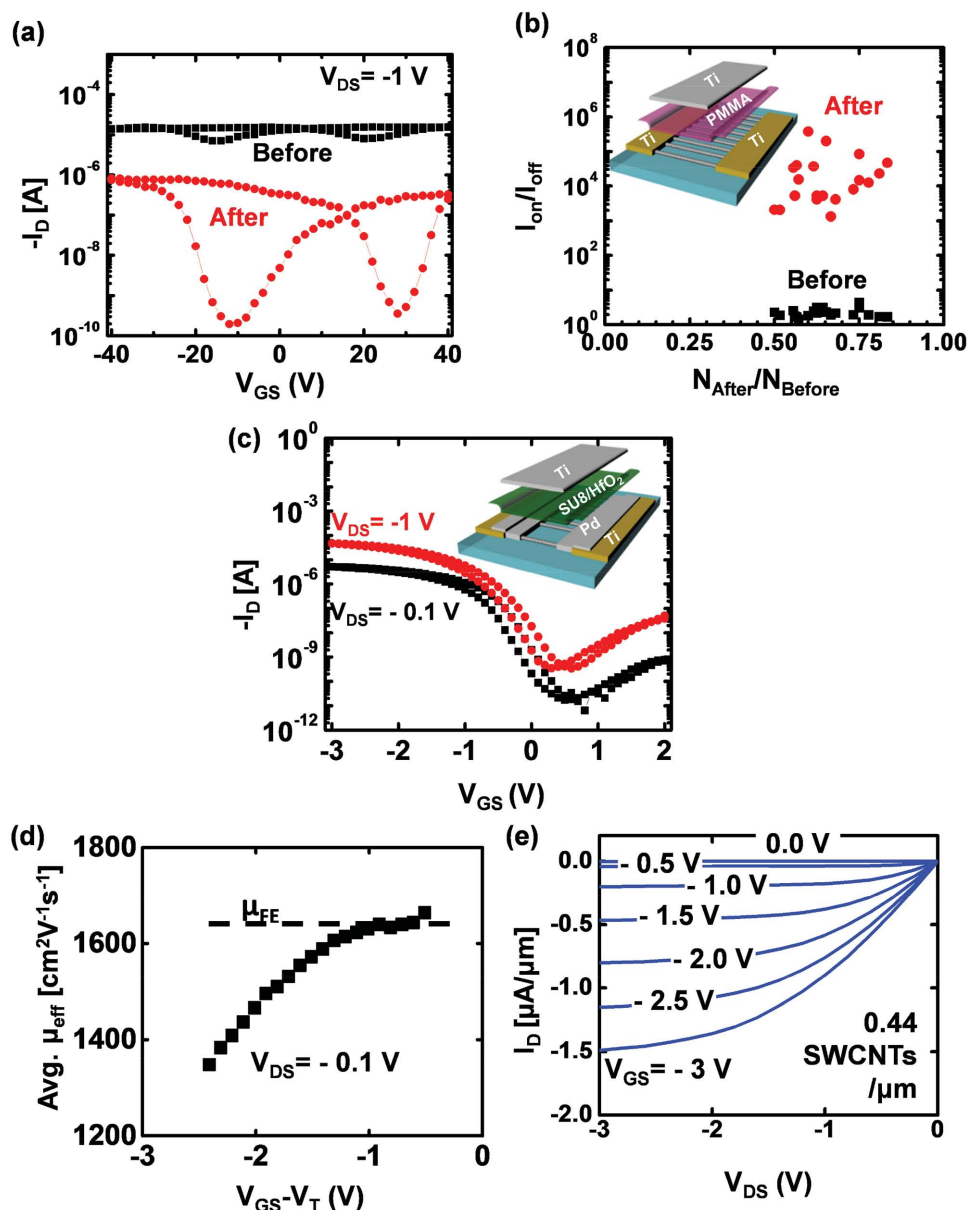


Figure 24. a) Transfer characteristics and b) $I_{\text{ON}}/I_{\text{OFF}}$ vs $N_{\text{After}}/N_{\text{Before}}$ for transistors made with aligned arrays of SWCNTs as the channel before and after the direct contact, microwave-based TcEP process. The transistors use Ti contacts as source/drain; these contacts also serve as antennas to amplify microwave during the TcEP process; Inset: schematic of the transistors. Here, N_{After} and N_{Before} refer to the number of SWCNTs in a transistor before and after TcEP, respectively. c) Typical transfer characteristics at two different V_{DS} , d) extracted effective mobility ($\mu_{\text{eff}} \equiv L_{\text{CH}}/W_{\text{CG}} V_{\text{DS}} \times \partial I_{\text{D}}/\partial V_{\text{GS}}$) averaged over 12 transistors vs $V_{\text{GS}} - V_{\text{T}}$ at low V_{DS} ($\mu_{\text{FE}} \equiv \mu_{\text{eff}}|_{\text{max}}$, see Equation (2), and e) typical output ($I_{\text{D}}-V_{\text{DS}}$) characteristics at different V_{GS} in transistors made with aligned arrays of s-SWCNTs as the channel. These transistors use Pd contacts as source/drain and SU8 (50 nm)/HfO₂ (5 nm) as gate dielectric; Inset of (c): device schematic. Reproduced with permission.^[120] Copyright 2014, Macmillan.

s-SWCNTs may achieve purity levels up to $\approx 96\%$ when formed using Co or Fe catalysts on supports such as silica, alumina, and magnesium oxide at temperatures below 600–700 °C with hydrocarbons as the carbon feedstock. Similar high purities can be achieved at higher process temperatures on silica supports with alcohol as the carbon feedstock. Aligned array transistors fabricated with these s-SWCNTs show excellent field-effect mobility and on-current, but low on/off ratio. These processes, therefore, are inadequate for modern transistors. For high-performance digital, analog, and RF electronics, s-SWCNT

purity in as-grown substrates needs further improvements towards values reaching up to and beyond 99.99%. Additional exploration of heterogeneous catalysis and an improved understanding of the relevant process will be essential to increase s-SWCNT purity to values larger than those presently possible.

The ex situ post-processing approaches, on the other hand, can enhance the purity of s-SWCNTs by selectively removing or chemically modifying the m-SWCNTs. These methods allow better transistor operation with improved on/off ratios. However, most fail to maintain the integrity of the remaining

Table 2. Summary of SWCNT post-processing methods and resultant transistor parameters.

Post-processing method	General requirements	Preserved SWCNTs	Transistor parameters				Refs.
			I_{ON}/I_{OFF}	μ_{FE} [$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$]	L_{CH} [μm]	Configuration	
Electrical breakdown	- High power - Electrostatic gating - Source/drain in predefined locations, as used for purification	$\approx 95\%$ s-SWCNTs	10^3 – 10^4	$75^{a,b)}$	≈ 0.4	Aligned array	[64]
				$350^{a,b)}$	≈ 1	Aligned array	[83]
Solution-based (centrifugation, chromatography, etc.)	- Surfactant/polymer - Centrifuge - Self-assembly for better performance	$>99\%$ s-SWCNTs and $<1\%$ m-SWCNTs	10^1 – 10^7	16 – $27^{a)}$	1 – 10	Aligned network	[27]
				1 – $16^{a)}$	≈ 2	Aligned array	[223]
				1 – $80^{a)}$	≈ 0.1	Single	[213]
				46	≈ 9	Random network	[228]
Patterned removal	- Random network of SWCNTs - Source/drain in predefined locations, as used for purification	All SWCNTs	10^2 – 10^4	$\approx 70^{a)}$	≈ 100	Random network	[34]
Chemical etching	Diazonium salt	–	10^4 – 10^5	$\approx 5^{a)}$	≈ 5	Random network	[254]
	Methane	–	10^5	$\approx 100^{a)}$	≈ 0.3	Single	[116]
	H_2O	–	10^3	–	≈ 2	Aligned array	[193]
	Ceria supports	–	15	$\approx 1000^{a)}$	≈ 1	Aligned array	[106]
Ablation	Radiation source	$d > 1$ nm s-SWCNTs	10^3	$\approx 180^{a)}$	≈ 3	Aligned array	[271]
Thermocapillary-enabled purification (TcEP)	Molecular resist	$\approx 100\%$ s-SWCNTs (contact based)	10^3 – 10^6	$>1000^{a)}$	5 – 150	Aligned array	[118–120]
	Heating source (electrical or electromagnetic)	$\approx 85\%$ s-SWCNTs (non-contact based)					

^{a)}These mobility numbers use rigorous C_C calculations that consider the density of s-SWCNTs.^[22,182] ^{b)}Calculated μ_{FE} from I_D – V_{GS} characteristics measured at $V_{DS} = 1$ V. All other values use I_D – V_{GS} measured at a lower V_{DS} of ≤ 0.1 V.

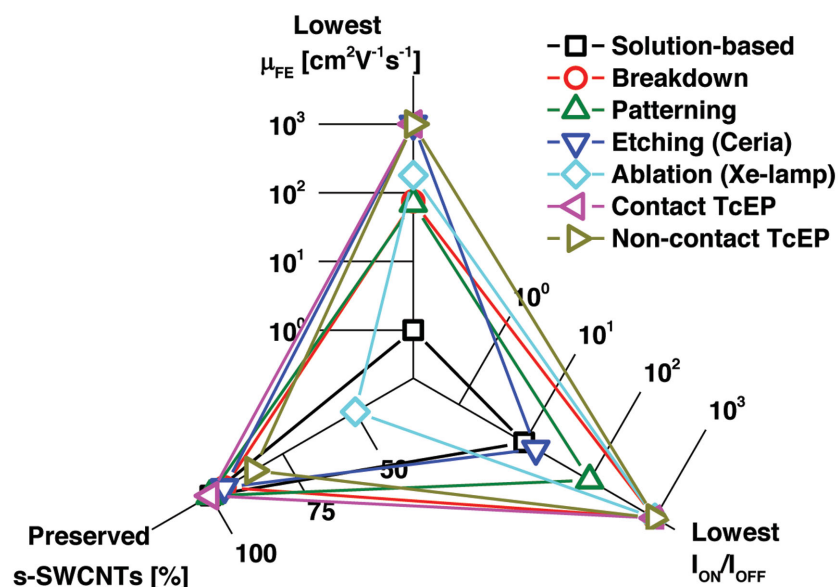


Figure 25. Comparison of three key parameters associated with different post-processing methods. Solution-based sorting uses results from refs. [27,81,197,223,229]. The breakdown data uses results from ref. [83]. The patterning data uses results from ref. [34]. The etching data uses results from growth on ceria catalyst supports, which have active oxygen for in situ etching of m-SWCNTs.^[106] The ablation data uses results from Xe-lamp irradiation.^[270] TcEP data uses results from refs. [118,120]. Except for the pattern removal method, μ_{FE} and I_{ON}/I_{OFF} ratios are obtained from transistors having aligned arrays of SWCNTs as the channel. To compare μ_{FE} for different methods, one should consider its L_{CH} dependence, as discussed in the text.

s-SWCNTs and result in transistors with low field-effect mobility and on-current. For transistors that use networked SWCNTs as the channel, the post-processing method with SWCNT removal using striped or hollow patterns is promising; on the other hand, for transistors with aligned arrays of SWCNTs as the channel, TcEP shows the best potential. Obtaining a cost-effective and scalable process that maximizes transistor parameters such as high on/off ratio and mobility with reduced device-to-device variability is a general target for practical application of all the proposed methods.

With these advanced methods for s-SWCNT purity improvement, s-SWCNT can compete effectively with the recently proposed two-dimensional (2D) materials as potential replacements for low-performance materials like amorphous silicon, polycrystalline silicon, and organic materials for applications in flexible electronics, transparent electronics, and flat-panel displays. The utility of high I_{ON}/I_{OFF} ratios and μ_{FE} using s-SWCNTs in biosensors or chemical sensors is unclear, as the performance parameters for these sensors are mostly limited by the diffusion and capture of biomolecules or chemical molecules.^[280] The s-SWCNTs

have no dangling bonds, surface states and, in contrary to 2D materials, they have no grain boundaries,^[281,282] which make them ideal for these applications. However, in addition to high purity s-SWCNTs, these applications will also demand predictable and highly uniform transistor performance via precise control of current conduction, threshold voltage, contact resistance, hysteresis, and sub-threshold (off-state to on-state) switching. All these outcomes can be ensured with s-SWCNTs that have a narrow diameter distribution, a suitable dopant, and a high density. The presented post-processing methods can achieve such diameter distribution, although at an expense of s-SWCNT density and, hence, will require the use of additional methods^[27,64] for density improvement. To overcome use of any post-processing, the development of in situ methods with adequate control on heterogeneous catalysis is desirable, which will enable growth of s-SWCNTs with a narrow diameter distribution at a high density. Successful further development of approaches to high purity s-SWCNTs with the added feature of controlled s-SWCNT doping offers the prospect to reignite the excitement for high-performance electronic applications of s-SWCNTs as a replacement of silicon.

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