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Materials and Fabrication Processes for Transient and Bioresorbable High-Performance Electronics

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Materials and fabrication procedures are described for bioresorbable transistors and simple integrated circuits, in which the key processing steps occur on silicon wafer substrates, in schemes compatible with methods used in conventional microelectronics. The approach relies on an unusual type of silicon on insulator wafer to yield devices that exploit ultrathin sheets of monocrystalline silicon for the semiconductor, thin films of magnesium for the electrodes and interconnects, silicon dioxide and magnesium oxide for the dielectrics, and silk for the substrates. A range of component examples with detailed measurements of their electrical characteristics and dissolution properties illustrate the capabilities. In vivo toxicity tests demonstrate biocompatibility in sub-dermal implants. The results have significance for broad classes of water-soluble, "transient" electronic devices.

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1. Introduction

Implantable biomedical components serve critically important roles in modern clinical medicine. Such devices can be classified into two types: those that exist for long periods of time, typically designed to be permanent; and those that disappear, or resorb, in the body after they provide some useful function. The former includes both simple, passive devices such as artificial joints and pins,[1] as well as sophisticated electronic components such as deep brain electrical stimulators,[2] cardiac pacemakers[3] and programmable drug delivery systems.[4] The latter, by contrast, is currently available only in the form of passive elements such as resorbable sutures[5,6] or matrices for drug release,[7,8] degradable intravascular stents[9,10] and resorbable plate-screw systems.[11] An unaddressed technology opportunity, then, exists in biodegradable devices that are capable of active electronic processing, sensing, communication and/or actuation within or on the surface of the body. Envisioned uses range from non-antibiotic appliques designed to reduce the incidence of surgical site infections, to electrical stimulators that can accelerate bone growth, to systems that can release drugs at programmed intervals. In each case, the devices operate only over some finite period of time, typically defined by a healing process; afterward, they resorb to eliminate unnecessary device load without surgical intervention.

Initial, early technical work toward this type of technology yielded two examples of partially resorbable devices, in the sense that certain, but not all, of the component materials resorb. One involves ultrathin electrodes and/or transistors built on films of silk fibroin, engineered to facilitate conformal contact with biological tissues, as demonstrated in electrocorticography,[12] or to disperse thin, miniaturized electronic components in ways that minimize adverse body responses, as demonstrated in sub-dermal implants.[13] The other uses organic or bio-organic semiconductors with polymer dielectrics/substrates to yield systems in which all components except for the electrodes and interconnects dissolve in bio-fluids, in a potentially biocompatible manner.[14,15] Although the modest properties of known organic electronic materials limit the performance that can be achieved, this approach has some potential for devices that require only simple functions. A recent report describes

materials and schemes that bypass constraints associated with these two previous directions.[16] The result is a fully resorbable, high performance class of electronics, where ultrathin sheets of semiconductor-grade monocrystalline silicon (i.e., silicon nanomembranes, or Si-NMs) serve as the active materials, inorganic dielectrics (e.g., MgO, SiO_2) and conventional metals (e.g., Mg) provide the other electronic functions, and silk forms the substrate and encapsulation layers. Enabled devices encompass nearly all of the key building blocks for integrated circuits, ranging from metal-oxide semiconductor field-effect transistors (MOSFETs) to pn junction diodes, resistors, inductors and capacitors. Additional demonstrated components include solar cells, photodetectors, strain and temperature gauges, inductive power delivery systems and others. Although initially conceived for bioresorbable devices and demonstrated in programmable non-antibiotic bacteriocidal appliqués, this same technology can be more generally considered as a physically transient form of electronics, capable of disappearing via controlled physical or chemical change with well-defined rates. Non-biological applications include environmental sensors that avoid the need for recovery and collection after use, and consumer devices that minimize costly and hazardous disposal procedures.

A disadvantage of the original embodiment of this class of transient electronics is that many of the fabrication steps occured on a transient substrate (e.g., silk), thereby constraining significantly the temperatures, lithographic techniques, solvents and other aspects of the processing. These limitations prevent the use of manufacturing techniques that serve as the basis for high volume, low cost production of commercial silicon integrated circuits. The work described here establishes a silicon wafer-based strategy to fully formed transient circuit components and circuits, in configurations that allow their subsequent, and separate, integration with transient substrates and packaging materials. The results are important because they have the potential to enable realistic manufacturing strategies for transient electronics, in which only modest modifications to microelectronic fabrication facilities are needed. The concepts rely on the combined use of a specialized type of silicon on insulator (SOI) wafer and the techniques of transfer printing. The resulting devices involve constituent materials that all have some solubility in water: silicon, silicon dioxide, magnesium oxide, magnesium and silk. The following describes the concepts and demonstrates their use in fabrication of various electronic components and simple logic gates, with studies of their transient behaviors both through in vitro investigations of the kinetics and in vivo evaluations of biocompatibility and resorption.

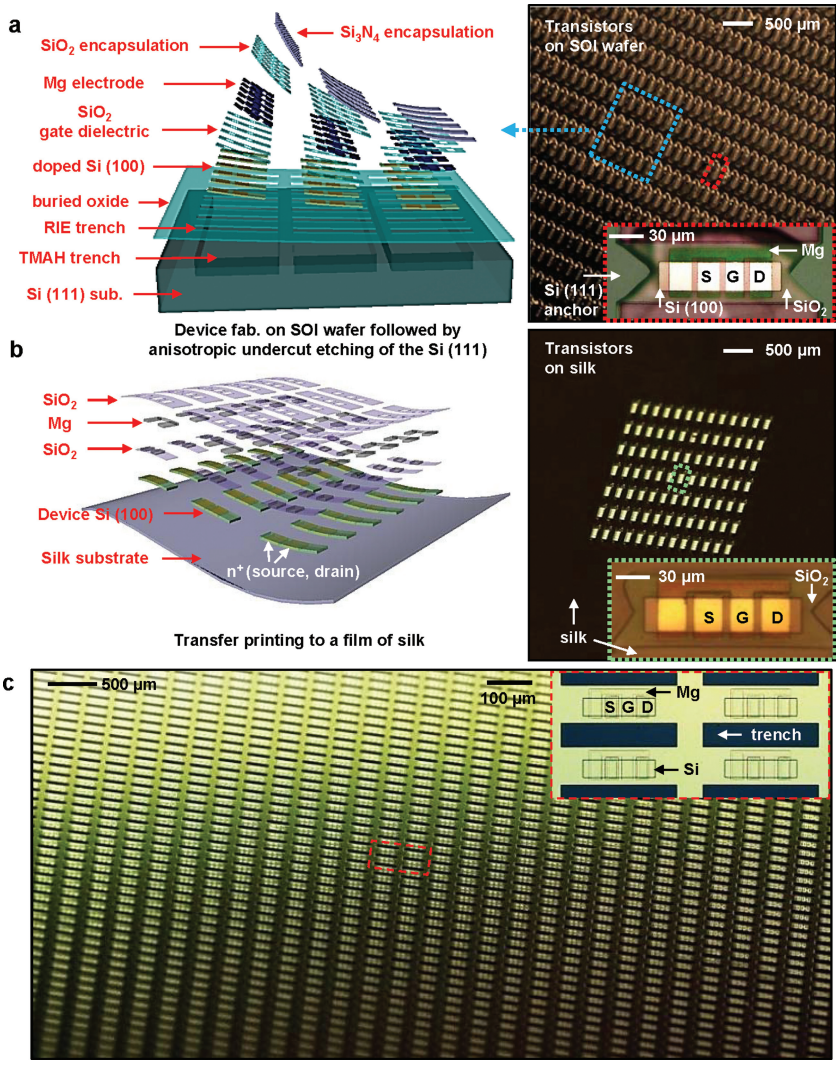

Figure 1. Wafer-scale fabrication of fully formed transient transistors on specialized SOI substrates and their subsequent transfer printing to films of silk. a) Schematic exploded view illustration and optical microscope images of devices after complete processing followed by anisotropic undercut etching of the surface region of the SOI wafer substrate with TMAH. The inset shows a magnified view of an individual transistor in the array. b) Schematic illustration and image of these same devices after transfer printing to a film of silk. The inset shows a magnified view of an individual transistor. The device uses magnesium (Mg; ≈200 nm) for source, drain and gate electrodes, silicon dioxide (SiO_2) for the gate (≈100 nm) and interlayer (≈100 nm) dielectrics, silicon (Si) for the semiconductor (≈100 nm) and silk for the substrate (≈25 μm). c) An optical image of a large area of n-channel MOSFETs, with microscope image of a representative set of devices in the inset.

2. Results and Discussion

The overall scheme involves complete fabrication of circuits and/or circuit components in transient materials on a silicon wafer, followed by their controlled release and subsequent integration onto a transient substrate via transfer printing. **Figure 1** presents exploded-view schematic illustrations and

optical micrographs of a representative system composed of a large-scale array of transient n-channel monocrystalline silicon metal-oxide field-effect transistors (MOSFETs), undercut etched from a SOI (111) wafer on which they were formed (Figure 1a) and after their transfer to a thin sheet of silk as a substrate (Figure 1b). The SOI wafer consists of ultrathin top layer of Si (p-type, ≈100 nm) with (100) orientation for the active regions of the devices, a buried oxide layer (≈1 μm) and supporting wafer with (111) orientation. The orientation of the wafer plays a critical role in the release of devices from its surface, as described in the following. Fabrication begins with high temperature, patterned doping (phosphorous at ≈950 °C) of the top Si to define the channel regions and contacts for the MOSFETs. Patterned etching of the silicon creates isolated regions for each of the devices. A coating of SiO_2 (≈100 nm) deposited by plasma-enhanced chemical-vapor deposition (PECVD) at 250 °C forms the gate dielectric. Etching in buffered oxide etchant (BOE, 6:1, Transene Company, USA) creates windows for source and drain contacts. Depositing Mg (≈200 nm) by electron beam evaporation yields source, drain and gate electrodes aligned to the contacts and channel areas (Supporting Information Figure S1a). Sequential PECVD steps define encapsulation layers of SiO_2 (≈100 nm thick; patterned to expose the source, drain, and gate contacts) and Si_3N_4 (≈400 nm thick; uniform across the entire area). Deep etching through a hard mask of Cr/Au (10/200 nm) establish trenches between the devices, down to a depth of ≈1.5 μm into the (111) silicon supporting wafer (Supporting Information Figure S1b). Anisotropic wet etching of the underlying (111) silicon with tetramethyl ammonium hydroxide (TMAH, 25 wt% in H_2O, Sigma-Aldrich, USA; 30 min at 100 °C) leaves free-standing MOSFETs tethered to the wafer at their ends by bridging films of the buried oxide (Supporting Information Figure S1c). Cross-sectional images in Supporting Information Figure S1d illustrate that the undercut proceeds in the (110) direction, along the surface of the wafer, to allow efficient release. Details appear in Supporting Information Figure S2. Free-standing MOSFETs created in this manner have total thicknesses of <2 μm, including the buried oxide layer (≈1 μm). Because the SOI substrates and processing conditions are compatible with state-of-the-art commercial microelectronics fabrication facilities, dramatic reductions in the thicknesses and lateral dimensions are possible.

Figure 1b illustrates an array of such MOSFETs after release from the SOI substrate and integration onto a film of silk, using the techniques of transfer printing.[17] A reactive ion etching (RIE; SF_6) step removes the Si_3N_4 after transfer. The buried SiO_2 and top coating of PECVD SiO_2 physically isolate the devices from their surroundings, thereby enabling performance that is nearly independent of substrate or subsequent encapsulating material. This versatility is important, particularly in an area such as transient electronics where choices of constituent materials can be highly unusual compared to those with proven utility in conventional electronics. Figure 1c demonstrates that these types of MOSFETs can be fabricated and transferred over large areas, with high yields.

Figure 2 provides a set of images collected during dissolution of a system like that illustrated in Figure 1c, at various times after immersion in deionized (DI) water at room temperature. Here, the silk rapidly dissolves within two minutes,

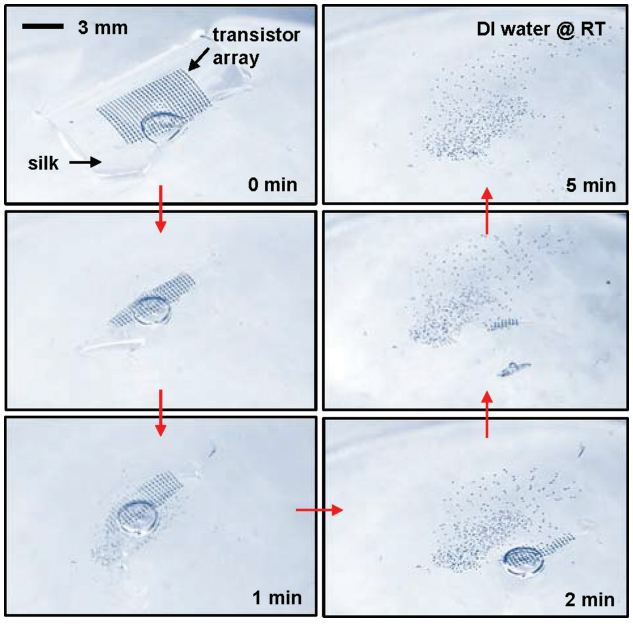

Figure 2. Optical images at various stages of disintegration and dissolution of an array of fully formed transient transistors on film of silk. These n-channel MOSFETs have total thicknesses of <2 μm, including a base layer of thermal SiO_2 (≈1 μm), and use Mg for the electrodes, SiO_2 for the gate dielectric and Si for the semiconductor. This process of dissolution occurs in DI water at room temperature.

thereby leading to disintegration of the array into individual devices. The rate of dissolution of silk can be controlled over a wide range.[18,19] Each component then gradually disappears in a manner defined by the dissolution rates of the various constituent materials.[16] Hydrolysis consumes the Mg in several hours ($Mg + 2H_2O \rightarrow Mg(OH)_2 + H_2$). Dissolution of PECVD SiO_2 and Si in PBS solution (pH 7.4) at room temperature occurs on a timescale of weeks ($SiO_2 + 2H_2O \rightarrow Si(OH)_4$; $Si + 4H_2O \rightarrow Si(OH)_4 + 2H_2$); the thermal oxide takes considerably longer. In all of the materials, the rates for complete disappearance depend strongly on temperature, pH, layer thicknesses and morphology.

The overall fabrication process accommodates not only individual MOSFETs, but also logic gates and small-scale integrated circuits. **Figure 3**a shows an array of inverters, with a magnified optical micrograph and a circuit diagram. Each inverter consists of a load and an input transistor with channel lengths and widths of ≈20 μm and ≈10 μm, and ≈10 μm and ≈40 μm, respectively. The fabrication procedures (Figure 3b) are similar to those described previously, including device isolation (top left), metallization (Mg evaporation, top middle), trench etching (bottom left), anisotropic undercut release (bottom right). A scanning electron microscope (SEM) image and a top view optical microscopy image appear in the bottom middle and top right frames, respectively. Supporting Information Figure S3 summarizes additional details. Electrical measurements on typical n-channel MOSFETs (channel length and width, L_{ch} = ≈10 μm, W = ≈40 μm) indicate on/off ratios of >≈10^5, saturation and linear regime mobilities of ≈530 cm^2/V s and ≈650 cm^2/V s, respectively (Figure 3c). Current-voltage

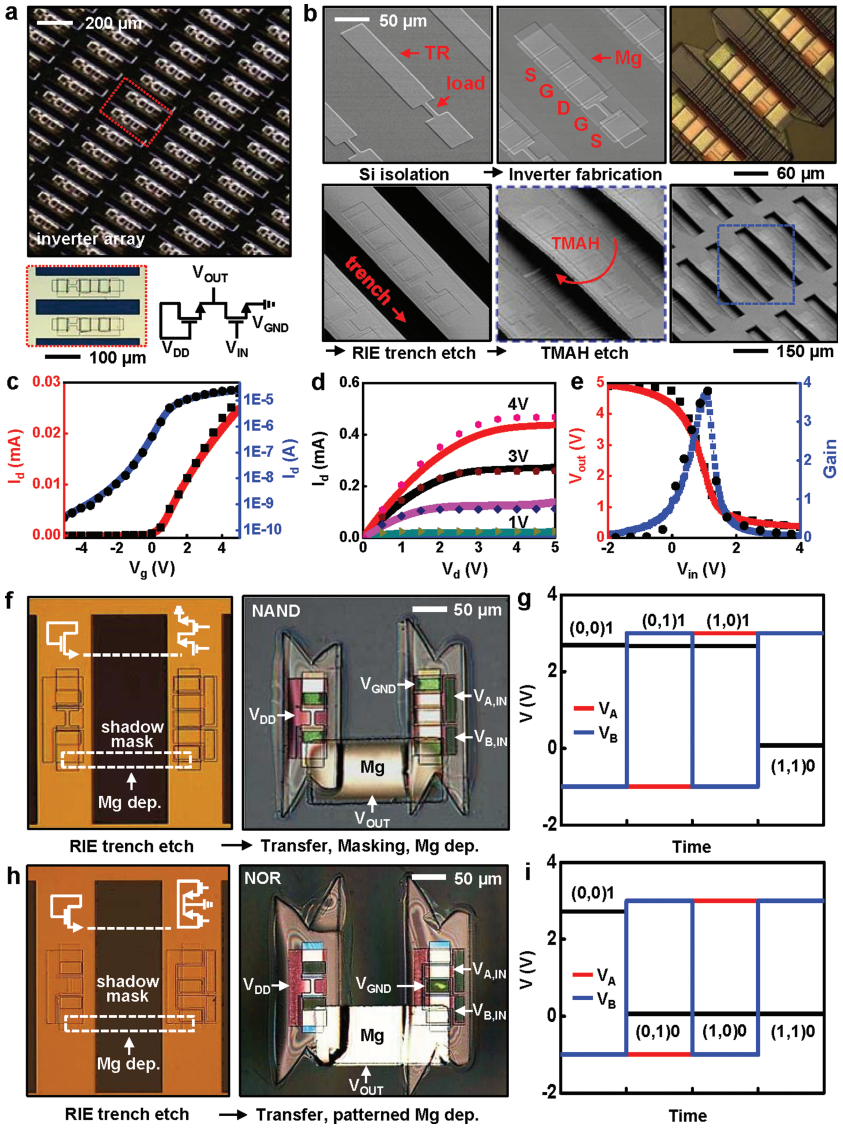

Figure 3. Fabrication of arrays of transient inverters and logic gates and their electrical properties. a) Image of an array of inverters, optical microscope image of a representative device (lower left) and circuit diagram (lower right). b) SEM and optical microscope images of key steps in the fabrication sequence. Device isolation (upper left), metallization (upper middle), RIE trench etch (lower left), anisotropic undercut etch with TMAH (upper right, lower right), and magnified image (lower middle). c) Linear (red) and log scale (blue) transfer curves of an n-channel MOSFET (channel length (L_{ch}) and width (W) are 10 μm and 40 μm, respectively). The mobility and on/off ratio are 650 cm^2/V s, and $>10^5$, respectively. Experimental results (lines) and simulations (dots). d) *I–V* characteristics of an n-channel MOSFET. e) Output voltage characteristics and voltage gain of an inverter (L_{ch} and W are 20 μm and 10 μm for load transistor and 10 μm and 40 μm for input transistor, respectively). The peak gain is ≈4. f) Demonstration of a pair of n-channel MOSFETs in a logic gate (NAND) formed by interconnection with Mg. When one or both of the input transistors (at V_A or V_B) are in their off state, the associated resistance of the input exceeds that of the load transistor, thereby leading to an output voltage in the "1" state. When the input transistors are turned on, the output voltage reaches the "0" state. Images after RIE trench etch (left) and after transfer and interconnection on a silk substrate (right). Circuit diagrams appear in the top regions of the images on the left. g) Output voltage characteristics of logic gates (NAND) at V_{DD} = 3 V. V_A and V_B represent input voltages. h) Images of a NOR circuit after RIE trench etching (left) and interconnection with Mg via deposition through a shadow mask after transfer printing a pair of n-channel transistors onto a silk substrate (right). The configuration of a NOR gate is similar to a NAND gate except for the connection of the input transistors. Here, parallel connection of the input transistors leads to an output state of "0", when either input is turned on. The output voltage can reach the "1" state only when both input transistors are turned off. i) Output voltage characteristics of NOR circuits at a supply voltage of 3 V (V_{DD}), with input voltages of V_A and V_B.

characteristics evaluated at different gate biases are shown in Figure 3d. Voltage transfer characteristics (VTC) of the inverters (Figure 3e) are consistent with expected behaviors, and gains of up to ≈4 at supply voltages of ≈5 V when the input voltage is swept from –2 V to 4 V (measured values (lines) and simulations (dots)). Behaviors in the transistors and circuits were verified by SPICE (Simulation Program with Integrated Circuit Emphasis) simulation. Here, the devices were modeled using a combination of parameters, such as channel width and length, gate oxide capacitance, carrier mobility, and channel length modulation, that yielded a good match with the measurements. The circuits were simulated based on the resulting device models. The observed electrical properties are comparable to those of devices reported previously, fabricated in a similar manner with conventional, non-transient materials.[20] Circuit components with increased sophistication are possible either through extended processing on the wafer, or through the use of interconnect structures formed after transfer printing. See Supporting Information Figure S4 for fabrication details. Examples of NAND and NOR gates appear in Figure 3f and 3h, respectively. Figure 3g,i show output voltage characteristics of NAND and NOR circuits. V_A and V_B are the input voltages. In case of the NAND gate, the output voltage assumes the "0" state when both input transistors are turned on. Output voltages for the "0" state and "1" state are ≈0.07 V and ≈2.67 V, respectively. For the NOR gate, output voltages reach the "1" state when both input voltages are low. Output voltages for the "0" state and the "1"state are ≈0.06 V and ≈2.7 V, respectively.

Inverters left in a released state on the SOI wafer allow for close examination of the dissolution processes. The image and schematic illustration in **Figure 4** provide detailed information on the device structure and material components: Mg (≈200 nm) for the electrodes, Si (≈100 nm) for the active layer, and SiO_2 (≈100 nm) for the gate and interlayer dielectrics. Upon immersion in phosphate buffered saline (PBS, pH 7.4, Sigma-Aldrich, USA) solution at physiological temperature (37 °C), the various components of the device begin to dissolve, beginning with Mg, which undergoes reactive dissolution (i.e., hydrolysis) to $Mg(OH)_2$ during the first 10 h. Although PECVD SiO_2 (≈100 nm, interlayer dielectrics) encapsulates most of the Mg electrodes, after the exposed Mg at the contacts (source, drain, and gate) dissolves, the solution is able to undercut the Mg that lies

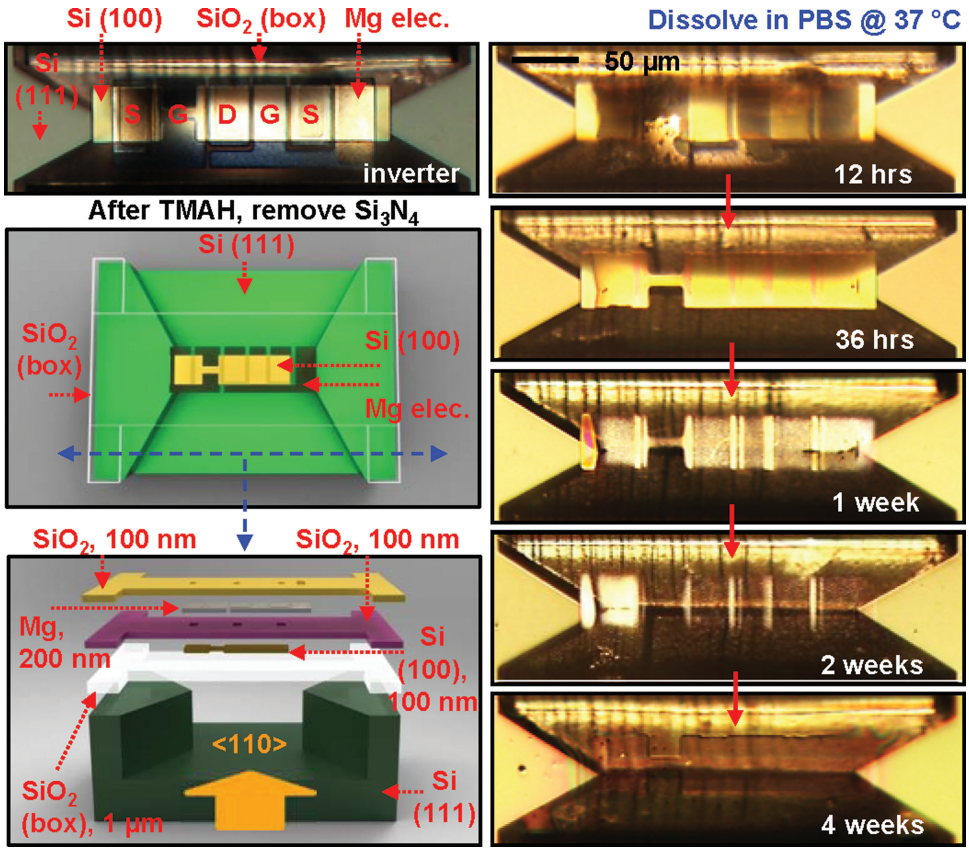

Figure 4. Schematic illustrations and time sequence of optical micrographs during dissolution of a transient inverter undercut etched but tethered at its ends to a Si wafer substrate, at various times of immersion in a phosphate buffered saline (PBS) solution at physiological temperature (37 °C) and pH (≈7.4). The frames in the middle and lower left provide schematic exploded view illustrations. The constituent materials include Si (100) with a thickness of ≈100 nm for the semiconductor, Mg (≈200 nm) for the electrodes, and SiO_2 (≈100 nm) for the gate and interlayer dielectric.

beneath the SiO_2. This etching induces cracks in the SiO_2 that start from the edges and propagate to the center regions. This type of disintegration accelerates the overall rate of disappearance of the PECVD SiO_2. After these top two layers mostly disappear, the SiO_2 gate dielectric (≈100 nm) begins to dissolve, reaching completion in two weeks or so. Over the next several weeks, the Si dissolves to form $Si(OH)_4$, with completion of this process in under 4 weeks. Consistent with previous reports of conventional acqueous etching approaches for silicon,[21] the detailed rates can depend strongly on dopant type and concentration, on temperature, and on composition of the bath. The results shown here are for silicon derived directly from the SOI substrates, without additional doping. After disappearance of silicon, only the thermally grown buried oxide (≈1 μm) remains, with dissolution rates that are many times slower than any of the other materials. A similar time sequence of images of interconnected arrays of logic gates on silk substrate appears in Supporting Information Figure S5.

Control over the kinetics of this transience behavior, and in particular of the effects on electrical properties, is an important aspect of any practical design. The most straightforward strategies involve patterned or uniform encapsulation layers, with thicknesses and compositions selected to define desired timescales for penetration of solution into the active regions. **Figure 5** shows, as an example, changes in electrical characteristics of MOSFETs and inverters encapsulated by MgO (≈800 nm) as a function of time of immersion in DI water at room temperature. The measured transfer curves (at a drain voltage V_d = 0.1 V) and drain currents (V_d = 0.1 V, and at a gate voltage V_g = 5 V) in Figure 5a indicate that the device properties are stable (i.e., time invariant) for the first ≈8 h before they degrade quickly over the next ≈45 min. The calculated mobility appears in Supporting Information Figure S6. A typical inverter, with key characteristics summarized in Figure 5b, shows similar behavior: stable properties for the first ≈7 h followed by rapid degradation within ≈50 min. Both cases exhibit two different stages in the transient behavior: i) stable operation for a time defined by removal of the transient encapsulation layer and ii) functional degradation with a timescale set by dissolution of the transient active materials. Tuning and programming of transience behavior using this strategy and more complex variants of it provide many options in design.[16]

Animal studies to examine biocompatibility were conducted by implanting a representative device in a Balb/c mouse in accordance with institutional IACUC-approved protocols as shown in **Figure 6**. In this example, the implant consisted of an array of resorbable transistors fabricated on a ≈5 mm × 5 mm silk film, sterilized by ethylene oxide and then inserted subcutaneously through an incision on the back of the mouse (Figure 6a, left). Here, the silk was treated in a manner that

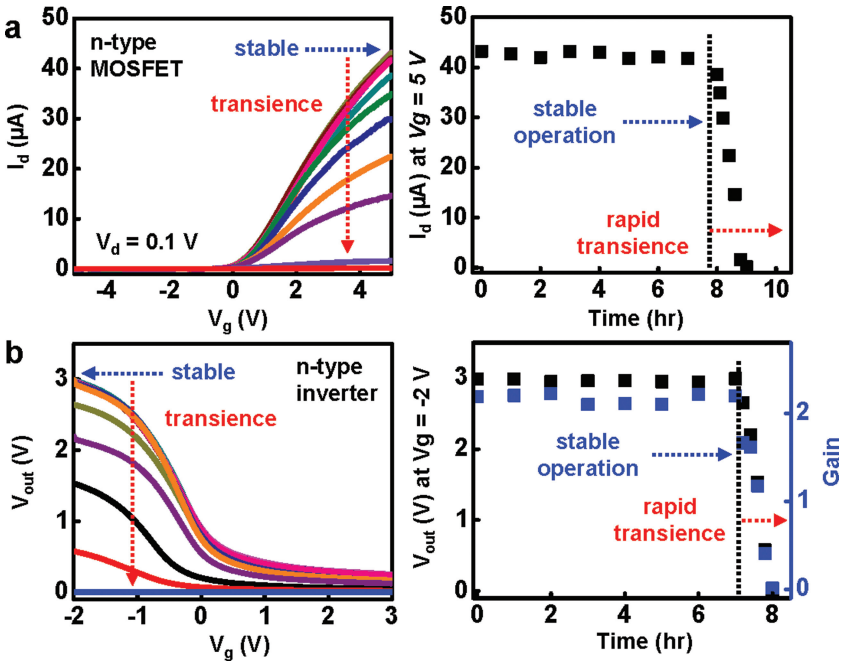

Figure 5. Study of the change in electrical properties of transient devices measured at various times during dissolution. a) Electrical properties of a representative n-type MOSFET encapsulated with MgO (≈800 nm) measured at various times during immersion in DI water at room temperature. The linear scale transfer curves (left), and the drain current (V_d = 0.1 V, V_g = 5 V) show that the properties are invariant for ≈8 h. Afterward, the performance degrades completely within ≈1 h. b) Measured characteristics of an n-channel inverter encapsulated with MgO (≈800 nm) at different times in DI water at room temperature. Voltage transfer characteristics (left), and output voltages at V_g = –2 V and gain (right) measured during dissolution. The device operation is stable for ≈7 h, followed by rapid degradation in ≈50 min.

leads to slow dissolution, thereby facilitating examination of the charcteristics of device resorption. The end of the functional life of the system is defined by disappearance of the encapsulation layer and/or substrate. After two weeks, the implanted sample (Figure 6a, right) was found to be nicely integrated into the surrounding tissues with no signs of magnesium or silicon. The device was retrieved and the surrounding tissue was extracted to determine the inflammatory response. Histological examination of the tissue surrounding the implant site revealed the absence of any severe inflammatory response, indicating that the implanted devices induced no significant adverse effects to the animal (Figure 6b).

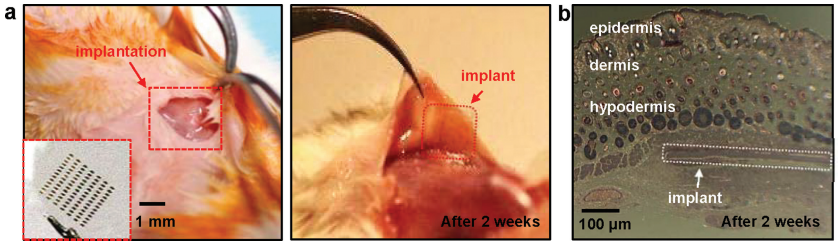

Figure 6. In vivo evaluation of biocompatibility. a) Image of the subcutaneous implantation of a representative device, consisting of an array of transistors on a sheet of silk, in the dorsal region of a BALB/c mouse. b) Image of the implant site after 2 weeks, showing that the implant integrated into the surrounding tissues with no signs of the transistors. c) Histological examination of the tissue surrounding the implant site reveals no inflammatory response.

3. Conclusions

The concepts, materials and fabrication techniques reported here provide a wafer-based approach to transient electronics, in which a set of foundry-compatible processing steps creates arrays of transistors, logic gates and potentially other components made of transient materials on a host wafer. The resulting device configurations are well suited for transfer printing onto transient substrates. Various examples illustrate the feasibility of this approach, and the levels of performance that can be achieved. These ideas have the potential to accelerate the translation of biodegradable electronic implants and other classes of devices enabled by transient circuits, sensors and/or actuators, into realistic, practical technologies. Different applications demand different functional lifetimes. The wide range of relevant timescales creates many opportunities for future work on materials, devices and packaging designs.

4. Experimental Section

Wafer-Based Fabrication of Fully Formed Transient Electronic Devices: The fabrication began with custom silicon-on-insulator (SOI, Silicon Quest Inc., USA) wafers with a top silicon (100) layer (≈2 μm thick, p-type 10–20 Ω·cm), a buried layer of silicon dioxide (≈1 μm thick) and a Si (111) supporting substrate. Repetitive cycles of dry oxidation at 1100 °C followed by wet chemical etching in hydrofluoric acid reduced the thickness of the top silicon layer to ≈100 nm. Patterned doping with phosphorous at ≈950 °C using a spin-on dopant (SOD, Filmtronics, USA) defined regions for source and drain contacts. Isolated areas of silicon were defined by patterned reactive ion etching (RIE; Plasmatherm, USA) with sulfur hexafluoride (SF_6) gas for ≈1 min. A thin layer of SiO_2 (100 nm) deposited by plasma-enhanced chemical vapor deposition (PECVD) served as the gate dielectric. Patterned wet-etching of this layer with buffered oxide etchant (BOE, 6:1, Transcene company, USA) opened windows for source and drain contacts. Photolithography and liftoff formed Mg electrodes (≈200 nm) for source, drain and gate contacts. An additional layer of PECVD SiO_2 (100 nm) served as an encapsulant, with openings to the contacts formed by immersion in BOE. A 400 nm thick, unpatterned layer of Si_3N_4 deposited by PECVD passivated the entire area of the devices. A bilayer of Cr/Au (10/150 nm) deposited by electron beam evaporation provided a hard mask for deep trench etching by RIE down to the underlying Si (111) wafer through the buried oxide. These processed substrates were then submerged in tetramethyl ammonium hydroxide (TMAH, 25 wt% in H_2O, Sigma-Aldrich, USA) for ≈30 min at 100 °C for anisotropic undercut etching of the wafer. Removal of the metal hard mask followed this etching. Next, the devices were transfer printed to a spin cast film of silk, and the passivation layer of Si_3N_4 was removed by RIE. In the case of logic gates, such as NAND and NOR gates, interconnection traces of Mg were deposited through fine-line stencil masks (Kapton, 12.5 μm, Dupont, USA).

Dissolution Experiments: To observe dissolution of the constituent materials (Si, SiO_2 and Mg), a collection of undercut etched inverters on SOI were immersed in phosphate buffered saline (PBS, pH 7.4, Sigma-aldrich, USA) solution at 37 °C. Optical microscope images revealed the various stages of dissolution over the course of 4 weeks. Most of the Mg electrodes (≈200nm) react with water to form $Mg(OH)_2$ within 12 h; any residual remaining Mg dissappeared completely in 36 h. The exposed regions of Mg dissolved first, followed by undercut dissolution of those regions of Mg that lie beneath PECVD SiO_2. Simultaneously, the SiO_2 (≈100nm, interlayer dielectrics) also began to dissolve to form $Si(OH)_4$. Due to the elimination of the underlying Mg, much of this SiO_2 disintegrated into tiny pieces (not visible directly), thereby accelerating the elimination of this layer. The SiO_2 (≈100 nm) that forms the gate dielectric disappeared in 2 weeks. Partial dissolution of the Si occurred at the same time. Dissapearance of all materials except for the buried oxide (SiO_2, 1 μm) was complete within 4 weeks. Previous studies indicate that oxides grown at high temperatures have slow dissolution rates due to their morphology/density.[22]

Monitoring of electrical properties during dissolution was performed using transistors and inverters encapsulated by a uniform layer of MgO (800 nm). These devices were completely immersed in DI water, but configured with external probing pads to enable continuous mesurement. Experimental results illustrate two-stage dissolution kinetics: stable device operation, without changes in electrical characteristics, followed by comparatively fast degradation in key performance parameters. The duration of the first stage depends on the rate of dissolution of the encapsulation materials and/or penetration of water through them. The second stage is determined, primarily, by relatively fast dissolution of the Mg electrodes.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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