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Effect of variations in diameter and density on the statistics of aligned array carbon-nanotube field effect transistors

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This paper describes a systematic experimental and theoretical analysis of performance variations in transistors that use aligned arrays of single-wall carbon nanotubes (SWNTs) grown on quartz substrates. Theoretical models, calibrated using measurements on statistically relevant numbers of transistors that each incorporate an individual aligned semiconducting SWNT, enable separate examination of different contributors to measured variations in transistors that incorporate arrays of SWNTs. Using these models and associated experiments, we study the scaling of the statistics of key performance attributes in transistors with different numbers of incorporated SWNTs and reveal long-range spatial nonuniformities in the distributions of SWNT diameters as the main contributor to observed performance variability. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3692048]

I. INTRODUCTION

Aligned arrays of single-wall carbon nanotubes (SWNTs) represent the most promising way to incorporate SWNTs into established, planar semiconductor device technologies. Work toward this goal is motivated by the potential for exploiting the excellent properties of SWNTs (i.e., carrier mobility of $\sim 10^4$ cm^2/V-s,[1] transconductance of ~ 6 mS/μm, inferred on a per-tube basis[2]) as field-effect transistors (array-SWNT FETs) in high performance electronics, either alone or heterogeneously integrated with otherwise conventional silicon or compound semiconductor circuits. Advanced growth strategies, which yield aligned array SWNTs by chemical vapor deposition growth on substrates such as quartz, have enabled devices with operating speeds in the GHz range,[3] and even integrated systems such as radio frequency (RF) electronics,[4–6] transparent electronics,[7,8] etc. In spite of these successes, such aligned arrays of SWNTs include a mixture of metallic and semiconducting nanotubes with some variations in diameters[9–11] and local densities[12] (measured as the number of SWNTs per unit length perpendicular to their alignment direction) that depend in a complex way on the size/composition[13,14] (yielding diameter variation) and placement[13] (yielding density variation) of the SWNT catalyst, and details of the growth conditions. Such variations lead directly to spatial nonuniformities in the electronic properties of array-SWNT FETs,[12,15,16] even when the contribution from metallic nanotubes are eliminated chemically[17] or electrically[18] or with clever circuit designs.[19]

Understanding the variability in array-SWNT FETs requires detailed knowledge of the intrinsic sources of this behavior (i.e., variations in diameter and density of SWNTs across the wafer, as opposed to variations that might arise due to nonideal aspects of device processing). One approach is to perform a combined experimental and theoretical study of the consequences of these variability sources on device performance. Such study involves *measuring* diameter and density variations across the wafer on which FETs are made, *establishing* insights at the microscopic level (e.g., diameter dependence of SWNTs' electronic properties using FETs with single SWNTs[20]), and then *propagating* the effects to macroscale device embodiments (FETs with several SWNTs) following "inferential statistics"[21] – *three basic steps* that are often neglected in literature.[12,15,16] Previous studies conclude that variability in device properties, which arise from diameter variations, are expected to diminish as the number of SWNTs in an individual device increases, due simply to statistical averaging,[9,12,16] making SWNT density variation as one of the major contributors to performance variations.[12] Such statistical averaging, however, might not occur in this manner, because density and diameter distributions over entire substrate areas ("population" distributions) are not necessarily the same as those determined in small-scale evaluations ("sample" distributions), a well-known aspect of "inferential statistics."[21] Our previous effort[15] to understand the implications of this system-level variation in diameter and density distributions is applicable only to short-channel FETs, because the analysis ignored diameter dependent conductance in SWNTs, which is important in the operation of long-channel length FETs.[1]

In this paper, we perform a comprehensive analysis of performance variation in array-SWNT FETs, consisting of

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SWNTs grown on stable temperature (ST) cut quartz substrates, by following the three steps mentioned above. The work enables quantitative assessment of contributions from diameter and density variations to the behavior of FETs with single SWNTs and large-scale arrays of them. We first experimentally calibrate a theoretical model for operation of single-SWNT FETs, and then use it to capture the effects of diameter variation on performance parameters such as drain current, transconductance, and threshold voltage. The resulting model allows quantitative propagation of variability in properties of single SWNT FETs to array-SWNT FETs. The results suggest that "population" and "sample" distributions in density and diameter are different, such that variability in performance of array-SWNT FETs decreases more slowly with increasing numbers of incorporated SWNTs than expected based on the effects of statistical averaging alone.

II. PERFORMANCE VARIABILITY IN ARRAY-SWNT FETs

Figure 1(a) shows a schematic illustration of an array-SWNT FET and a scanning electron microscope (SEM) image of an aligned array of SWNTs (fabrication details in Sec. III) that forms the channel of the FET. The drain current ($I_{D,ARRAY}$) versus gate voltage (V_G) characteristics (measured using a sweep from $+V_G$ to $-V_G$) of three nominally identical (i.e., same physical dimensions, electrodes, and dielectric materials) array-SWNT FETs [Fig. 1(b)] illustrate the level of variation in device performance that can be observed. The low ON/OFF ratios are consistent with the presence of metallic SWNTs in the arrays. We define the threshold voltage (V_T) as the value of V_G at minimum drain current (I_{MIN}) and separate the effects related to variations in V_T by evaluating distributions of drain current at a fixed value of V_G-$V_T \sim -1$ V. Figure 1(c) plots this drain current (referred as I_{ON}) distribution for array-SWNT FETs having $\langle N \rangle \sim 11$ SWNTs, where $\langle N \rangle = \langle \rho \rangle W$ is nominal number of SWNT within the FET, W is the channel width, and $\langle \rho \rangle$ is the average density of SWNTs on the substrate. We divide standard deviation of $I_{ON}/\langle N \rangle$ (σ_{ION}) by $\sqrt{\mu_{ION}}$, where μ_{ION} is the average of $I_{ON}/\langle N \rangle$, to compensate for the effect of variation in μ_{ION} [Supplemental Fig. 1(a)].[42] (The variation in μ_{ION} potentially reflects variation in sample preparation for array-SWNT FETs of different W made on different wafers. To compensate for the effect of such μ_{ION} variation in the calculated σ_{ION}, we use the fact that the average is proportional to the square of the standard deviation for Poisson statistics, as seen for $I_{ON}/\langle N \rangle$ distributions in Supplemental Figs. 1(b)–1(f),[42] and divide σ_{ION} by $\sqrt{\mu_{ION}}$.) Calculated $\sigma_{ION}/\sqrt{\mu_{ION}}$, normalized with respect to the value measured for FETs with single SWNT, shows only a small reduction as $\langle N \rangle$ increases [Fig. 1(d)]. If the distribution of diameter and density for each array-SWNT FETs (sample distribution) were same as the substrate-level distribution (population distribution) of these parameters, then the normalized standard deviation would be expected to decrease as $1/\sqrt{\langle N \rangle}$ (Supplemental Fig. 2),[42] by consequence of the central limit theorem.[21] Deviation from this expected behavior suggests significant variations in SWNT density and/or diameter at the device-level across the substrate. Studies involving extensive atomic force microscopy (AFM) at different locations over a macroscopic area of a typical quartz substrate with as-grown arrays of SWNTs reveal spatial variations in density (ρ) and mean diameter (μ_d). These properties, along with the standard deviation of the diameter distribution (σ_d), appear in Figs. 2(a)–2(c), respectively. The results clearly

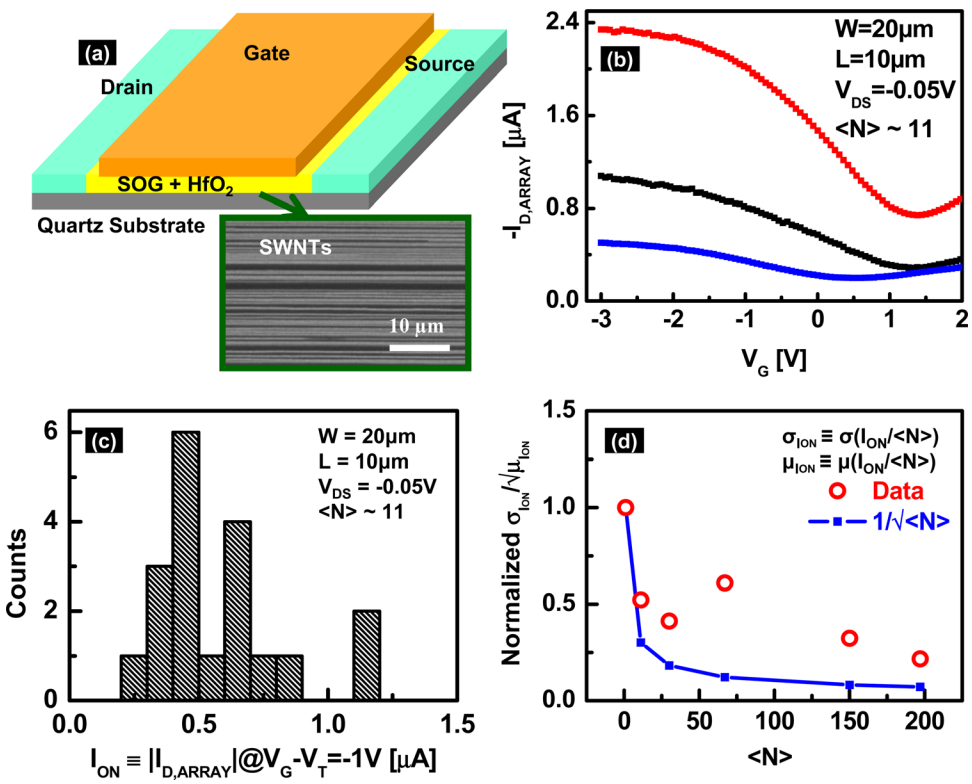

FIG. 1. (Color online) (a) Schematic illustration of a top-gated array-SWNT FET with source/drain electrodes of Ti/Pd, gate dielectric of spin-on-glass(-SOG)/Hafnium oxide(HfO_2) and gate of Ti/Au. Aligned arrays of SWNTs (inset) serve as the channel. (b) Drain current ($I_{D,ARRAY}$) vs gate voltage (V_G) characteristics for three array-SWNT FETs with channel length L=10 μm, on a substrate that has an average density of SWNTs of $\langle \rho \rangle \sim 0.55/\mu$m, corresponding to an average number of SWNTs per device of $\langle N \rangle \sim 11$. (c) Distribution of I_{ON} among M = 19 array-SWNT FETs with $\langle N \rangle \sim 11$, where M is the sample size for the distribution. (d) Comparison of normalized $\sigma_{ION}/\sqrt{\mu_{ION}}$ (with respect to its value for $\langle N \rangle = 1$) at different $\langle N \rangle$ and the $1/\sqrt{\langle N \rangle}$ scaling (expected based on the central limit theorem). Here, σ_{ION} and μ_{ION} are the standard deviation and average of $I_{ON}/\langle N \rangle$, respectively.

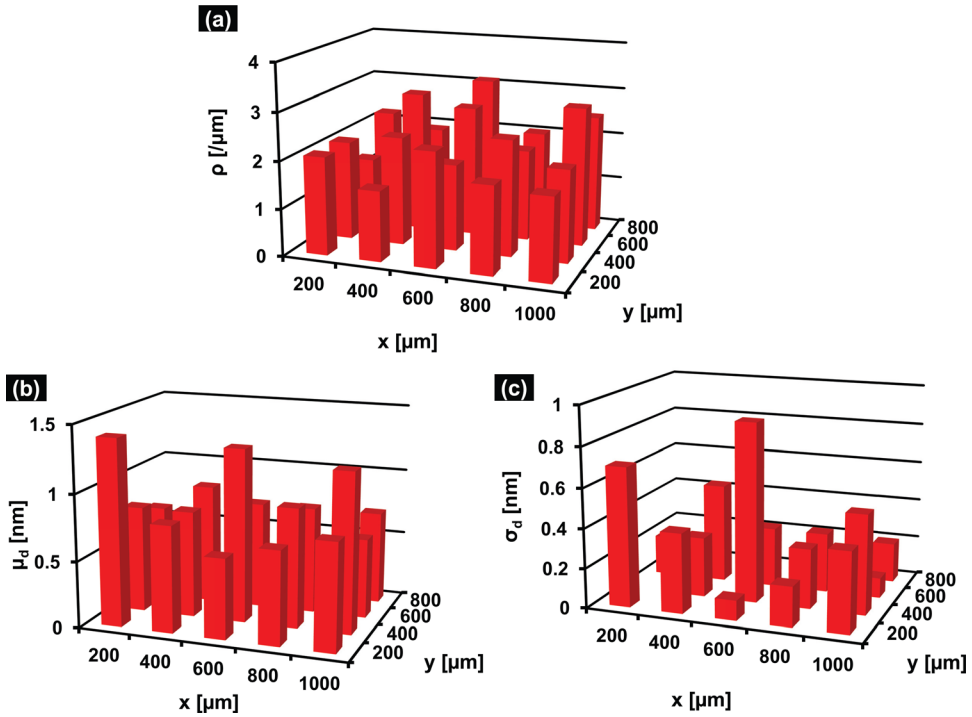

FIG. 2. (Color online) Representative spatial distribution of key properties of arrays of SWNTs grown on a ST-cut quartz substrate: (a) density (ρ), (b) average diameter (μ_d) and (c) standard deviation of diameter (σ_d), determined by analysis of 20 atomic force microscope images; each image has a spatial extent of 20 μm in the direction perpendicular to the SWNT alignment direction (y) and 1.25 μm in the orthogonal direction (x).

suggest spatial variation in "sample" distributions at the substrate-level.

Figure 3 summarizes the procedure for studying the variability in performance of array-SWNT FETs. The diameter dependence of electrical parameters (shown in Sec. IV and Figs. 5 and 6), measured and simulated for FETs built with single semiconducting SWNTs (SS-SWNT FET), enables simulation of $I_{D,ARRAY}$-V_G for M different FETs by using the following steps (red box in Fig. 3):

(1) Randomly choose a value for ρ from the measured distribution [Fig. 2(a)] and calculate the number of SWNTs (N) in the array-SWNT FET using $N = \rho W$.
(2) Randomly choose a mean diameter μ_d and standard deviation σ_d from the measured distributions [Figs. 2(b) and 2(c)] and calculate the diameter distribution, $f(d)$, for the array-SWNT FET.
(3) Obtain the distribution of $I_{D,SS}$-V_G for SS-SWNT FETs, i.e., $f(I_{D,SS}\text{-}V_G)$, using $f(d)$ and the diameter dependence of the $I_{D,SS}$-V_G characteristics [Fig. 5(b)]. Here, $I_{D,SS}$ is the drain current for SS-SWNT FET.
(4) Randomly select N current-voltage characteristics, $(I_{D,SS}\text{-}V_G)_i$ (where $i = 1,\ldots,N$), from $f(I_{D,SS}\text{-}V_G)$ and then calculate $I_{D,ARRAY} - V_G = \sum_{i=1}^{N} (I_{D,SS} - V_G)_i$.
(5) Repeat steps 1–4 M times to obtain the distribution of $I_{D,ARRAY}$-V_G for array-SWNT FETs.

Simulations of M different array-SWNT FETs of width W yield $\langle N \rangle$ SWNTs, on average, with associated distributions of I_{ON} and maximum transconductance ($G_{M,MAX}$). Figure 7 shows normalized standard deviations of I_{ON} (σ_{ION}) and $G_{M,MAX}$ (σ_{GM}) for different $\langle N \rangle$ and their comparison to measured quantities. Although the simulation framework for these devices (Fig. 3) neglects contributions from metallic SWNTs, the procedure is suitable for present purposes, i.e., to highlight the importance of system-level variations in diameter and density, thereby explaining the deviation from central limit theorem's expectations for σ_{ION} [Fig. 1(d)] and σ_{GM}.

III. FABRICATION DETAILS

Fabrication of array-SWNT FETs starts with the growth of aligned SWNTs via chemical vapor deposition (CVD) on a ST-cut quartz substrate using procedures described elsewhere.[22] Definition of source and drain electrodes (2 nm Ti/60 nm Pd) occurs by electron beam deposition (Temescal FC-1500) onto the substrate in regions defined by photolithography. Etching the SWNTs in regions outside the channel by O_2 plasma (Plasma Therm; 100 mTorr pressure, 20 sccm flow, 100 W RF power) through a photolithographically defined mask isolates the devices. The gate dielectric consists of a film of spin-on-glass (Filmtronics; siloxanes 215 F; 35 nm thick, measured using Gaertner L116 C Ellipsometer) deposited by spin-coating 10:1 solution of isopropyl alcohol and spin-on-glass, then baking it sequentially at 85 °C for 1 min, 155 °C for 1 min, 255 °C for 1 min, 72 °C for 30 min to enhance planarization, and finally curing it at 375 °C for 1 h. A capping layer of hafnium dioxide (HfO_2; 20 nm) formed by atomic layer deposition (Savannah 100, Cambridge Nanto Tech Inc.) at 120 °C using H_2O and $Hf(NM_2)_4$ (99.99+%, Aldrich) reduces the gate leakage current for the fabricated FETs. Electron beam deposition and photolithography defines the top gate metal (2 nm Ti/60 nm Au). Removal of the HfO_2 and spin-on-glass from regions of the source/drain contact pads defined by photolithography, using concentrated HF completes the process. The equivalent oxide thickness (EOT)[23] of the resultant top-gated FET is ~40 nm (calculated by using the dielectric constant of 3.7

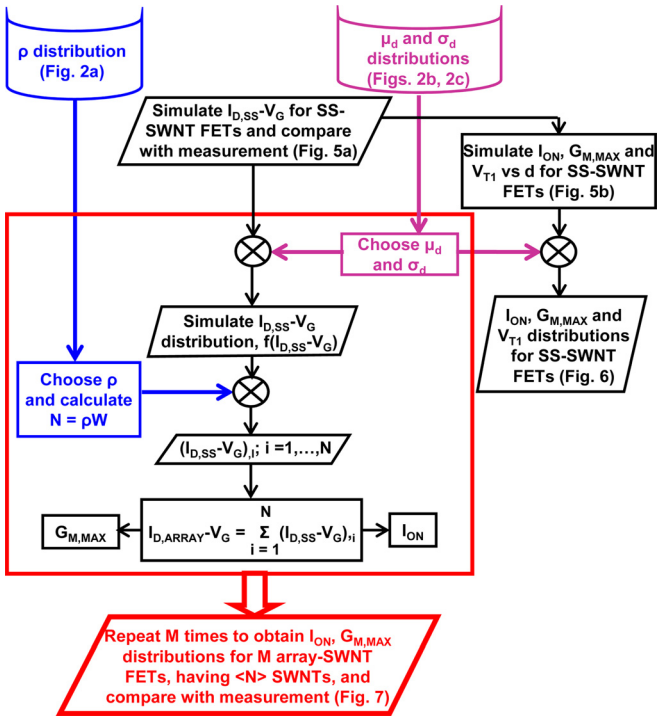

FIG. 3. (Color online) Flow chart that illustrates procedures for studying the statistics of M different array-SWNT FETs having width W and average number of SWNTs $\langle N\rangle = \langle\rho\rangle W$. Here, N is the number of SWNT in an individual array-SWNT FET, $I_{D,SS}$ is the drain current for FETs with single semiconducting SWNT (SS-SWNT FET), $G_{M,MAX}$ is the maximum transconductance, V_T is the threshold voltage for array-SWNT FET defined as $V_G@(I_{D,ARRAY} = I_{MIN})$, V_{T1} is the threshold voltage for SS-SWNT FET defined as $V_G@(I_{D,SS} = I_{MAX}/100)$, I_{MIN} is the minimum drain current for any FET, and I_{MAX} is the drain current at $V_G = -1.5$ V for SS-SWNT FET.

for SOG,[24] 25 for HfO_2[23]). The channel length (L) for all devices is ~10 μm.

Fabrication of FETs with single SWNTs (Supplemental Fig. 3)[42] uses procedures identical to those described above for array-SWNT FETs. An additional step involves removal of SWNTs everywhere except for a narrow strip (~1.5 μm) defined by photolithography in the channel region. SEM imaging allows identification of FETs with single SWNTs. The yield of working FETs containing single SWNTs is ~3%.

IV. FETS WITH SINGLE SWNT

A. Measurement

Figure 4(a) shows a SEM image of a FET, taken before deposition of gate dielectric and gate, to illustrate a single SWNT bridging the source and drain. Measurements of drain current versus gate voltage characteristics of 45 such FETs can be sorted according to semiconducting [Supplemental Fig. 4(a)][42] or metallic [Supplemental Fig. 4(b)][42] behavior, based on their ON/OFF ratios ($= I_{MAX}/I_{MIN}$; where, I_{MAX} is the drain current at $V_G = -1.5$ V and I_{MIN} is the minimum drain current). SS-SWNT FETs show predominantly *p*-type behavior, as expected for Pd source/drain contacts.[25] By contrast, SM-SWNT FETs (i.e., FETs with single metallic SWNT) have ambipolar characteristics, perhaps due to the presence of Mott-insulating state[26] and/or strain-induced bandgap.[27] Figure 4(b) presents I_{MAX} vs I_{MIN} for all measured FETs and shows M = 25 SS-SWNT FETs with ON/OFF ratios greater than ~100. Noise associated with the experimental setup limits measurable I_{MIN} to values greater than ~0.1–1 pA. Figure 5(a) shows $I_{D,SS}$ vs V_G-V_{T1} for a few representative SS-SWNT FETs, where the threshold voltage for SS-SWNT FET (V_{T1}) is defined as the gate voltage at $I_{MAX}/100$.

B. Modeling of SS-SWNT FET

We model the source-to-drain conductance (G_{DS}) of a SS-SWNT FET as a combination of the conductance of the semiconducting SWNT (G_{SS}) and the conductance of the SWNT/Pd contact (G_C), i.e. $G_{DS}^{-1} = G_{SS}^{-1} + G_C^{-1}$ and calculate $I_{D,SS}$ at different V_G using -

$$I_{D,SS} = G_{DS} * V_{DS}. \quad (1)$$

Since the conduction through SWNT is due to a combined flow of electrons in the conduction band and holes in the valence band, G_{DS} at any gate bias will be –

$$G_{DS} = G_{DS,e} + G_{DS,h} = (G_{SS,e}^{-1} + G_{C,e}^{-1})^{-1} + (G_{SS,h}^{-1} + G_{C,h}^{-1})^{-1}. \quad (2)$$

Calculation of G_{SS} and G_C at different V_G uses

$$V_G = E_{Fi} + Q_{SS}/C_G, \quad (3)$$

where $E_{Fi} = E_i - E_F$, E_i is the intrinsic Fermi level of the semiconducting SWNT or the midgap energy level of graphene, E_F is the Fermi energy level of the semiconducting SWNT, $C_G = 1/[(2\pi\varepsilon_{SiO2}/\ln(1 + 2*EOT/d))^{-1} + C_Q^{-1}]$ is the gate capacitance, ε_{SiO2} is the dielectric constant of SiO_2, C_Q

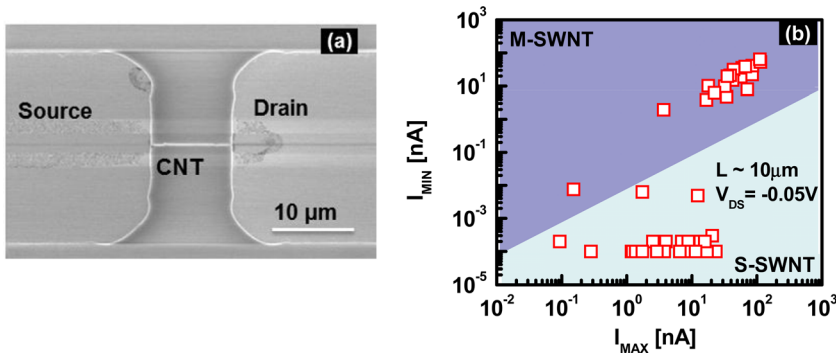

FIG. 4. (Color online) (a) SEM image of a FET with a single SWNT (taken before depositing the gate dielectric and gate metal). (b) I_{MIN} vs I_{MAX} for 45 FETs with single SWNTs. FETs with $I_{MAX}/I_{MIN} > 100$ are considered to incorporate semiconducting SWNT (S-SWNT), while the rest are defined as metallic SWNT (M-SWNT).

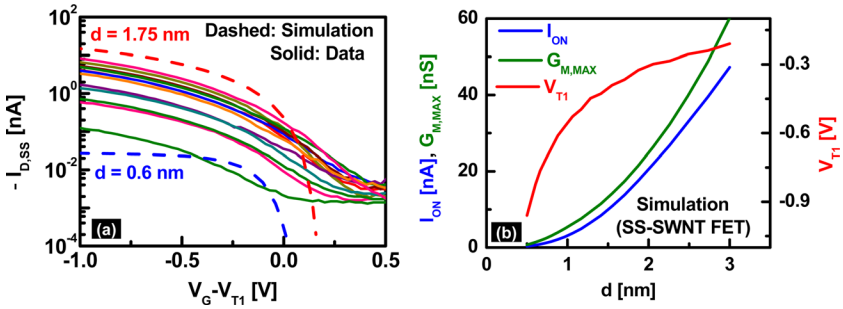

FIG. 5. (Color online) (a) Measured $I_{D,SS}$ vs V_G-V_{T1} ($V_{T1} \equiv V_G@I_{MAX}/100$) characteristics of SS-SWNT FETs ($L \sim 10\ \mu m$, $V_{DS} = -0.05$ V) is within the simulated results for $d = 0.6$ nm and $d = 1.75$ nm FETs. (b) Simulated I_{ON} ($|I_{D,SS}|@V_G\text{-}V_{T1} = -1$ V, $V_{DS} = -0.05$ V), $G_{M,MAX}$ ($\max(\partial I_{D,SS}/\partial V_G)$), and V_{T1} ($V_G@I_{D,SS} = I_{MAX}/100$) vs diameter for SS-SWNT FETs.

is the quantum capacitance, and Q_{SS} is the charge within the semiconducting SWNT that is expressed as[28] -

$$Q_{SS} = -q\int_{-\infty}^{\infty} dE * \text{sign}(E) * v(E) * F(\text{sign}(E) * (E - E_{Fi})), \quad (4)$$

where q is the electron charge, $v(E) = (4/\pi h v_F)(|E|u(E-E_{Fi})/\sqrt{E^2 - E_{Fi}^2})$ is the density of states of semiconducting SWNT, h is the Planck's constant, v_F is the Fermi velocity, F(E) is the Fermi distribution, sign (E) is the sign of energy level E, and $u(E)$ is the unit step function. Calculated Q_{SS} is later used to compute G_{SS} and G_C (Supplemental Sec. S1),[42] then G_{DS} using Eq. (2), and finally I_D using Eq. (1).

C. Simulation results: SS-SWNT FET

Supplementary Fig. 5[42] shows simulated $I_{D,SS}$ vs V_G-V_{T1} for SS-SWNT FETs with d between 0.6 and 3 nm using $v_F = 8 \times 10^5$ m/s,[1] $E_i \sim 4.7$ eV,[29] $\alpha = 80$ m/K-s, $G_{c0} = 1/28$ kΩ,[1] $C_Q = 4 \times 10^{-12}$ F/cm,[30] and T = 300 K. Simulated results at $V_G < V_{T1}$ (regions where $G_{DS} \sim G_{SS}$) are consistent with the measurements of Fig. 5(a) for 0.6 nm < d < 1.75 nm. The differences at $V_G > V_{T1}$ (regions where $G_{DS} \sim G_C$) reflect the fact that variations in G_{C0}[31] are not included in the simulation. Figure 5(b) plots the diameter dependence of $I_{D,SS}$ at V_G-$V_{T1} = -1$ V (I_{ON}), maximum transconductance $G_{M,MAX}$, and V_{T1} of SS-SWNT FETs. At large diameters, when the transmission of carriers through the Schottky barrier near the contact is unity, $I_{ON} \sim d$ and $G_{M,MAX} \sim d^2$ due simply to the expected diameter dependence of the mobility of semiconducting SWNTs.[1,32,33] By definition of V_{T1} ($\equiv V_G@\ I_{MAX}/100$), its diameter dependence follows the diameter dependence of I_{ON}. At small diameters, nonlinear behavior of the transmission through the Schottky barrier leads to a nonlinear dependence of I_{ON}, $G_{M,MAX}$, and V_{T1} with diameter.

With the diameter distribution of Fig. 6(a) as input, the results of Fig. 5(b) can be used to compute distributions of I_{ON}, $G_{M,MAX}$, and V_{T1} in collections of SS-SWNT FETs. The outcomes agree well with respective measurements [Figs. 6(b)–6(d)]. The observed distribution in V_{T1} - $\langle V_{T1}\rangle$ (where $\langle V_{T1}\rangle$ is the average of the distribution) is wider than the corresponding simulation, possibly due to the additional contributions from defects,[34,35] variations in the work function of the gate,[36,37] and adventitious doping of source/drain contacts.[38] The distribution in I_{ON} for SS-SWNT FETs [Fig. 6(b)] follows log-normal statistics, as does the diameter

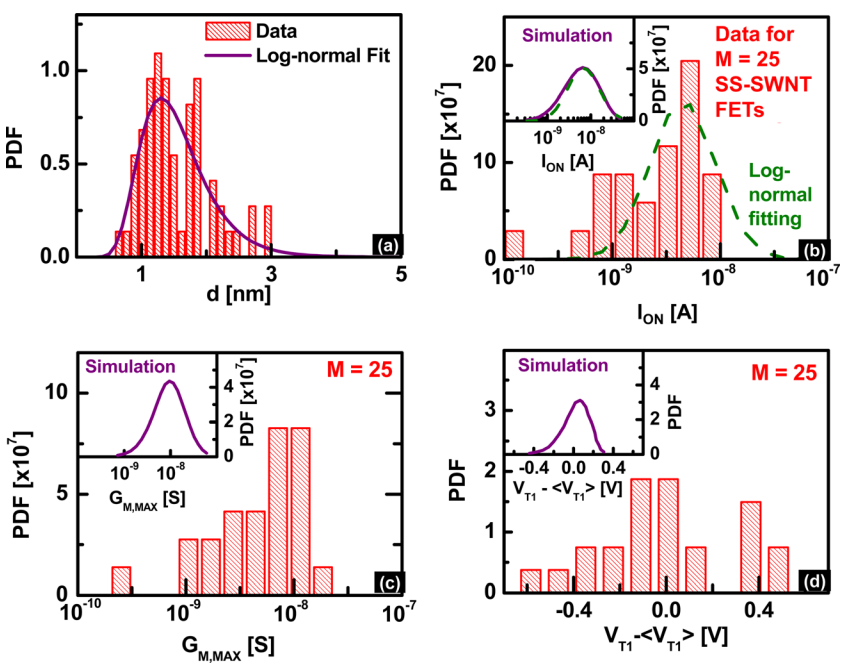

FIG. 6. (Color online) (a) Diameter distribution that is used to simulate performance distributions of SS-SWNT FETs. Measured distributions of (b) I_{ON}, (c) $G_{M,MAX}$, and (d) V_{T1} for SS-SWNT FETs agree well with the simulated distributions (insets). Measured and simulated I_{ON} distributions in (b) have longer negative tails (negative skewness) compared to the fitted log-normal distributions. For (d), $\langle V_{T1}\rangle$ is the average of the V_{T1} distribution.

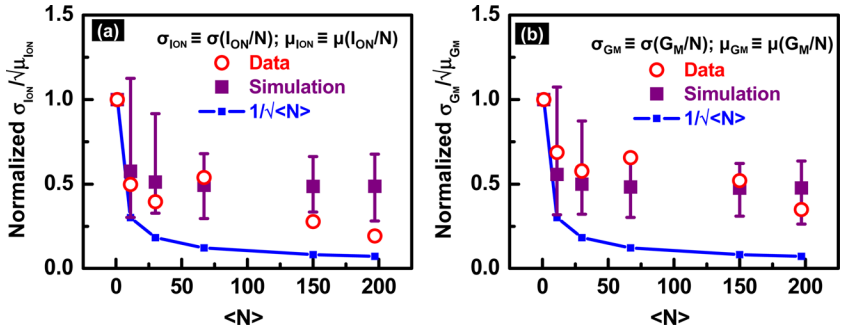

FIG. 7. (Color online) Normalized (a) $\sigma_{ION}/\sqrt{\mu_{ION}}$ and (b) $\sigma_{GM}/\sqrt{\mu_{GM}}$ calculated from measured $(I_{D,ARRAY}/N)$-V_G characteristics (open circles) differs from $1/\sqrt{<N>}$; M = 19, 20, 20, 35, 17 array-SWNT FETs for <N> = 11, 30, 67, 150, 197, respectively are used to calculate σ_{ION}, μ_{ION}, σ_{GM}, and μ_{GM}. Plots also show simulated quantities (filled squares), where variations in density [Fig. 2(a)] and diameter distributions [Figs. 2(b) and 2(c)] are considered. The error bars suggest variation among 500 calculations of simulated standard deviation in M = 20 array-SWNT FETs.

distribution [Fig. 6(a); $I_{ON} \sim d$], except near the lower tail of the distribution where transport through the Schottky barrier dominates the current. These behaviors suggest that narrowing the distribution of I_{ON} (hence performance distribution of array-SWNT FETs) might be possible by reducing the Schottky barrier width with decreased oxide thickness,[39] as explored in Sec. V.

V. ARRAY-SWNT FETS: ANALYSIS

Using experimentally calibrated SS-SWNT FET results as input, the steps of Fig. 3 yield simulated $I_{D,ARRAY}$-V_G characteristics of array-SWNT FETs, as well as standard deviations σ_{ION} and σ_{GM} for comparison with the measured quantities. In calculating these standard deviations both from simulated and measured $I_{D,ARRAY}$-V_G, we eliminate the effect of SWNT density variation by counting N for each array-SWNT FET and then using $(I_{D,ARRAY}/N)$-V_G characteristics for the standard deviation calculation. Counting N for each FETs allows the complete elimination of effects of density variation (see Supplemental Fig. 6 for effectiveness of this approach),[42] but even in this case the calculated σ_{ION} at different $\langle N \rangle$ (normalized to its value for $\langle N \rangle = 1$) still shows significant deviation from $1/\sqrt{\langle N \rangle}$ scaling [Fig. 7(a)]. Such deviation suggests that SWNT density variation is a minor contributor to performance variation.

Next, we append the diameter variations of Figs. 2(b) and 2(c) within the simulation and observe excellent agreement with the measurement both for normalized σ_{ION} [Fig. 7(a)] and σ_{GM} [Fig. 7(b)]. One additional aspect of simulated standard deviations is noteworthy for such comparison: the total sample size for statistical analysis is modest. For example, we measured current-voltage characteristics of M = 19, 20, 20, 35, and 17 array-SWNT FETs for $\langle N \rangle \sim$ 11, 30, 67, 150, 197 SWNTs, respectively, to calculate the standard deviations. To analyze the effect of such small sample size, we also simulate the standard deviations for M = 20 and observe variations from one simulation to another. Figure 7 shows the variation (using error margin) of simulated standard deviations for 500 different calculations, together with measured data. (Variations in V_T ($\equiv V_G@I_{MIN}$) and I_{MIN} appear in Supplemental Fig. 7.[42] The distributions of these parameters are mainly related to the metallic SWNT populations. Standard deviations of these distributions reduce with increase in $\langle N \rangle$ due to statistical averaging. Since practical applications of array-SWNT FETs demand incorporation of only semiconducting SWNTs, we do not pursue a theoretical analysis of V_T and I_{MIN} here.)

We finally study the performance variation in small-scale array-SWNT FETs, involving small equivalent oxide thickness (EOT) and short channel length (L = 300 nm), by calibrating the simulation parameters with short-channel SS-SWNT FET measurements of Ref. 40 [Supplemental Figure 8(a)].[42] Decreasing the equivalent oxide thickness (EOT) reduces the width of the Schottky barrier of the SWNT/Pd-contacts[39] in these FETs and removes the nonlinear I_{ON} vs d relationship for small diameter semiconducting SWNTs [Supplemental Fig. 8(b)].[42] Moreover, I_{ON} vs d for these short-channel SS-SWNT FETs with channel lengths comparable to carrier mean-free paths in SWNT,[1,40,41] saturates at larger diameters. As a combined effect of Schottky barrier reduction for small diameter SWNTs and current saturation for large diameter SWNTs, the normalized standard deviation of I_{ON} for SS-SWNT FETs (with $\langle N \rangle = 1$) decreases with decreasing EOT [Fig. 8(a) and Supplemental Fig. 8(c)[42]]. However, at larger $\langle N \rangle$, EOT scaling cannot improve the statistics because the effects of variations in density and diameter become significant [Fig. 8(b)]. In this regime of behavior, improved

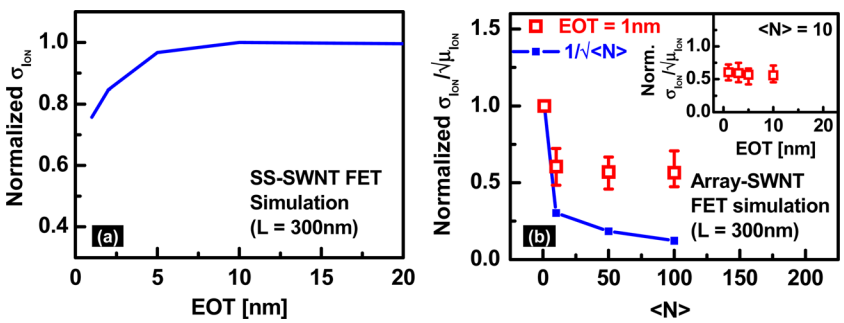

FIG. 8. (Color online) (a) Oxide scaling of SS-SWNT FET reduces σ_{ION} (normalized by its value at EOT = 20 nm). (b) Normalized $\sigma_{ION}/\sqrt{\mu_{ION}}$ (with respect to its value for <N> = 1) differs from $1/\sqrt{<N>}$ for array-SWNT FETs with EOT = 1 nm and show negligible effect of oxide scaling at fixed $\langle N \rangle$ (inset). Here, σ_{ION} and μ_{ION} are the standard deviation and average of I_{ON}/N, respectively.

procedures for achieving enhanced uniformity in the arrays of SWNTs appear necessary.

VI. CONCLUSION

We present detailed studies of performance statistics in FETs that contain single and multiple SWNTs in aligned array configurations. Experimental and theoretical understanding of FETs with single SWNT, along with separately measured variations in SWNT density and diameter, provides an ideal platform to examine variability in array-SWNT FETs. Our analysis suggests that although variations decrease with increasing numbers of SWNTs within the FETs, nonuniformities in density and diameter distributions across the substrate lead to deviations from expectation based on the central limit theorem. For the systems examined here, the performance variation is due largely to the distributions in SWNT diameters, thereby identifying this characteristic as an area for improvement that could be addressed with advanced growth and/or purification techniques.

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