Intrinsic Performance Variability in Aligned Array CNFETs

Shuaib Salamat, *Student Member, IEEE*, Xinning Ho, John A. Rogers, *Fellow, IEEE*, and Muhammad Ashraful Alam, *Fellow, IEEE*

***Abstract*—The I–V characteristic of carbon nanotube (CNT) transistors is dictated by the Schottky barrier (SB) at metal–nanotube interface. The SB is defined by the diameter of the CNT along with the source/drain metal and is presumed a device constant for single CNT transistors. Given the wide distribution of diameter of CVD-grown nanotubes, the presumption of single SB, however, is inappropriate for transistors with aligned array of CNTs. Indeed, array transistors with similar geometries and contact material can still exhibit considerable variation in threshold voltage (V_T), ON current ($I_{\rm ON}$), and device resistance (R_d). We use measured diameter distribution within the framework of detailed numerical simulations to demonstrate that the diameter distribution of CNTs (in CNT FETs) plays a dominant role in defining the fluctuation of array transistors. Besides, it is argued that the large-scale integration of these devices within an IC would be feasible only if the distribution of diameter is considerably narrowed.**

***Index Terms*—Aligned network transistor, carbon nanotube (CNT) FET (CNFET), diameter distribution, thin-film transistor (TFT).**

I. Introduction

As CARBON nanotube (CNT)-nanonet technology explores niche applications in micro [1]–[5] and macroelectronics [6]–[10], it is increasingly important to create transistors with nominally uniform characteristics as the basis for large-scale circuit integration. Studies based on *single tube* CNT FET (CNFET) have shown that among various transistor parameters, control of tube diameter is most critical because diameter dictates bandgap and injection barriers, and these two parameters in turn dictate (exponentially) the I–V characteristics of a transistor [11]. The question is: does diameter distribution play an equally important role in multitube transistors or does the self-averaging, over various tube diameters, obviate the problem? It is well known that in long-channel nanonet transistors, the sensitivity of the I–V characteristics on tube diameter is suppressed as electrons percolate through an "ensemble-averaged" network of tubes with various diameters [7], [12]. In short-channel aligned array CNFETs, however, such "path-averaging" may be absent and distribution of CNT parameters (e.g., diameter, mobility, etc.) could be directly reflected in the I–V characteristics. In principle, therefore, short-channel directly bridging CNFETs using similar device geometries could exhibit significant variation in the ON current, especially for ultrascaled transistors appropriate for high-frequency operation. While the role of the metal/nanotube contact and its effect on device performance for FET with single CNT has been studied by many groups [11], [13]–[16], the effect of diameter distribution (of CNT array) on FET performance parameters (e.g., $I_{\rm ON}$, V_T, R_d, and $I_{\rm ON}/I_{\rm OFF}$), especially in the presence of metallic CNTs (m-CNTs), has not been considered. In this paper, we use measured diameter distribution and transistor characteristics along with systematic theoretical simulations to demonstrate that, of all the parameters, intrinsic process-induced diameter distribution would continue to play a dominant role in dictating the performance of short-channel CNT transistors, even if the channel length was scaled to the ballistic limit. Given typical diameter distribution, we find that: 1) only a fraction of the tubes carry most of the current (i.e., larger diameter nanotubes, despite being relatively small percentage of the total number of tubes, carry a significant amount of current [$d_{\rm CNT} \sim 1/E_g$]) and 2) depending on the contact material (source/drain), a fraction of the semiconducting tubes behave essentially like metallic tubes (from OFF-state to ON-state) and must be removed for good $I_{\rm ON}/I_{\rm OFF}$ ratio.

II. Fabrication of Nanotube Arrays and Devices

As shown in Fig. 1, the thin-film transistors (TFTs) used in this study are based on perfectly aligned parallel array of single-walled CNTs (SWNTs) as the channel material. The SWNTs were grown directly into such configuration via CVD on a specially prepared quartz substrate, using the procedures described in our earlier study [17]. The devices studied here used palladium (Pd) for source and drain electrodes. Layers of hafnium oxide (HfO_2) deposited on top of the resulting structure formed the gate dielectric (94 ± 7 nm). Gold (Au) was used as the gate electrode. The gate was aligned to the channel and it overlapped significantly with both the source and the drain (by $\sim$20 μm).

Manuscript received July 15, 2009; revised January 11, 2010; accepted February 18, 2010. Date of publication March 29, 2010; date of current version May 11, 2011. This work was supported in part by NCN computational resources and Motorola Corporation. The work of S. Salamat and M. A. Alam was supported by the Motorola Corporation. The work of X. Ho was supported by the Agency for Science, Technology and Research (ASTAR), Singapore. Experimental work was carried out in part in the Frederick Seitz Materials Research Laboratory Central Facilities, University of Illinois, which were supported in part by the U.S. Department of Energy under Grant DE-FG02–07ER46453 and Grant DE-FG02–07ER46471. The review of this paper was arranged by Associate Editor C. Zhou.

S. Salamat and M. A. Alam are with Network for Computational Nanotechnology and Department of Electrical Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: ssalamat@ecn.purdue.edu; alam@ecn.purdue.edu).

X. Ho and J. A. Rogers are with Frederick Seitz Material Research Laboratory and Department of Material Science and Engineering, University of Illinois, Urbana-Champaign 61801 (e-mail: xho2@illinois.edu, jrogers@uiuc.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2010.2046674

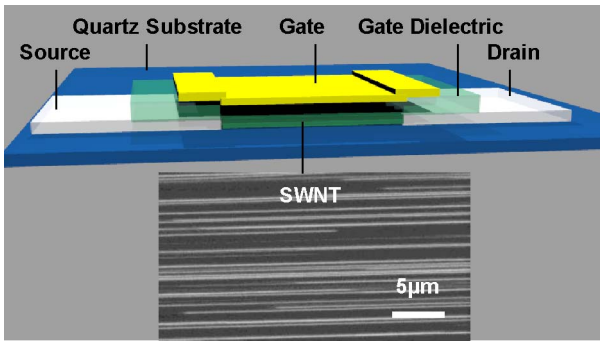


Fig. 1. Schematic illustration of TFT with perfectly aligned parallel array of SWNTs. Lower portion of the figure shows the scanning electron micrograph of a representative CNT array.

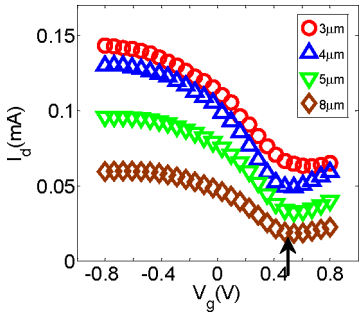


Fig. 2. Transfer curves of devices for channel lengths of 3, 4, 5, and 8 μm. Measurements were taken with the source grounded and the drain held at a bias of -0.01 V. Gate bias was swept between ± 0.8 V. Upward arrow on the bottom curve (corresponding to channel length of 8 μm) indicates V_T of this device.

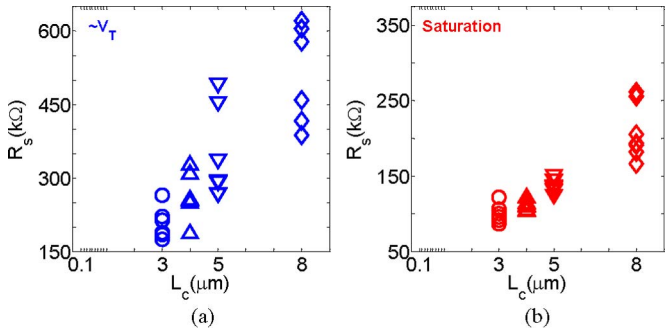


Fig. 3. (a) Resistance variations in the the semiconducting tubes measured at threshold voltage. (b) Resistance variations in the semiconducting tubes measured in saturation. All the devices had same contact material and the applied biases (gate/drain). Nonetheless, significant variations in resistance R_s were present for all channel lengths and were particularly large near V_T.

To study the transport characteristics, we fabricated six samples for each channel length of 3, 4, 5, and 8 μm (a total of 24 devices). The widths (W) of all the transistors were kept constant at 400 μm.

Fig. 2 shows typical transfer curves of one sample of each channel length. Consistent with the earlier reports [14], these Pd-contacted devices exhibited predominantly p-type characteristics.

Remarkably, however, even though all the devices were processed in parallel and used the same metallization scheme, Fig. 3 shows that the devices with the same channel length (e.g., 3 μm) exhibited significant variations in the $I_{\rm ON}$, V_T, and R_d. Here, $I_{\rm ON}$ is defined as drain current (I_d) at maximum applied gate bias (V_g) of -0.8 V, V_T is defined as the gate bias (V_g) at which I_d is minimum [18] (this definition is different from that of MOSFET, wherein V_T is traditionally defined by taking the point of maximum slope on I_d–V_g curve (or linear transconductance) and V_T is extracted by the intercept of the tangent through the point [19]), and R_d is the device resistance given by$R_d = V_{\rm ds}/I_{\rm ON}$ and it includes the resistance of semiconducting as well as metallic tubes. Given that the ratio of m-CNTs to semiconducting CNTs (s-CNTs) is $\sim$1:2, we associate $I_{\rm OFF}$ with transport through m-CNTs, and the difference of $I_{\rm ON}$ and $I_{\rm OFF}$ with transport through semiconducting tubes. The average resistance of each semiconducting tube can be calculated as $R_s = N_s \times V_{\rm ds}/(I_{\rm ON} - I_{\rm OFF})$, where N_s is the number of semiconducting tubes per device (determined from the density measurements of CNTs making up the transistor) and $V_{\rm ds}$ is the applied drain bias.

Fig. 3(a) and (b) summarizes the observed fluctuations in the average resistance of semiconducting tubes for various channel lengths measured at threshold and in saturation. These variations were present for all channel lengths (3, 4, 5, and 8 μm), and were particularly large around V_T [see Fig. 3(a)].

These results immediately bring into focus a number of issues regarding the variability in transistors' performance. It is conceivable that at longer channel lengths, extrinsic factors like mobility fluctuation, variability in the number of tubes able to bridge source and drain, length-dependent scaling of defects along the tube, etc. can potentially increase device-to-device fluctuation. If, however, we examine Fig. 3 along with Fig. 6, we notice that as the devices are scaled down, the *relative* fluctuation in resistance remains almost independent of channel length (especially if we examine Fig. 6(b), it is evident that channel lengths of 3, 4, and 5 μm exhibit similar experimental R_s variability that is within the extents of simulations). The aforementioned characteristic of "resistance variability" depicts the possibility that the fluctuation in devices' resistance may not be averaged out even at ultrascaled, quasi-ballistic channel lengths (<300 nm) [14] relevant for high-speed electronic applications. While fluctuation at the longer channel lengths may be amplified by extrinsic variability, there appears to be an irreducible intrinsic variability present in all array-based CNT transistors.

The aforementioned discussion leads one to the hypothesis that the distribution of diameters of CNTs may be the source of this variability and may play a more important role than is commonly appreciated. To verify this proposition, we first measured the diameter distributions of as-grown CVD SWNTs (before defining channel lengths and depositing gate dielectric) of four different samples using atomic force microscopy (AFM) (see Fig. 4). The diameters of CNTs were determined by measuring the height difference between top of CNT and substrate next to it (quartz) and approximately 600 measurements were taken to reduce statistical error. Fig. 4 shows that some of the

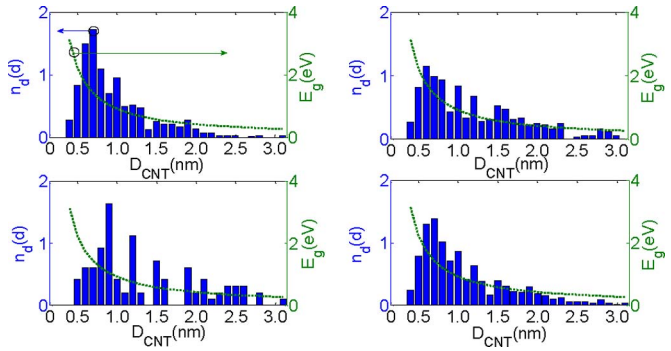


Fig. 4. Normalized diameter distributions for four samples. These measurements correspond to different TFTs that use perfectly aligned array of single-wall CNTs for the channel. The measurements were taken using AFM, on as-grown CVD tubes before defining the channel lengths and depositing the gate dielectric. We determined the diameter by measuring the height difference between the top of the CNT and the area just next to the CNT (i.e., quartz). The number of tubes on each device were different, therefore, the data has been normalized to highlight the general shape of diameter distribution in the CNFETs.

CNTs have diameter ∼0.4 nm. These very low values may reflect the resolution limit of our AFM setup. Nonetheless, the fraction of such tubes ($d_{\rm CNT} \leq 0.4$ nm) is very small and given their large E_g, these CNTs would have very little effect on device characteristics ($I_{\rm ON}$, R_d, etc). Also noted in Fig. 4 is that CVD-grown tubes exhibit a wide range of diameter distribution that cannot be represented by a simple distribution function, let alone by an average value [20]. In general, the exact shape of the diameter distribution would depend on the CNT growth technique and device processing details. For typical ranges of diameter distributions, the spread in transistors' characteristics can be significant, as discussed in the following.

III. Modeling of the Effect of Diameter Distribution on I–V Characteristics

Although I–V characteristics of CNFETs resemble that of a conventional MOSFET, however, the underlying physics of the two transistors is very different. Contacts in the conventional MOSFET are ohmic, but owing to the difficulty in making an ohmic contacts in CNFETs, the transport through CNFETs is thought to be dominated by Schottky barrier (SB) at the (contact) metal/CNT interface [1], [15], [21]–[23]. For short-channel CNFETs, experiments have shown that the metal–CNT contacts limit the current flow through CNT and determine the electrical characteristics of the device [21]. The SB at metal/CNT interface, however, is a function of the metal work function (Φ_m) and CNT diameter (or, equivalently E_g). If the metal work function is fixed, the diameter of CNT dictates the nature of the contact, i.e., SB or ohmic. In essence, if metal–CNT combination is such that the metal Fermi level contacts CNT inside the valence band (or conduction band), the contact will be ohmic; alternatively, if the metal Fermi level contacts CNT inside the bandgap, the contact will be SB. Many researchers have shown Pd to make an excellent ohmic contact with CNTs [14], [24]. Since our devices have aligned network of CNTs with wide range of diameter distribution, *some of the CNTs are likely to form SB, while remaining will make ohmic contact*.

The electronics structure of SWNTs strongly depends on their diameter and chirality [25]. The work function of SWNTs ($\Phi_{\rm CNT}$) would therefore, be different depending on the structure of CNT. Many studies have been conducted on the work functions of SWNTs [26], [27] and the values reported vary slightly depending on the method used for measurement. We used work function for nanotube $\Phi_{\rm CNT} = 4.7$ eV [28]. Since the bandgap (E_g) of CNT depends on the reciprocal of CNT diameter ($d_{\rm CNT}$) [29], [30], we calculated the E_g for each CNT using the relationship [31]

$$E_g = \frac{2|t|a_{c-c}}{d_{\rm CNT}}. \tag{1}$$

An overlap integral value of $|t| = 2.7$ eV is used in this study [29], [31], and with carbon-to-carbon bond length $a_{c-c} = 0.144$ nm, the aforementioned expression simplifies to

$$E_g \sim \frac{0.78 \text{ eV}}{d_{\rm CNT(nm)}}. \tag{2}$$

With $\Phi_{\rm CNT} = 4.7$ eV and $\Phi_{\rm Pd} = 5.1$ eV (Pd work function) [11], [14], the barrier for holes (Φ_P) is calculated using analytical expression

$$\Phi_P = \left(\Phi_{\rm CNT} + \frac{E_g}{2}\right) - \Phi_m \tag{3}$$

.

This relationship suggests that there would be no hole barrier (i.e., $\Phi_P = 0$) for CNTs with diameter equal to 1 nm, $d_{\rm CNT} \cong 1.0$ nm($E_g = 0.8$ eV), and there would be a positive SB (Φ_P) for holes for all nanotubes with diameters less than 1 nm, $d_{\rm CNT} < 1.0$ nm ($E_g > 0.8$ eV $\pm$ 3 kT). As seen in Fig. 4, in our devices there are many CNTs with diameter smaller than 1 nm. Hence, the transport in these CNTs will be dominated by SB. For all the CNT with diameter larger than 1 nm, $d_{\rm CNT} > 1.0$ nm ($E_g < 0.8$ eV $\pm$ 3 kT), there is no barrier for holes and metal/CNT contact will essentially be ohmic.

Given the barrier for holes (and electrons), metal, and CNT work functions and other parameters (drain/gate bias, oxide thickness, etc.), we can now calculate the current through the transistor using self-consistent numerical simulations [32]. As discussed earlier, in order to isolate the *intrinsic* effect of diameter distribution from other *extrinsic* effects, like charge trapping and mobility variation, (that might add to the drain current fluctuation in long-channel transistors), we focus on ballistic transport in very short channel transistor (100 nm) that is exclusively affected by contact metal and the diameter distribution of the tubes. Briefly, our numerical simulations involve solution of quantum transport equations (the standard nonequilibrium Green's function formulation), which are self consistent with the Poisson equation. Details of the simulation model have been discussed elsewhere [33].

Due to nearly ballistic nature of transport in short-channel CNFETs [14], the transistor performance is dictated by the SBs at the metal/nanotube interface and the s-CNTs' resistance (R_s) can be approximated by the contact resistance (R_c). For the long channel lengths (3, 4, 5, and 8 μm), where transport is scattering dominated and is also affected by extrinsic factors, we calculate

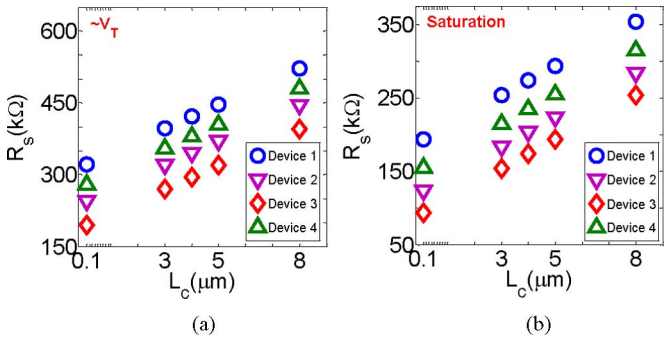


Fig. 5. Simulation results for resistance variations resulting from diameter distributions of CNTs (in the aligned array CNFETs) for the four devices are shown. (a) Resistance variations at threshold voltage. (b) Resistance variations in saturation. Resistance of CNT is calculated as $R = R_c + \rho L_c$, where R_c is contact resistance of CNT (calculated assuming the ballistic transport with the given SB height), ρ is the resistivity of the CNT, extracted from the slope of R_s versus L_c measurements, and L_c is the channel length.

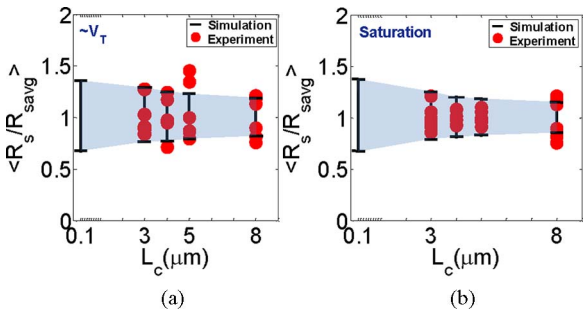


Fig. 6. Normalized R_s variability observed in simulations and experiments. (a) R_s variability at threshold voltage. (b) R_s variability in saturation. R_s has been normalized with respect to average. Lines (black) show the spread of normalized R_s and dots (red) show the experimental values. As seen in the figure, most of the experimental data fall within the extents of simulations (supposed to be originating from diameter distribution).

the total resistance R_s by using the expression $R_s = R_c + \rho L_c$, where R_c is the ballistic contact resistance, ρ is the resistivity of semiconducting tubes (determined from the slope of the experimental measurements of R_s versus L_c), and L_c is the channel length (3, 4, 5, or 8 μm). Fig. 5(a) and (b) shows that large variations in the resistance R_s are expected from the intrinsic variation in the diameter distribution, and these variations are comparable to those observed in the experiments [see Fig. 3(a) and (b)]. Fig. 6(a) and (b), on the other hand, shows the comparison of simulation result and experimental values of normalized resistances R_s (normalized with respect to averages). Black lines in the plot show the expected variability in R_s, as obtained from simulations, whereas the red circles show the measured experimental variations (measured at threshold and in saturation). The experimental variability is found within the extents of the intrinsic variation limits established by simulation results. Obviously, as discussed earlier, there are additional sources of extrinsic variability at longer channel devices.

Noting the simulation results of Figs. 5 and 6 and comparing with the observed experimental variations (see Fig. 3), we conclude that even for long-channel transistors, where other extrinsic effects like increase in defect density, charge trapping,

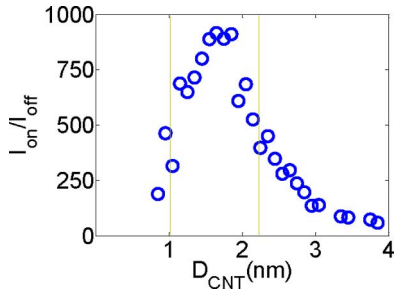


Fig. 7. Simulation results for the $I_{\rm ON}/I_{\rm OFF}$ as function of diameter of CNTs. Maximum $I_{\rm ON}/I_{\rm OFF}$ is only ~1000 due to small drain bias $V_{\rm ds} = -0.01$ V in these simulations ($I_{\rm ON}$ is drain current corresponding to the gate bias of -0.8 V).

etc. may play a significant role, the effect of diameter distribution is still significant, and therefore, a key conclusion of this paper is that unless the diameter distribution of the semiconducting tube is controlled, large-scale integration of the transistors based on this technology would be difficult.

Apart from fluctuation in the drain current, Fig. 7 demonstrates another important consequence of the diameter distribution in ultrascaled quasi-ballistic CNFET transistors. That is, in aligned array CNFETs, only a small fraction of the semiconducting CNTs with diameter 1.0 nm $< d_{\rm CNT} <$ 2.2 nm is capable of giving a good $I_{\rm ON}/I_{\rm OFF}$ ratio, and the rest must be eliminated for good transistors' performance. For $d >$ 2.2 nm, the $I_{\rm ON}/I_{\rm OFF}$ ratio is poor for the following reason: the metal Fermi level contacts large-diameter CNTs deep inside the valance band and the channel conductance (from OFF-state to ON-state) changes very little with gate bias. Therefore, even though these large diameter (small E_g) tubes carry significant amount of ON current, there is essentially no SB available to suppress the current during OFF-state. Such tubes, therefore, have poor $I_{\rm ON}/I_{\rm OFF}$ ratio that is not appropriate for digital logic operation. On the other hand, for very small diameter tubes with $d_{\rm CNT} <$ 1.0 nm, the barrier height is too large for any significant contribution to the ON current and the OFF current. These tubes are essentially electrically inactive and while they contribute to physical density, their contribution to electrical performance is negligible.

In fact, for the given diameter distribution shown in Fig. 4, only ~40% of s-CNTs carry most of the current through the device and ~60% carry insignificant current due to large bandgap (or SB). Of these 40% s-CNTs with high ON-state current, ~50% have $I_{\rm ON}/I_{\rm OFF} \geq 500$, while the bandgap of the remaining tubes are too small to be turned off effectively. Therefore, the performance of the device is dictated by ~20% of the total s-CNTs that have substantial current and good ON/OFF ratio ($I_{\rm ON}/I_{\rm OFF} \geq$ 500). On the other hand, if the $I_{\rm ON}/I_{\rm OFF} \sim 200$ is sufficient for specific applications, the percentage of performance determining s-CNTs rises to ~30%. Since two out of three SWNTs are semiconducting, therefore, eventually only about 15%–20% of the tubes that have good ON/OFF ratio are useful for directly bridging transistors. *In sum, increasing tube density without corresponding control over the diameter distribution may cause unacceptable level of fluctuation in ON current and threshold voltage, as well as poor ON/OFF ratio.*

While the aforementioned conclusion is based on CNFETs with Pd as source/drain contact material, we have also fabricated transistors with gold (Au) metallization scheme. These Au-contacted CNFETs exhibited ambipolar characteristics, contrary to p-type behavior of Pd-contacted devices. The detailed analysis of these Au-contacted transistors is underway and will be published elsewhere; however, the fluctuations in the devices' characteristics, having similar channel lengths and operating under similar conditions, are quite similar and can be understood in the same theoretical framework.

IV. Conclusion

In this paper, we have explored the origin of the surprisingly large device-to-device fluctuation in aligned array transistors, although originally we presumed that the source of the fluctuation is extrinsic and would rapidly diminish with improved processing. Detailed characterization and systematic modeling, however, lead us to a dramatically different conclusion, i.e., we now believe that even if the extrinsic factors during device processing (e.g., mobility, defect density, etc.) are controlled/eliminated, the intrinsic variations arising from CVD-grown diameter distributions of CNTs in aligned array CNFETs will still be a persistent source of variation in devices' performance, both for short- as well as long-channel transistors. Indeed, good ON/OFF ratio can only be achieved over a narrow range of diameters (see Fig. 7), and the definition of this range will be an important part of device optimization.

Therefore, our analysis of the effects of diameter distribution on the performance of aligned array CNT transistors shows that the control over diameter distribution is a critically important process parameter for attaining high-performance transistors and circuits with characteristics rivaling those of the state-of-the-art Si technology. Aligned network CNFETs are desirable to gain higher drive current, large active areas and to resolve inherent "impedance mismatch" problems for high-frequency applications (quantum of resistance $\sim$25 kΩ, typical of nanodevices and characteristics impedance of free space $\sim$377 Ω) [34], [35]. Of late, p-type and n-type single and aligned network nanotube FETs have been fabricated and logic gates have been demonstrated [36]–[38]; therefore, reproducibility in device current becomes essential before such applications are realized and promising results are achieved.

Can the diameter distribution of CNTs be easily controlled? Of the various techniques to control diameter distribution discussed in the literature, presorting by density differentiation seems effective in producing tubes of diameter 1.2–1.6 nm [39]. Fig. 7 suggests that the ideal diameter distribution for high ON current and ON/OFF ratio should be confined to 1.2–2.1 nm; however, tubes of 1.2–1.6 nm diameter would give reasonable performance as well. Since it is difficult to align solution-processed nanotubes for high-performance transistor applications, the integration of presorted tubes for use in the aligned arrays remains an open problem. Perhaps the most effective route of controlling diameter for aligned array CNFETs would come within the CVD process, where the initial size distribution of the catalysts are controlled by self-assembly technique. The problem of device-to-device fluctuation could also be addressed if long tubes are shared among various transistors so that regardless the diameter distribution, their device-to-device fluctuation is eliminated. This approach would restrict transistor layout; however, such layout rules are now routine in silicon ICs [40] and have been found not to have significant effect on transistors' performance or area penalty.

Acknowledgment

The authors would like to thank J. Appenzeller for discussion on carbon nanotube physics. The authors would also like to thank T. M. Abdolkader for his technical assistance in some CNT simulations.

References

[1] J. Appenzeller, "Carbon nanotubes for high-performance electronics – Progress and prospect," *Proc. IEEE*, vol. 96, no. 2, pp. 201–211, Feb. 2008.

[2] P. Avouris, "Molecular electronics with carbon nanotubes," *Acc. Chem. Res.*, vol. 35, pp. 1026–1034, Dec. 2002.

[3] P. Avouris, "Carbon nanotube electronics and optoelectronics," *Abs. Pap. Amer. Chem. Soc.*, vol. 227, pp. U253–U254, Mar. 28, 2004.

[4] J. Chen, M. Freitag, C. Klinke, A. Afzali, J. Tsang, and P. Avouris, "Carbon nanotube electronics and optoelectronics," *Abs. Pap. Amer. Chem. Soc.*, vol. 229, pp. U925–U925, Mar. 13, 2005.

[5] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, and H. J. Dai, "High-kappa dielectrics for advanced carbon-nanotube transistors and logic gates," *Nature Mater.*, vol. 1, pp. 241–246, Dec. 2002.

[6] G. Gruner, "Carbon nanotube films for transparent and plastic electronics," *J. Mater. Chem.*, vol. 16, pp. 3533–3539, 2006.

[7] N. Pimparkar, C. Kocabas, S. J. Kang, J. Rogers, and M. A. Alam, "Limits of performance gain of aligned CNT over randomized network: Theoretical predictions and experimental validation," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 593–595, Jul. 2007.

[8] E. S. Snow, P. M. Campbell, M. G. Ancona, and J. P. Novak, "High-mobility carbon-nanotube thin-film transistors on a polymeric substrate," *Appl. Phys. Lett.*, vol. 86, pp. 033105-1–033105-3, Jan 17, 2005.

[9] R. Seidel, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Steinhoegl, F. Kreupl, W. Hoenlein, and W. Pompe, "High-current nanotube transistors," *Nano Lett.*, vol. 4, pp. 831–834, 2004.

[10] V. Sazonova, Y. Yaish, H. Ustunel, D. Roundy, T. A. Arias, and P. L. McEuen, "A tunable carbon nanotube electromechanical oscillator," *Nature*, vol. 431, pp. 284–287, Sep. 16, 2004.

[11] Z. Chen, J. Appenzeller, J. Knoch, Y. M. Lin, and P. Avouris, "The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors," *Nano Lett.*, vol. 5, pp. 1497–1502, 2005.

[12] N. Pimparkar, Q. Cao, S. Kumar, J. Y. Murthy, J. Rogers, and M. A. Alam, "Current-voltage characteristics of long-channel nanobundle thin-film transistors: A "bottom-up" perspective," *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 157–160, Feb. 2007.

[13] P. Avouris, J. Appenzeller, R. Martel, and S. J. Wind, "Carbon nanotube electronics," *Proc. IEEE*, vol. 91, no. 11, pp. 1772–1784, Nov. 2003.

[14] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. J. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, pp. 654–657, Aug. 7, 2003.

[15] J. Appenzeller, J. Knoch, R. Martel, V. Derycke, S. J. Wind, and P. Avouris, "Carbon nanotube electronics," *IEEE Trans. Nanotechnol.*, vol. 1, pp. 184–189, Dec. 2002.

[16] W. B. Choi, E. Bae, D. Kang, S. Chae, B. H. Cheong, J. H. Ko, E. M. Lee, and W. Park, "Aligned carbon nanotubes for nanoelectronics," *Nanotechnology*, vol. 15, pp. S512–S516, Oct. 2004.

[17] S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," *Nat. Nano.*, vol. 2, pp. 230–236, 2007.

[18] M. H. Yang, K. B. K. Teo, L. Gangloff, W. I. Milne, D. G. Hasko, Y. Robert, and P. Legagneux, "Advantages of top-gate, high-k dielectric carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 88, pp. 113507-1–113507-3, Mar. 13, 2006.

[19] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambrige, U.K.: Cambridge Univ. Press, 1998.
[20] X. Liu, T. Pichler, M. Knupfer, M. S. Golden, J. Fink, H. Kataura, and Y. Achiba, "Detailed analysis of the mean diameter and diameter distribution of single-wall carbon nanotubes from their optical response," *Phys. Rev. B*, vol. 66, pp. 045411-1–045411-8, Jul. 15, 2002.
[21] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and P. Avouris, "Field-modulated carrier transport in carbon nanotube transistors," *Phys. Rev. Lett.*, vol. 89, pp. 126801-1–126801-4, 2002.
[22] M. P. Anantram and F. Leonard, "Physics of carbon nanotube electronic devices," *Rep. Progr. Phys.*, vol. 69, pp. 507–561, Mar. 2006.
[23] P. Avouris, "Carbon nanotube electronics," *Chem. Phys.*, vol. 281, pp. 429–445, Aug. 1, 2002.
[24] D. Mann, A. Javey, J. Kong, Q. Wang, and H. J. Dai, "Ballistic transport in metallic nanotubes with reliable Pd ohmic contacts," *Nano Lett.*, vol. 3, pp. 1541–1544, Nov. 2003.
[25] M. S. Dresselhaus, G. Dresselhaus, and R. Saito, "Physics of carbon nanotubes," *Carbon*, vol. 33, pp. 883–891, 1995.
[26] M. Shiraishi, K. Hinokuma, and M. Ata, "The measurement of work function of carbon nanotubes," *Electron. Properties Novel Mater.-Mol. Nanostruct.*, vol. 544, pp. 359–362, 2000.
[27] M. Shiraishi and M. Ata, "Work function of carbon nanotubes," *Carbon*, vol. 39, pp. 1913–1917, 2001.
[28] X. Cui, M. Freitag, R. Martel, L. Brus, and P. Avouris, "Controlling energy-level alignments at carbon nanotube/Au contacts," *Nano Lett.*, vol. 3, pp. 783–787, 2003.
[29] R. Saito, G. Dresselhaus, and M. S. Dresselhaus, *Physical Properties of Carbon Nanotubes*. London, U.K.: Imperial College Press, 1998.
[30] J. W. Mintmire and C. T. White, "Electronic and structural properties of carbon nanotubes," *Carbon*, vol. 33, pp. 893–902, 1995.
[31] J. W. G. Wildoer, L. C. Venema, A. G. Rinzler, R. E. Smalley, and C. Dekker, "Electronic structure of atomically resolved carbon nanotubes," *Nature*, vol. 391, pp. 59–62, Jan. 1, 1998.
[32] N. Neophytou, S. S. Ahmed, E. Polizzi, G. Klimeck, and M. Lundstrom, "CNTFET Lab," 2006. DOI: 10254/nanohub-r1091.6.
[33] N. Neophytou, J. Guo, and M. S. Lundstrom, "Three-dimensional electrostatic effects of carbon nanotube transistors," *IEEE Trans. Nanotechnol.*, vol. 5, no. 4, pp. 385–392, Jul. 2006.
[34] C. Rutherglen and P. Burke, "Carbon nanotube radio," *Nano Lett.*, vol. 7, pp. 3296–3299, 2007.
[35] P. Avouris, Z. Chen, and V. Perebeinos, "Carbon-based electronics," *Nature Nanotechnol.*, vol. 2, pp. 605–615, 2007.
[36] R. Martel, V. Derycke, J. Appenzeller, P. H. S. Wong, and P. Avouris, "Carbon nanotube field-effect transistors and logic devices," *Abs. Pap. Amer. Chem. Soc.*, vol. 222, pp. U184–U185, Aug. 2001.
[37] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, "Logic circuits with carbon nanotube transistors," *Science*, vol. 294, pp. 1317–1320, 2001.
[38] Q. Cao, H. S. Kim, N. Pimparkar, J. P. Kulkarni, C. J. Wang, M. Shim, K. Roy, M. A. Alam, and J. A. Rogers, "Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates," *Nature*, vol. 454, pp. 495–U4, Jul. 24, 2008.
[39] M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, and M. C. Hersam, "Sorting carbon nanotubes by electronic structure using density differentiation," *Nat Nano*, vol. 1, pp. 60–65, 2006.
[40] D. D. Jansen, *The Electronic Design Automation Handbook*. Norwell, MA: Kluwer, 2003.

Shuaib Salamat (S'09) received the B.S. degree in aeronautical engineering from National University of Science and Technology, Islamabad, Pakistan, in 1998, and the M.S. degree in electrical engineering, in 2008, from Purdue University, West Lafayette, IN, where he is currently working toward the Ph.D. degree.

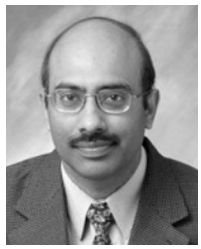
His research interests include simulation and modeling of carbon nanotube and other nanotransistors. He is currently engaged in the research on the effects of electronic and thermal transport in nanoscale devices.

Xinning Ho received the B.S. degree in materials science and engineering from Cornell University, Ithaca, NY, in 2005. She is currently working toward the Ph.D. degree in materials science and engineering at the University of Illinois, Urbana-Champaign under Professor J. A. Rogers' guidance.

Her research interests include device physics and design of solid-state devices.

John A. Rogers (F'09) received the B.A. degree in chemistry, the B.S. degree in physics, both from the University of Texas, Austin, in 1989, the S.M. degrees in physics and in chemistry, in 1992, and the Ph.D. degree in physical chemistry, in 1995, all from Massachusetts Institute of Technology, Cambridge.

He is currently the Flory-Founder Chair in engineering at the University of Illinois, Urbana-Champaign. His research interests include fundamental and applied aspects of nanometer- and molecular-scale fabrication, materials and patterning techniques for unusual format electronics, and photonic systems.



Muhammad Ashraful Alam (F'06) received the B.S. degree from Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 1988, the M. S. degree from Clarkson University, Potsdam, New York, in 1991, and the Ph.D. degree from Purdue University, West Lafayette, IN, in 1994, all in electrical engineering.

From 1995 to 2001, he was a Member of Technical Staff in Silicon Ultra-Large Scale Integration (ULSI) Research Department, Bell Laboratories. From 2001 to 2003, he was a Distinguished Member of Technical Staff at Agere Systems. He is currently a Professor of electrical and computer engineering at Purdue University, where he is engaged in research and teaching on physics, simulation, characterization, and technology of classical and novel semiconductor devices including theory of oxide reliability, nanocomposite thin-film transistors, and nanobio sensors. He has authored or coauthored more than 80 papers published in international journals and has presented many invited and contributed talks at international conferences.

Dr. Alam is a Purdue University Faculty Scholar. He received the 2006 IEEE Kiyo Tomiyasu Award for his contributions to device technology for communication systems.