LETTERS

GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies

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Compound semiconductors like gallium arsenide (GaAs) provide advantages over silicon for many applications, owing to their direct bandgaps and high electron mobilities. Examples range from efficient photovoltaic devices[1,2] to radio-frequency electronics[3,4] and most forms of optoelectronics[5,6]. However, growing large, high quality wafers of these materials, and intimately integrating them on silicon or amorphous substrates (such as glass or plastic) is expensive, which restricts their use. Here we describe materials and fabrication concepts that address many of these challenges, through the use of films of GaAs or AlGaAs grown in thick, multilayer epitaxial assemblies, then separated from each other and distributed on foreign substrates by printing. This method yields large quantities of high quality semiconductor material capable of device integration in large area formats, in a manner that also allows the wafer to be reused for additional growths. We demonstrate some capabilities of this approach with three different applications: GaAs-based metal semiconductor field effect transistors and logic gates on plates of glass, near-infrared imaging devices on wafers of silicon, and photovoltaic modules on sheets of plastic. These results illustrate the implementation of compound semiconductors such as GaAs in applications whose cost structures, formats, area coverages or modes of use are incompatible with conventional growth or integration strategies.

Some of the most daunting technical challenges associated with established methods for using GaAs occur in terrestrial photovoltaics, where the extremely high efficiencies of GaAs solar cells[7,8] might otherwise offer compelling opportunities. Here, the demands on cost and the necessity for integration over large areas on glass or other foreign substrates lead to requirements that lie well outside current capabilities. Previously known techniques, most notably epitaxial lift-off[9–12], separate GaAs solar cells from their growth substrates to reduce their cost or weight[10,11], but difficulties in handling the lifted materials[12] limit their use. Despite continuing progress[11,12], photovoltaic epitaxial lift-off has remained as a research topic for over 30 years, with no commercial implementation. More tractable, yet still difficult, problems appear in advanced electronics and optoelectronics where, as examples, device-level integration of compound semiconductors with silicon electronics can improve high speed operation in radio-frequency systems[13], add capabilities for light emission in devices for lightwave communications[14] or enable efficient photodetection for night-vision cameras[15]. Wafer bonding[16], heteroepitaxy[17], pick-and-place techniques[18] and chip-scale packaging methods[19] can meet certain requirements of these and other applications, but not without some combination of disadvantages that include restricted scales or modes for integration, limited substrate compatibility and poor cost effectiveness.

Alternative methods that avoid these drawbacks and, at the same time, provide realistic means of distributing large quantities of material over large areas on amorphous substrates could have significant practical value. Recent work by us and others demonstrates potential for compound semiconductor nanomaterials and unusual guided or deterministic assembly methods to address some of these challenges[20–22]. Limitations in the amounts and formats of these materials, difficulties in their scalable integration into devices and/or uncertain compositions and properties frustrate their use for many important applications. We present here concepts that overcome these issues by exploiting device-quality compound semiconductor films epitaxially grown in thick, multilayer formats specially designed for separation from one another, release from the wafer and subsequent integration in diverse layouts on various substrate types. This approach greatly reduces the need for wafer refinishing, compared to analogous single-layer lift-off approaches, and eliminates cycles of loading and unloading of wafers into the growth chamber. In favourable cases, the net effect can be an increase in throughput and a decrease in cost of more than an order of magnitude (Supplementary Information). The outcomes are applicable to every area of use for compound semiconductors, from electronics to optoelectronics and photovoltaics, as illustrated in the following.

The basic strategy appears in Fig. 1. Metal organic chemical vapour deposition (MOCVD) forms multiple layers of GaAs and/or AlGaAs or other related materials with compositions and layouts that match device requirements, with separating films of AlAs ($Al_{0.95}Ga_{0.05}As$). Figure 1a presents a simple case of 14 such layers, similar to designs used in the electronics examples described next. Figure 1b shows secondary ion mass spectrometry (SIMS) depth profiles of the composition of a structure with the layout of Fig. 1a, illustrating well defined layers with abrupt interfaces. Many more layers are possible, limited by layer morphologies, doping profiles and differential stresses and, ultimately for certain systems (for example, Fig. 1e), by practical constraints on growth times (Supplementary Information). Patterned vertical etching through the entire stack exposes the sidewalls of the layers and delineates the material into separated blocks with desired lateral dimensions. Immersion in hydrofluoric acid (HF) selectively eliminates the AlAs layers, thereby releasing large collections of pieces of GaAs (and/or multilayers with AlGaAs or other materials), with sizes that can range from micrometres to centimetres, and thicknesses from several nanometres to micrometres.

Figure 1c shows a cross-sectional scanning electron microscope (SEM) image of the system schematically illustrated in Fig. 1a after vertical etching and brief immersion in HF. The etching rate for $Al_xGa_{1-x}As$ over GaAs depends on the aluminium fraction[23].

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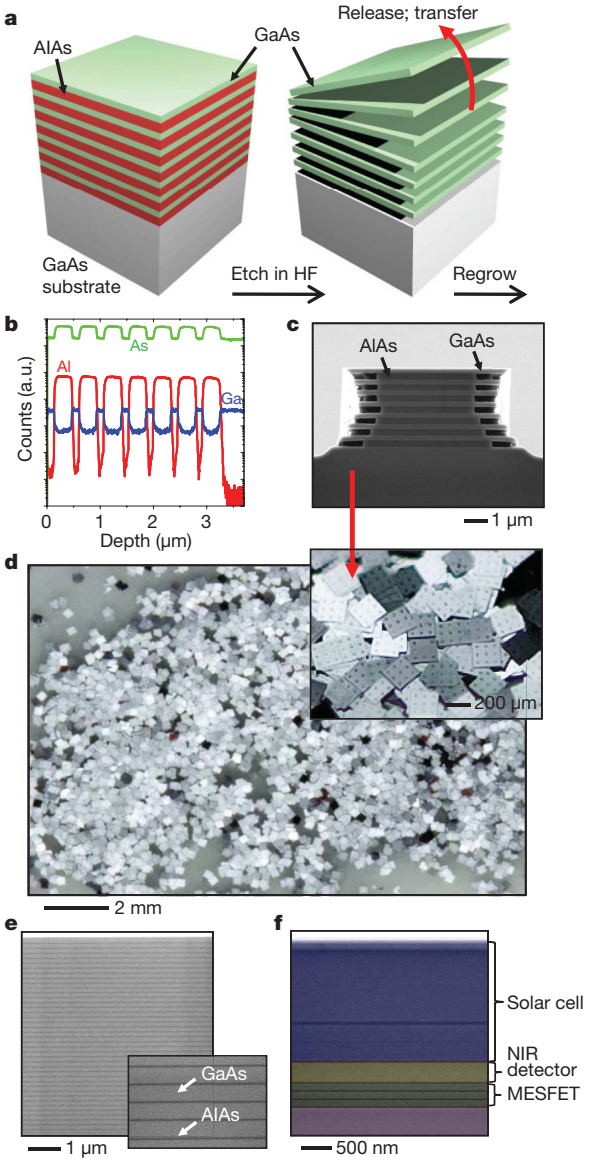

Figure 1 | Schematic illustration, optical and SEM images, and SIMS profile of GaAs/AlAs multilayers. a, Schematic illustration of a multilayer stack of GaAs/AlAs and schemes for release through selective etching of the layers of AlAs. **b**, Corresponding SIMS profile of this stack. **c**, Cross-sectional SEM image after partial etching of the AlAs layers. **d**, Optical image of a large collection of GaAs solar cells formed by release from a three-layer stack, and then solution casting onto another substrate. Inset, high magnification view. **e**, Cross-sectional SEM image of a 40 repeat multilayer stack of GaAs (200 nm)/AlAs with ultrathin (20 nm) AlAs sacrificial layers. Inset, high-magnification view. **f**, Cross-sectional SEM image (coloured) of a heterogeneous multilayer stack composed of three layers for MESFETs (green), one layer for an NIR detector (yellow) and one layer for a single junction solar cell (blue). The substrate is purple. Each of the device layers is separated by 20 nm AlAs (red). Details of stack design and corresponding SIMS profile are in Supplementary Information.

Increasing the fraction (for $x > 0.7$) results in highly enhanced rates of etching in HF. For example, etching of GaAs occurs at a rate 10^6 times lower than that of AlAs (ref. 24). The GaAs component can incorporate other layers of epitaxial materials, with the constraint that their etching rate is sufficiently low in HF and that thermally driven diffusion of any mobile species during growth does not lead to adverse effects. In the following, we exploit this flexibility to grow multilayer stacks for metal semiconductor field effect transistors (MESFETs), Schottky diodes, near-infrared (NIR) photodetectors and single-junction photovoltaic cells. Figure 1d shows a macroscopic pile of such cells (square platelets ~200 μm on a side, and ~4.5 μm thick), formed from an AlAs-separated three-layer assembly of GaAs stacks that each consist of six Zn and Si doped layers of GaAs and AlGaAs; details appear below. The collective assembly on the growth wafer incorporates 22 epitaxial layers, with a total thickness of ~17 μm. In this case, and others, the wafer surface can be refinished after complete lift-off to prepare it for additional growths. These concepts can be extended to extremely large multilayer stacks (for example, 40-layer repeats; Fig. 1e) and to heterogeneous collections of devices (for example, solar cells, transistors and photodetectors; Fig. 1f).

To demonstrate the simplest example first, we formed multilayers (seven repeats) of n-type GaAs (200 nm; Si-doped to 4×10^{17} cm^{-3}) and AlAs (300 nm) on a (100)GaAs substrate, for building MESFETs. Complete etching and release of GaAs active elements, followed by solution assembly on a target substrate, represents one conceivable route to device integration. Here we use extensions of deterministic assembly procedures described elsewhere[25,26], in which each of the individual GaAs layers in the stack is released and then transfer printed one at a time, in a step and repeat fashion, onto a glass substrate coated with a thin layer of polyimide. Printing tools, with yields >99.5%, submicrometre placement accuracy and throughputs corresponding to millions of dies per hour, are under commercial development. Details, including cost estimates, appear in Supplementary Information. Fabricating MESFETs from the printed GaAs membranes involves patterned etching to define the channel regions, followed by additional processing to create ohmic source and drain contacts (Pd/Ge/Au) and Schottky gates (Ti/Au). Figure 2a and b shows schematic illustrations and optical images, respectively. Figure 2c and d presents current/voltage (I/V) characteristics and transfer curves of representative devices (with channel widths of 130 μm, channel lengths of 25 μm and gate lengths of 3 μm) from each of the top five layers in the stack. In all cases the layer-to-layer variations in properties are random, with magnitudes comparable to device-to-device variations observed in any given single layer.

The electrode layouts enable probing of high frequency response with a vector network analyser. Representative results appear in Fig. 2e, which plots the current gain (H_{21}) and maximum available gain (MAG) as a function of frequency for the fourth layer device, indicating that the unity current gain frequency (f_T) and unity power gain frequency (f_{max}) are around ~2 and ~6 GHz, respectively, even for this relatively coarse channel dimension, as expected on the basis of the high electron mobility in GaAs (ref. 27). This response, as well as the maximum transconductances (~3.4 mS), on/off current ratios (~10^6), maximum current outputs per channel width (~1.1×10^{-5} A μm^{-1}) and other parameters inferred from electrical testing, is consistent with expectation based on devices with similar designs formed on a GaAs wafer. Integration of multiple MESFETs yields logic gates, as a step towards integrated circuits. Figure 2f shows optical images of NAND and NOR gates that each consist of three interconnected devices. The load and switching transistors have channel lengths of 55 and 25 μm, respectively, both with gate lengths of 3 μm and channel widths of 130 μm. Figure 2g and h presents output–input characteristics of NAND and NOR gates, respectively. In both cases, the logic '0' and '1' input signals correspond to −3 V and 1 V, respectively, for V_{dd} (the drain voltage of the load transistor) equal to 5 V. The logic '0' and '1' outputs of the NAND gate are 0.5–0.9 V and 5 V, respectively; the corresponding outputs of the NOR gate are 0.3–0.6 V and 5 V.

NIR imagers composed of interconnected arrays of GaAs photodiodes and blocking diodes provide a second, more advanced and different means of exploiting the multilayer concepts. Figure 3a provides a schematic illustration of the device layout in this case. The epitaxial stacks include bilayers of undoped GaAs (500 nm thick) and n-type GaAs (50 nm thick; Si-doped to 8×10^{16} cm^{-3}), in a four-layer assembly separated by AlAs (300 nm thick). To demonstrate a processing option different from that for the MESFETs, we built fully functional, interconnected systems using each active layer on the growth wafer, followed, in sequential fashion, by transfer to a target substrate. We chose silicon in this case owing to its established use for

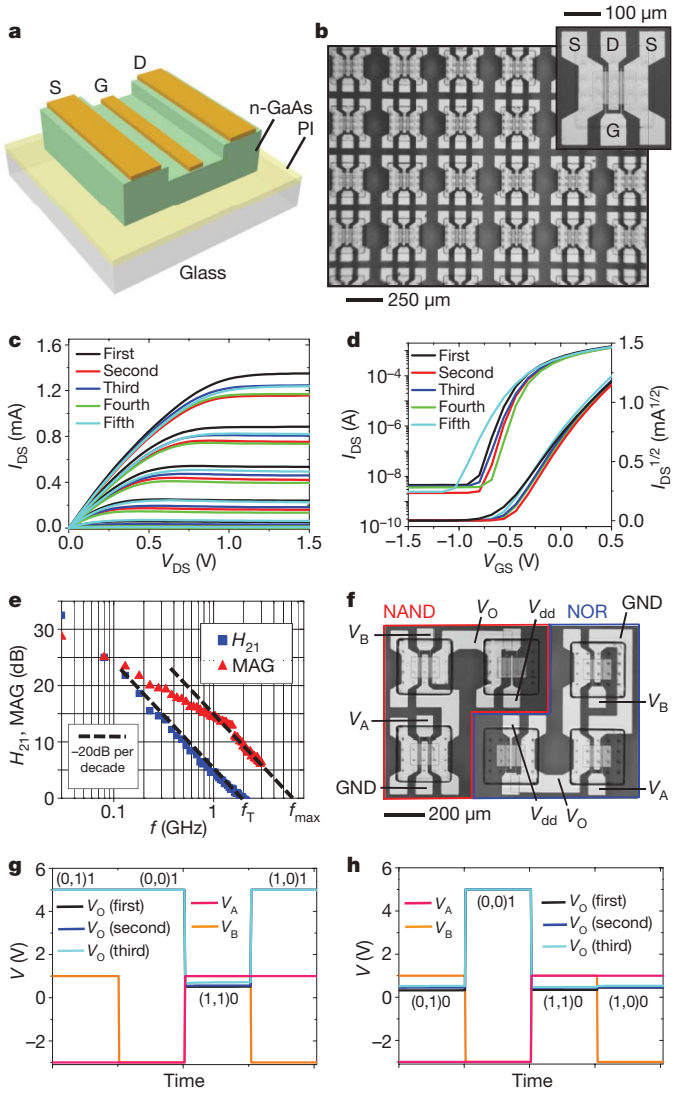

Figure 2 | Multilayer GaAs MESFETs and logic circuits. **a**, Schematic illustration of a GaAs MESFET on a polyimide (PI) coated glass substrate. **b**, Optical image of arrays of MESFETs on glass substrate. Inset, a single MESFET with source (S), drain (D) and gate (G) metal layers. **c**, V_{DS} (drain–source voltage) versus I_{DS} (drain–source current) curves of MESFETs fabricated from first, second, third, fourth and fifth layers at gate–source voltages (V_{GS}) of 0.4, 0.2, 0, −0.2, −0.4 and −0.6 V, from top to bottom. **d**, I_{DS} versus V_{GS} transfer curves of MESFETs fabricated from first, second, third, fourth and fifth layers, at V_{DS} = 1.5 V. **e**, Amplitude plots for current gain (H_{21}) and MAG measured from the fourth layer device. The unity current gain frequency (f_T) and unity power gain frequency (f_{max}) are ~2 and ~6 GHz, respectively. **f**, Optical image of NAND and NOR gates on polyimide (V_A, V_B, input voltages for switching transistors; V_{dd}, drain voltage for load transistor; V_O, output voltage). **g**, Output–input characteristics of NAND gates using devices from the first, second and third layers. **h**, As **g** but for NOR gates.

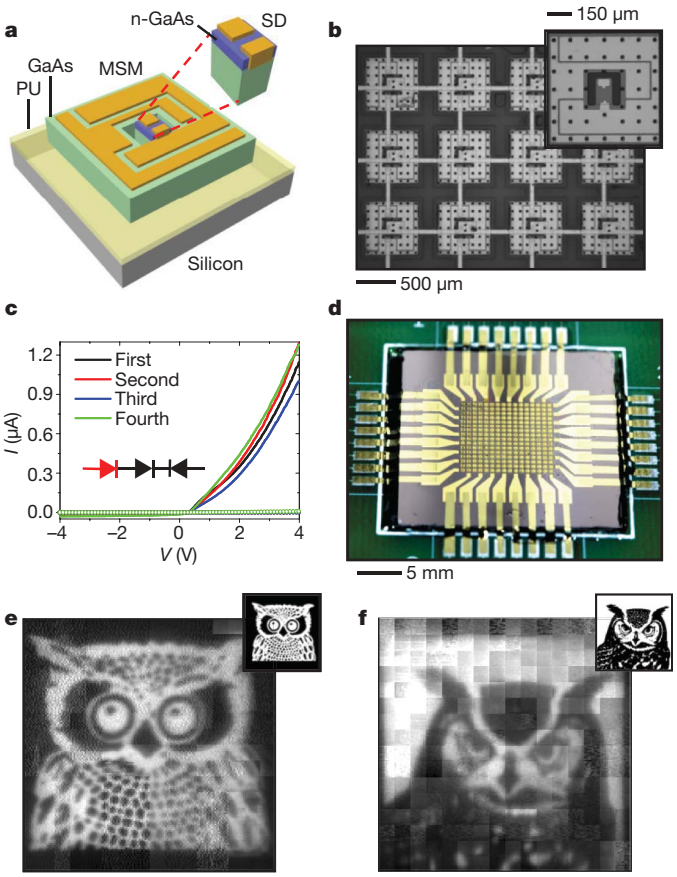

Figure 3 | Multilayer GaAs NIR imagers. **a**, Schematic illustration of a GaAs metal–semiconductor–metal (MSM) NIR detector on a Si wafer coated with a photocurable polyurethane (PU). Inset, Schottky blocking diode (SD). **b**, Optical image of a NIR imager consisting of a 16 × 16 array of detectors (12 pixels are shown). Inset, a unit cell before interconnect metallization. **c**, I/V characteristics of a cell formed with material from the first, second, third and fourth layers. Open circles and lines correspond to responses in the dark and under NIR illumination (wavelength 830 nm), respectively. **d**, Photograph of an NIR imager mounted on a printed circuit board. **e**, Image acquired with an NIR imager formed with material from the second layer. **f**, As **e** but using material from the fourth layer. Insets in **e** and **f** correspond to objects that were imaged.

image processing in conventional infrared cameras formed by solder bump bonding[28]. Forming Schottky contacts (Ti/Au) to the top, undoped GaAs layers yields metal–semiconductor–metal diodes. Such contacts combined with ohmic contacts (Pd/Ge/Au) to the Si-doped GaAs provide Schottky diodes. The metal–semiconductor–metal devices enable NIR detection, while the Schottky diodes block the reverse bias current to prevent crosstalk for passive matrix readout of the array.

Figure 3b shows an image of the layout of a photodiode/blocking diode pair, in the geometry used for the NIR imagers. Figure 3c presents representative I/V characteristics and photoresponse for typical devices formed using the first, second, third and fourth layers in the stack. The open circles and lines correspond to responses in the dark and under NIR illumination (830 nm), respectively. The data indicate comparable and reproducible behaviour for all layers. Ratios of currents in the on and off states are ~200, sufficient for passive matrix readout. A spin cast, photodefinable epoxy serves as a mechanical support and substrate for metal interconnection lines between 256 such devices, to yield independently addressable arrays (16 × 16 elements) for imaging. Transfer printing delivers the completed system to a silicon wafer that mounts on a printed circuit board interface to a computer for image acquisition (Fig. 3d). The yields of properly functioning pixels were better than ~96% in individual pixels and ~70% in interconnected arrays, limited mainly by breaks in interconnection metals. Figure 3e and f shows images of pictures of owls collected with NIR illumination and two separate cameras formed with the second and fourth layers, respectively. Image collection involved a scanning mode[29], to achieve an effective level of resolution much higher than that defined by the numbers of pixels and to provide oversampling for minimizing adverse effects of non-uniformities and malfunctioning pixels.

The third demonstration is in photovoltaics, where six-layer stacks of Zn and Si doped GaAs and AlGaAs form single-junction solar cells, epitaxially grown in trilayer assemblies separated by layers of AlAs (1 μm thick). Figure 4a illustrates the layout of the materials and the

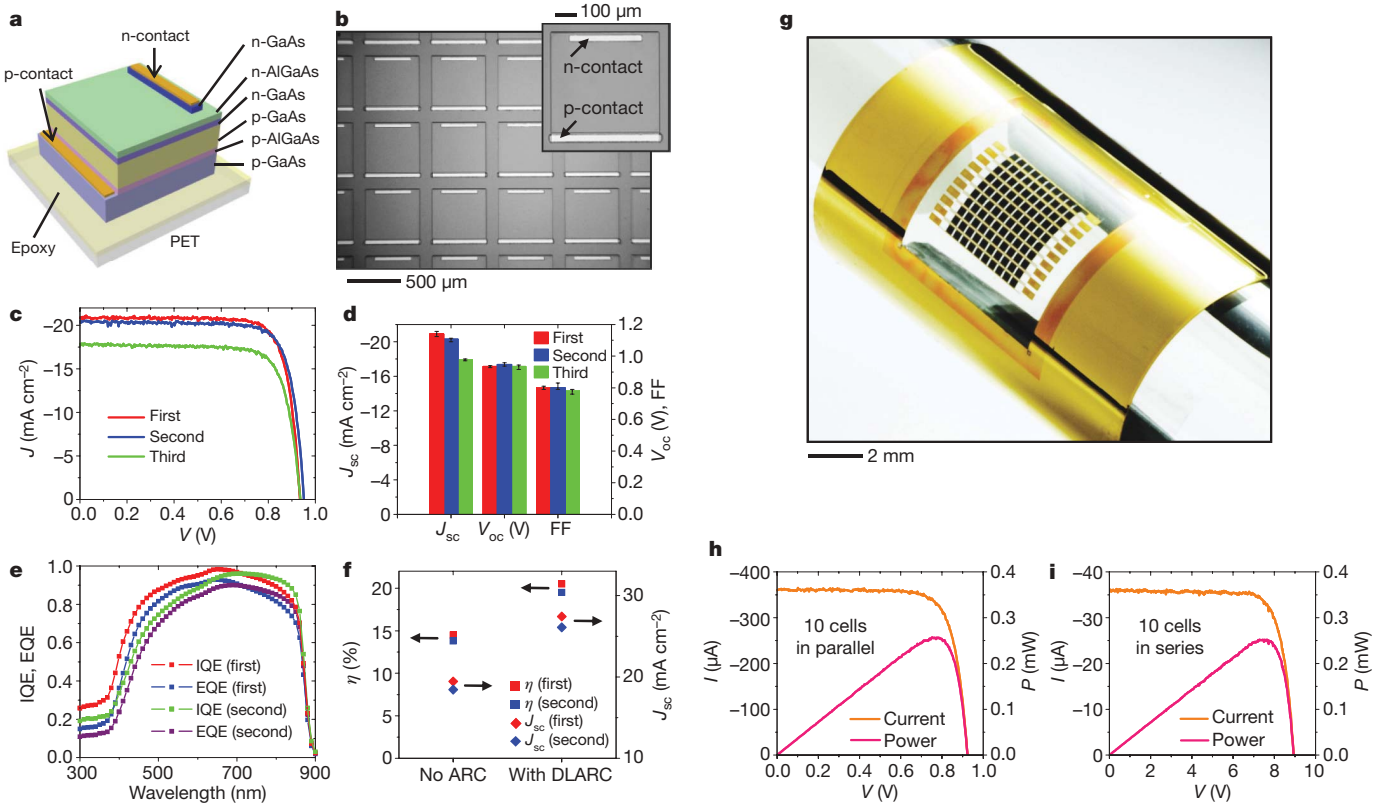

Figure 4 | Multilayer GaAs single-junction solar cells. a, Schematic illustration of GaAs single-junction solar cell on a PET substrate coated with a photodefinable epoxy. **b**, Optical image of arrays of such devices formed on the source wafer. Inset, magnified view of top (n-type) and bottom (p-type) contacts. **c**, Representative light current density (J)-voltage (V) curves for Zn-doped solar cells formed from the first (top), second (middle) and third (bottom) layers, under AM1.5D illumination measured on the source wafer with a single-layer ARC of Si_3N_4. **d**, Short-circuit current density (J_{sc}), fill factor (FF) and open circuit voltage (V_{oc}) of first, second and third layer devices. Error bars, max./min. **e**, IQE and EQE of first and second layer devices. **f**, Projected efficiencies (η) and J_{sc} values without ARC and with double-layer ARCs (DLARC; MgF_2/ZnS) for devices formed using material from the first and second layers. **g**, Photograph of a solar module consisting of a 10 × 10 array of GaAs solar cells (each ~500 μm × 500 μm) on a PET substrate. **h**, Light current–voltage (I/V) and power–voltage (P/V) curves for such a module with parallel interconnection of 10 cells. **i**, As **h** but with series interconnection. Both measurements were made in a flat configuration.

geometry of the contacts. Each GaAs and AlGaAs epitaxial construct consists of an n-type top contact layer (0.2 μm thick GaAs; Si-doped), an n-type window layer (40 nm thick $Al_{0.4}Ga_{0.6}As$; Si-doped), an n-type emitter (0.1 μm thick GaAs; Si-doped), a p-type base (2 μm thick GaAs; Zn-doped), a p-type back surface field layer (0.1 μm thick $Al_{0.3}Ga_{0.7}As$; Zn-doped) and a p-type bottom contact layer (2 μm thick GaAs; Zn-doped). Vertical etching delineates arrays of cells with lateral dimensions of ~500 × 500 μm on the source wafer. Controlled etching of selected regions (35 × 500 μm) near the edges of these cells exposes the bottom p-contact layer. This process, followed by removal of all but a small part of the top n-contact layer (30 × 330 μm) prepares the wafer for deposition and patterning of contact metals. The n and p contacts consist of Pd/Ge/Au and Pt/Ti/Pt/Au, respectively (Fig. 4b). Current density/voltage (J/V) curves and extracted characteristics of individual cells from each layer measured under simulated AM1.5D (air mass 1.5 direct) illumination (1,000 W m^{-2}) at room temperature with a single-layer antireflection coating (ARC; Si_3N_4) appear in Fig. 4c and d, respectively, where the current densities correspond to the active areas of the cells. AM1.5D illumination provides measurements that are relevant to terrestrial concentrator photovoltaics.

Moderate decreases in J from the top to the bottom layer are systematic, and can be attributed to the diffusion of Zn in the p-type GaAs layers, as revealed by SIMS analysis (Supplementary Information). This behaviour might be eliminated by the use of alternative dopants, such as carbon, that have negligible diffusion coefficients. Figure 4e shows external and internal quantum efficiencies (EQE and IQE, respectively) with an ARC for top and middle layer devices. The calculated efficiencies based on these measurements and AM1.5D reference spectrum without an ARC are ~14.5% and ~13.5% for top and middle layer devices, respectively (Fig. 4f). A double-layer ARC (such as MgF_2/ZnS; Fig. 4f) can increase the efficiency to ~20.5% (~19.5% for the middle layer; see Supplementary Information), which approaches the performance of some of the best reported devices designed for ultrahigh concentration (~20.6%)[30]. The performance can be further improved by the use of optimized cell designs and ARCs. These ultrathin cells provide other interesting features, such as the ability to integrate onto thin (~50 μm) sheets of polyethylene terephthalate (PET) for mechanically flexible modules capable of bending to radii of curvature of <5 mm without degradation in performance. Figure 4g presents an image of such a device, consisting of 100 interconnected cells (10 × 10 array), wrapped onto a cylindrical support. The cells can be combined in series and/or parallel configurations to yield output power at high or low voltages (or anything in between), thereby highlighting an important advantage of the use of large collections of small cells. Figure 4h and i presents output characteristics of devices that use parallel and series interconnects for output voltages of 0.93 V and 8.9 V, respectively, with similar total maximum output power (0.23 mW and 0.25 mW, respectively). Similar processing steps can be used with large (>1 cm) devices, as described in the Supplementary Information. Edge recombination, even at 100 μm cell sizes, reduces the efficiency by less than 1% (Supplementary Information).

In conclusion, approaches reported here provide advantages in integration possibilities, designs and cost, to create opportunities that are inaccessible to established technologies. The remaining technical barriers to commercialization are specific to the application. For example, solar cells that incorporate tunnel junctions may

require special growth strategies for production in thick, multilayer configurations. Exploring other material systems, such as gallium nitride and indium phosphide, and other devices, such as light emitting diodes, lasers and sensors, represent additional promising directions for future work.

METHODS SUMMARY

Multilayer structures for MESFETs, NIR imagers and single-junction solar cells were grown on (100)GaAs substrates by MOCVD. Etching through the top GaAs layer (or GaAs/AlGaAs stack) with a mixture of citric acid and hydrogen peroxide created vertical trenches. Partially etching into the underlying, exposed AlAs layer with HF created a slight undercut around the periphery of the trenches. Spin coating a layer of photoresist and patterning it by photolithography formed structures that, after complete etching of the AlAs, tethered fully released GaAs membranes to the underlying wafer. Techniques of transfer printing were used to integrate the released GaAs/AlGaAs structures onto substrates of interest. Repetitive application of this sequence of steps separated each of the layers in the original stack, and integrated them onto target substrates. For MESFETs and logic gates, n-type GaAs membranes were transfer printed to a glass substrate coated with a partially cured polyimide. A sequence of photolithography, electron beam evaporation and annealing steps yielded ohmic source and drain electrodes and Schottky gate electrodes to form the MESFETs and logic gates. For NIR imagers, fully interconnected device arrays were formed on the source wafer. After undercut etching, the arrays were transfer printed to a Si wafer coated with a photocurable polyurethane, and connected to a computer for image acquisition. For single-junction solar cells, individual cells were formed through bottom contact exposure, top contact etch, isolation and ohmic contact formation. Si_3N_4 served as an ARC. Arrays of the resulting cells were released by undercut-etching and then were transfer printed to a PET substrate coated with a photodefinable epoxy, followed by fabrication of metal interconnects and encapsulation layers. Current–voltage measurements were conducted using a direct-current (d.c.) source meter and a full-spectrum solar simulator. External and internal quantum efficiencies were measured using a spectroradiometer system.

Full Methods and any associated references are available in the online version of the paper at www.nature.com/nature.

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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METHODS

Epitaxial multilayer growth. Multilayer structures for MESFETs, NIR imagers and heterogeneous devices (MESFETs, NIR photodetectors and solar cells) were grown on an n-type Si-doped GaAs(100) substrate using a Thomas Swan atmospheric pressure MOCVD reactor. In all cases, a GaAs buffer layer with thickness of 200 nm was formed first, at 800 °C. Trimethyl gallium, trimethyl aluminium and arsine (AsH_3) served as precursors for Ga, Al and As, respectively. Disilane (Si_2H_6) and dimethylzinc were used for Si (n-type) and Zn (p-type) doping, respectively. Purified hydrogen served as the carrier gas. The growth temperature in all cases was 800 °C. Epitaxial multilayer structures for the MESFETs consisted of either seven or forty bilayers of n-type GaAs (200 nm, 4×10^{17} cm^{-3}, Si-doped) and $Al_{0.95}Ga_{0.05}As$ (300 nm for 7 bilayers, 20 nm for 40 bilayers). For the NIR imagers, the structure included four repeats of n-type GaAs (50 nm, 8×10^{16} cm^{-3}, Si-doped), undoped GaAs (500 nm) and $Al_{0.95}Ga_{0.05}As$ (300 nm). Details on heterogeneous stacks appear in the Supplementary Information. Multilayer structures for n-on-p type single-junction solar cells were grown by Epiworks Inc. with its commercial EpiSure solar cell growth processes in a low-pressure MOCVD production system (modified Aixtron 2600G3). The materials were deposited on (100)GaAs substrates (2° off towards the nearest [111] plane) using standard precursors including trimethyl gallium, AsH_3, trimethyl aluminium, dimethylzinc and Si_2H_6. The multilayer structures for single-junction solar cells were composed of three repeats of n-type GaAs (200 nm, (4–5) $\times 10^{18}$ cm^{-3}, Si-doped), n-type $Al_{0.4}Ga_{0.6}As$ (40 nm, 2×10^{18} cm^{-3}, Si-doped), n-type GaAs (100 nm, 2×10^{18} cm^{-3}, Si-doped), p-type GaAs (2 μm, 3×10^{17} cm^{-3}, Zn-doped), p-type $Al_{0.3}Ga_{0.7}As$ (100 nm, 1×10^{19} cm^{-3}, Zn-doped), p-type GaAs (2 μm, 4×10^{19} cm^{-3}, Zn-doped) and $Al_{0.95}Ga_{0.05}As$ (1.0 μm).

Multilayer release and assembly. Vertical etching through the entire thickness of a multilayer stack in a mixture of citric acid (100 g of citric acid monohydrate (Sigma-Aldrich); 83 ml of deionized water) and hydrogen peroxide (H_2O_2, 30%, Fisher Scientific) at a 10:1 volume ratio, followed by removal of the AlAs in HF, yielded solution suspensions of released GaAs structures. Subsequent assembly onto a target substrate provided one route to devices. For work reported here, vertical etching of trenches through the top GaAs layer (or GaAs, AlGaAs stack) and partially into the underlying AlAs layer by brief immersion in HF created a slight undercut around the periphery of the trenches. A layer of photoresist formed structures that tethered fully released pieces of GaAs to the underlying wafer after complete etching of the AlAs. Techniques of transfer printing were used to integrate the released GaAs structures onto substrates of interest. Repetitive application of this sequence of steps completed the process. The Supplementary Information provides additional details.

MESFETs and logic circuits. Etching according to procedures described above prepared the GaAs source wafer (Fig. 1a) for delivery of organized collections of GaAs membranes to a glass substrate coated with a partially cured layer of polyimide. Removing residual photoresist with acetone, and fully curing the polyimide by baking at 250 °C for 2 h completed the process. A sequence of photolithography, electron beam evaporation and annealing steps yielded ohmic source and drain electrodes (Pd/Ge/Au (5/35/80 nm); 175 °C for 60 min) and Schottky gate electrodes (Ti/Au (10/100 nm)) to form the MESFETs. Similar procedures formed interconnects for the logic gates. d.c. measurements of MESFETs were carried out using a semiconductor parameter analyser (Agilent, 4155C). High frequency measurement used a network analyser (Agilent, 8720) calibrated with a standard-open-load-through technique. The Supplementary Information provides additional details.

NIR imagers. Ohmic and Schottky contacts used Pd/Ge/Au (5/35/80 nm, annealed at 175 °C for 60 min) and Ti/Au (30/100 nm), respectively. Wet etching with a mixture of citric acid and hydrogen peroxide at a 10:1 volume ratio removed the n-type GaAs layer. A photodefinable epoxy (SU8, Microchem) served as a support structure for interconnecting metal lines and as an encapsulation layer. After etching the AlAs in concentrated HF, the entire NIR imager array was transferred to a silicon wafer coated with a photocurable polyurethane as an adhesive (NOA 61, Norland Products). Electrical measurements of individual pixels were conducted using a semiconductor parameter analyser (Agilent, 4155C). The detector was mounted in a printed circuit board and connected to a computer for image acquisition. The Supplementary Information provides additional details.

Solar cells and flexible modules. The p-type bottom contact layer was exposed by etching with mixtures of citric acid and hydrogen peroxide at different volume ratios (citric acid:H_2O_2 = 10:1 and 4:1) in a sequential manner. Next, most of the top contact layer except the area for the ohmic contact was selectively etched away with a 4:1 mixture of citric acid and hydrogen peroxide. Etching with a 10:1 mixture of citric acid and hydrogen peroxide provided isolation of individual cells. Ohmic contacts for both top and bottom contact layers were then formed by electron beam evaporation of Pd/Ge/Au (5/35/80 nm) and Pt/Ti/Pt/Au (10/40/10/80 nm) for n-type and p-type contacts, respectively. Annealing at 175 °C under N_2 atmosphere was used for the n-type ohmic contact. Before the *I*/*V* measurements on the source wafer, Si_3N_4 (thickness: ~80 nm, $n \approx 1.76$) was deposited by plasma enhanced chemical vapour deposition (PlasmaTherm SLR) as a single-layer ARC. Arrays of the resulting cells were undercut-etched in HF and transfer printed to PET substrates using a photodefinable epoxy (SU8, Microchem) as an adhesive. Patterning holes through the SU8 followed by lift-off of metals (Cr/Au: 10/300 nm) deposited by sputtering formed interconnects. Encapsulating with SU8 completed the entire process. *I*/*V* measurements were carried out using a d.c. source meter (Keithley, 2400) and a 1,000 W full-spectrum solar simulator (Oriel, 91192). External and internal quantum efficiencies of GaAs solar cells on the source wafer were measured using an automated spectroradiometer system (Optronic Lab., OL-750) in the wavelength range of 280–1,100 nm with 10 nm resolution. The Supplementary Information provides additional details.

Table of Contents

Supplementary Methods

Processing scheme for GaAs MESFETs (Figure S1)

Hole etching

1. Clean a GaAs source wafer (acetone, isopropyl alcohol (IPA), deinoized (DI) water).
2. Spin-coat photoresist (PR; Clariant AZ5214, 3000 rpm, 30 s) and soft-bake at 110 °C for 1 min.
3. Expose with 365 nm optical lithography (Karl Suss MJB3) through an iron oxide mask.
4. Develop in aqueous base developer (Clariant AZ327 MIF) and post-bake on a hot plate (110°C, 3 min).
5. Etch oxide in HCl:DI water (1:1, by volume) for 30 s and rinse with DI water.
6. Etch GaAs in a mixture of citric acid (100 g of citric acid monohydrate (Sigma-Aldrich) in 83ml DI water) and hydrogen peroxide (H_2O_2) (10:1, by volume) for 2 min.

Isolation

7. Clean the processed wafer in step 6 (acetone, IPA, DI water).
8. Pattern PR (step 2-4).
9. Etch oxide in HCl:DI water (1:1 by volume) for 30 s and rinse with DI water.
10. Etch GaAs in a mixture of citric acid and H_2O_2 (10:1) for 2 min.

Sacrificial layer ($Al_{0.95}Ga_{0.05}As$) partial etching

11. Etch in diluted HF (49% HF in DI water, 20:1 by volume) for 20 s.

Forming PR support layer and undercut etching

12. Clean the processed wafer in step 11 (acetone, IPA, DI water).
13. Pattern PR (step 2-4).
14. Etch in diluted HF (20:1) for 1 h.

Printing onto glass substrate

15. Lift-off GaAs using a flat polydimethylsiloxane (PDMS) (Sylgard 184, Dow Corning) stamp.

16. Transfer print GaAs onto a substrate coated with a partially cured polyimide (PI2525, HD Microsystems, spun at 600 rpm/5 s, 4000 rpm/40 s, baked on a hot plate at 110°C for 40 s).
17. Bake on a hot plate at 150°C for 1 min.
18. Remove PR with acetone, IPA, DI.
19. Bake on a hot plate at 250°C for 2 h in N_2 ambient.

Active area defining

20. Clean the processed sample in step 19 (acetone, IPA, DI water).
21. Pattern PR (step 2-4).
22. Etch oxide in HCl:DI water (1:1 by volume) for 30 s and rinse with DI water.
23. Etch GaAs in a mixture of citric acid and H_2O_2 (10:1) for 2 min.

Channel etching

24. Clean the processed sample in step 23 (acetone, IPA, DI water).
25. Pattern PR (step 2-4).
26. Etch oxide in HCl:DI water (1:1 by volume) for 30 s and rinse with DI water.
27. Etch GaAs in a mixture of citric acid and H_2O_2 (10:1) for 30 s.

Ohmic contact metallization

28. Clean the processed sample in step 27 (acetone, IPA, DI water).
29. Pattern PR (step 2-4 but no post-bake).
30. Etch oxide in HCl:DI water (1:1 by volume) for 30 s (no rinse).
31. Deposit 5/35/80 nm of Pd/Ge/Au by electron beam evaporation.
32. Lift-off metal in acetone.
33. Anneal at 175°C for 1 h in N_2 ambient.

Schottky contact metallization

34. Clean the processed sample in step 33 (acetone, IPA, DI water).
35. Pattern PR (step 2-4 but no post-bake).
36. Etch oxide in HCl:DI water (1:1 by volume) for 30 s (no rinse).
37. Deposit 10/100 nm of Ti/Au by electron beam evaporation.

38. Lift-off metal in acetone.

Processing scheme for GaAs NIR imagers (Figure S9)

Ohmic contact metallization

1. Clean a GaAs source wafer (acetone, IPA, DI water).
2. Pattern PR (step 2-4 but no post-bake).
3. Etch oxide in HCl:DI water (1:1 by volume) for 30 s (no rinse).
4. Deposit 5/35/80 nm of Pd/Ge/Au by electron beam evaporation.
5. Lift-off metal in acetone.
6. Anneal at 175°C for 1 h in N_2 ambient.

N-doped layer etching

7. Clean the processed wafer in step 6 (acetone, IPA, DI water).
8. Pattern PR (step 2-4).
9. Etch oxide in HCl:DI water (1:1 by volume) for 30 s and rinse with DI water.
10. Etch GaAs in a mixture of citric acid and H_2O_2 (10:1) for 40 s.

Schottky contact metallization

11. Clean the processed wafer in step 10 (acetone, IPA, DI water).
12. Pattern PR (step 2-4 but no post-bake).
13. Etch oxide in HCl:DI water (1:1 by volume) for 30 s (no rinse).
14. Deposit 10/100 nm of Ti/Au by electron beam evaporation.
15. Lift-off metal in acetone.

Hole etching and isolation

16. Clean the processed wafer in step 15 (acetone, IPA, DI water).
17. Pattern PR (step 2-4).
18. Etch oxide in HCl:DI water (1:1 by volume) for 30 s and rinse with DI water.
19. Etch GaAs in a mixture of citric acid and H_2O_2 (10:1) for 3 min.

Sacrificial layer ($Al_{0.95}Ga_{0.05}As$) partial etching

20. Clean the processed wafer in step 19 (acetone, IPA, DI water).

21. Pattern PR (step 2-4).

22. Etch in diluted HF (49% HF in DI water, 20:1 by volume) for 35 s.

Forming PR support layer

23. Clean the processed wafer chip in step 22 (acetone, IPA, DI water).

24. Spin-coat with epoxy (SU8-2, spun at 3000 rpm for 30 sec). Soft bake at 65°C and 110°C.

25. Pattern epoxy by exposing to UV, baking, developing, rinsing and curing.

Interconnect metallization

26. Clean the processed wafer in step 25 (acetone, IPA, DI water).

27. Pattern PR (step 2-4 but no post bake).

28. Deposit 30/220 nm of Ti/Au by electron beam evaporation.

29. Lift-off metals in acetone.

Forming encapsulating layer

30. Clean the processed wafer in step 29 (acetone, IPA, DI water).

31. Spin-coat with epoxy (SU-8 2, spun at 3000 rpm for 30 sec). Soft bake at 65°C and 110°C.

32. Pattern epoxy by exposing to UV, baking, developing, rinsing and curing.

Undercut etching

33. Etch in diluted HF (100:1) for 4 h 30 min.

Printing the GaAs NIR imager arrays

34. Lift-off GaAs arrays using a flat PDMS stamp.

35. Transfer print GaAs arrays onto a substrate coated with optical adhesive (NOA 61, Norland Products Inc.).

36. Cure under UV for 1 h.

Processing scheme for GaAs 1J solar cells (Figure S12)

Bottom contact exposure

1. Clean a source wafer (acetone, IPA, DI water).
2. Pattern PR (step 2-4).
3. Etch oxide in HCl:DI water (1:1 by volume) for 15 s and rinse with DI water.
4. Etch GaAs in a mixture of citric acid and H_2O_2 (10:1) for 8 min 30 s with no DI rinse.
5. Etch GaAs in a mixture of citric acid and H_2O_2 (4:1) for 20 min.
6. Etch oxide in HCl:DI water (1:1 by volume) for 5 s and rinse with DI water.
7. Etch GaAs in a mixture of citric acid and H_2O_2 (10:1) for 1 min 30 s and rinse with DI water.

Top contact etching

8. Clean the processed wafer in step 7 (acetone, IPA, DI water).
9. Pattern PR (step 2-4).
10. Etch oxide in HCl:DI water (1:1 by volume) for 30 s and rinse with DI water.
11. Etch GaAs in a mixture of citric acid and H_2O_2 (4:1) for 50 s.

Hole etching

12. Clean the processed wafer in step 11 (acetone, IPA, DI water).
13. Pattern PR (step 2-4).
14. Etch oxide in HCl:DI water (1:1 by volume) for 30 s and rinse with DI water.
15. Etch GaAs in a mixture of citric acid and H_2O_2 (10:1) for 32 min.

Isolation

16. Clean the processed wafer in step 15 (acetone, IPA, DI water).
17. Pattern PR (step 2-4).
18. Etch oxide in HCl:DI water (1:1 by volume) for 30 s and rinse with DI water.
19. Etch GaAs in a mixture of citric acid and H_2O_2 (10:1) for 32 min.

Sacrificial layer ($Al_{0.95}Ga_{0.05}As$) partial etching

20. Etch in diluted HF (49% HF in DI water, 20:1 by volume) for 1 min.

Top contact metallization

21. Clean the processed wafer in step 20 (acetone, IPA, DI water).

22. Pattern PR (step 2-4 but no post-bake).
23. Etch oxide in HCl:DI water (1:1 by volume) for 30 s (no rinse).
24. Deposit 5/35/80 nm of Pd/Ge/Au by electron beam evaporation.
25. Lift-off metal in acetone.
26. Anneal at 175°C for 1 h in N_2 ambient.

Bottom contact metallization

27. Clean the processed sample in step 26 (acetone, IPA, DI water).
28. Pattern PR (step 2-4 but no post-bake).
29. Etch oxide in HCl:DI water (1:1 by volume) for 30 s (no rinse).
30. Deposit 10/40/10/80 nm of Pt/Ti/Pt/Au by electron beam evaporation.
32. Lift-off metal in acetone.

Forming PR support layer and undercut etching

33. Clean the processed wafer in step 32 (acetone, IPA, DI water).
34. Pattern PR (step 2-4).
35. Etch in diluted HF (20:1) for 2 h 30 min.

Printing onto polyethyleneterephthalate (PET) substrate

36. Lift-off GaAs using a flat PDMS (Sylgard 184, Dow Corning) stamp.
37. Clean a PET substrate (thickness: ~50 μm) in acetone, IPA, and DI water.
38. Expose to ultraviolet induced ozone (UVO) for 10 min.
39. Spin-coat SU8-2 (600 rpm/5 s, 3000 rpm/30 s) and soft-bake at 65°C for 12 s.
40. Print and UV exposure for 30 s.
41. Post-bake at 65°C for 1 min and 95°C for 2 min.
42. Retrieve the stamp and post-bake at 110°C for 7 min.
43. Remove PR in acetone.

Via hole patterning

44. Clean the processed sample in step 43 (acetone, IPA, DI water).
45. Expose to UVO for 40 min.
46. Spin-coat SU8-2 (600 rpm/5 s, 1500 rpm/30 s) and soft-bake at 65°C for 1 min and 95°C

for 3 min 30 s.

47. UV exposure and post- bake at 65°C for 1 min and 95°C for 1 min.

48. Develop in aqueous base developer (SU8 developer, Microchem).

49. Post-bake at 110°C for 20 min.

Interconnect metallization

50. Clean the processed sample in step 49 (acetone, IPA, DI water).

51. Spin-coat lift-off PR (AZnLOF2070, Clariant, 600 rpm/5 s, 4000 rpm/ 30s) and soft-bake at 110°C for 90 s.

52. UV exposure and post-exposure-bake at 110°C for 90 s.

53. Develop in AZ327 MIF for 120 s.

54. O_2 reactive ion etching (20 sccm, 50 mTorr, 150 W, 1 min).

55. Deposit 30/350 nm of Cr/Au by sputter coater (AJA international).

56. Lift-off metal in acetone.

Encapsulation

57. Clean the processed sample in step 56 (acetone, IPA, DI water).

58. Expose to UVO for 30 min.

59. Spin-coat SU8-2 (600 rpm/5 s, 1500 rpm/30 s) and soft-bake at 65°C for 1 min and 95°C for 3 min 30 s.

60. UV exposure and post- bake at 65°C for 1 min and 95°C for 1 min.

61. Develop in SU8 developer for 1 min 30 s.

62. Post-bake at 110°C for 20 min.

Imaging with NIR imagers

Figure S10(a) provides a photograph of the optical setup for image acquisition with the NIR imagers. For the NIR source, an infrared LED lamp (IR045, Clover electronics) was used. As target images, both lithographically patterned chromium masks and machined metal stencils were used to achieve perfect blocking of NIR in the metal regions. For imaging optics, a plano-convex lens (diameter of 9 mm and focal length of 22.8 mm, JML Optical Industries, Inc) was used. Figure S10(b) shows images of the NIR source and a target image at different illumination conditions taken by a digital camera (Powershot A620,

Canon). The discrete nature of LED arrays in the NIR source (upper left figure) is evident in the target image (upper right figure). To avoid such aspects, a diffuser (commercial quality sandblasted glass 50 mm x 50 mm, Edmund optics) was placed between the source and the target image. The distance between the diffuser and the source was set at 30 mm, the minimum distance needed to obtain fully diffused light.

Secondary ion mass spectrometry (SIMS)

Dynamic secondary ion mass spectrometry (SIMS) experiments for GaAs/AlAs multilayers (Figure 1b, S5 and S8) were performed on a Cameca ims 5f instrument at Frederick-Seitz Materials Research Laboratory at UIUC. Atomic depth profiles were obtained using a 10 kV Cs+ beam with a current of 40 nA, which was rastered over a 250 μm square. Negative secondary ions were collected with an electron multiplier for the Al and Ga signals and with a faraday cup for the As signal. The depth of the SIMS crater was measured on a Dektak3 ST stylus profilometer. Dynamic SIMS measurements for triple stack GaAs solar cells (Figure S15) were conducted by Evans Analytical Group. Atomic concentrations of Al and Zn through the sample thickness were obtained from measured positive secondary ion signals using 3keV Cs+ beam, and the crater depth measured on a Tencor P10 stylus profilometer.

Supplementary Note and Discussion

***IV* characteristics of 3rd layer GaAs solar cells**

IV characteristics for the 3rd (bottom) layer device shown in Figure 4c and 4d were obtained only from cells that exhibit a good diode response. About 50% of the probed cells at 3rd layer showed poor or no diode response, possibly due to the effect of Zn diffusion near the junction area (Figure S15).

Estimation of GaAs solar cell efficiency with a double layer ARC

The efficiencies of single junction GaAs solar cells (in the top and middle layers) with a double layer ARC under AM 1.5D illumination were estimated based on measured internal quantum efficiency (IQE) and AM 1.5D reference solar spectrum (Figure 4f). First, external quantum efficiencies (EQE) of top and middle layer GaAs solar cells with a double

layer ARC were obtained from measured IQE and calculated transmission spectra of double layer antireflection coating (MgF_2/ZnS) (Figure S16). Multiplying such EQE values to the current density at each wavelength (derived from AM 1.5D reference solar irradiance (ASTMG 173 D+C)), and integrating them over an entire wavelength (280-1100 nm) gave total current densities of ~27.4 mA/cm^2 and ~26.1 mA/cm^2 for top and middle layer devices, respectively. Energy conversion efficiencies of these GaAs solar cells with double layer ARC were then calculated using the total current density as J_{sc}, and experimentally obtained V_{oc} and FF.

Calculation of transmission spectra of a double layer ARC

Normal incidence transmission spectra (Figure S16) of a double layer ARC (MgF_2: 105 nm, ZnS: 55 nm) through $Al_{0.4}Ga_{0.6}As$ window layer were calculated using a commercial software (GD-calc®, KJ Innovation), where optical constants (n and k) of MgF_2, ZnS and $Al_{0.4}Ga_{0.6}As$ were obtained from a website (http://www.ioffe.ru/SVA/NSM/).

Cost and throughput analysis of multilayer approach

The total cost of epilayer growth, C_T, can be separated into three parts. The first is C_W, the cost of the growth wafer. The second is C_S, the summed cost of the growth system (except the cost of source materials consumed during the growth), which consists of the cost associated with personnel, the cost of ownership and equipment depreciation, the cost of utilities and materials for loading and unloading, and for stand-by periods between growth of different epilayers and the cost of carrier gas during the growth. The third is C_M, the cost of source materials (metal organics) consumed for the growth of epilayers.

$$\text{Total cost } (C_T) = \text{Wafer cost } (C_W) + \text{System cost } (C_S) + \text{Materials cost } (C_M) \quad (1)$$

To quantify the cost and throughput benefits of the multilayer approach, we define following parameters:

N: number of device layers (n.b. one device layer can comprise multiple epilayers, depending on the device design)
A: total time to load and unload a substrate in the growth chamber (min)
B: time to grow a device layer (min)

B′: time to grow a sacrificial layer (min)

T: total time of use of the growth system (min) (time for load/unload + time for growth)

R: rate of operation costs of the growth system ($/h) (we assume a single operation rate that applies to the use of the system for growth and for load/unload)

M: cost of metal-organic source materials to grow a device layer ($)

M′: cost of metal-organic source materials to grow a sacrificial layer ($)

W: cost of a wafer ($).

W′: cost of reusing a wafer = p·W (where p is typically ~0.2-0.3) ($)

We consider two cases. Case 1 corresponds to the standard commercial process, in which a single device layer is grown on a wafer that is not reused. Case 2 corresponds to the multilayer and printing concepts described in this manuscript, where N device layers are grown on a wafer that is reused.

We examine the costs to create the same total amount of device material via Case 1 and Case 2. We take this total as that formed by growth on N wafers for Case 1, and N layers for Case 2. The total times (T) for the growth in these two cases are

$$T_1 \text{ (T for case 1)} = (A + B)\cdot N \quad (2)$$

$$T_2 = A + (B + B')\cdot N \quad (3)$$

Dividing these times by N gives the total time for the use of growth system for the growth of a single device layer according to

$$T_1/N = A + B \quad (4)$$

$$T_2/N = A/N + B + B' \quad (5)$$

Reciprocal values of eqn. (4) and (5) yield the throughput (TP) of the growth system, as defined by the number of device layers per total time of usage of the growth system:

$$TP_1 = 1/(A + B) \quad (6)$$

$$TP_2 = 1/(A/N + B + B') \quad (7)$$

The throughput for the standard approach remains fixed with N. The throughput for the multilayer approach, on the other hand, increases with N, as is evident from eqns. (6) and (7).

Multiplying eqns. (2) and (3) by R gives values for C_S according to

$$C_{S1} = R\cdot(A + B)\cdot N \quad (8)$$

$$C_{S2} = R\cdot(A + B\cdot N + B'\cdot N) \quad (9)$$

Case 1 consumes N growth wafers. Case 2 consumes none, but it incurs the cost of one reusing process.

$$C_{W1} = W\cdot N \quad (10)$$

$$C_{W2} = W' = p\cdot W \quad (11)$$

The cost of source materials for Case 1 and Case 2 can be expressed by following equations:

$$C_{M1} = M\cdot N \quad (12)$$

$$C_{M2} = (M + M')\cdot N \quad (13)$$

Combining eqns. (8)-(13) yields values for C_T according to

$$C_{T1} = W\cdot N + R\cdot (A + B)\cdot N + M\cdot N = [W + R\cdot(A + B) + M]\cdot N \quad (14)$$

$$C_{T2} = W' + R\cdot(A + B\cdot N + B'\cdot N) + (M + M')\cdot N$$
$$= p\cdot W + R\cdot(A + B\cdot N + B'\cdot N) + (M + M')\cdot N \quad (15)$$

Subtracting eqns. (14) and (15) yields the difference in cost between these two cases.

$$C_{T1} - C_{T2} = W \cdot N + R \cdot (A + B) \cdot N + M \cdot N - [p \cdot W + R \cdot (A + B \cdot N + B' \cdot N) + (M + M') \cdot N]$$
$$= (N - p) \cdot W + R \cdot A \cdot (N - 1) - R \cdot B' \cdot N - M' \cdot N$$
$$= (W + R \cdot A - R \cdot B' - M') \cdot N - p \cdot W - R \cdot A \quad (16)$$

As shown in eqn. (16), the cost benefit increases with N, without bound, independent of device specifications.

In the limit of large N, eqn. (16) can be written as follows:

$$C_{T1} - C_{T2} \cong (W + R \cdot A - R \cdot B' - M') \cdot N \quad (17)$$

If the sacrificial layer is thin enough such that $W + R \cdot A >> R \cdot B' + M'$, then eqn. (17) can be further simplified according to

$$C_{T1} - C_{T2} \cong (W + R \cdot A) \cdot N \quad (18)$$

In this limiting case of large N and a thin sacrificial layer, the cost difference between these two cases is equal to N times the sum of the cost of the wafer and the cost of the growth system for the loading and unloading processes.

Dividing eqns. (14) and (15) by N yields the total cost for growing a single device layer, or the total cost per device. In the standard approach, the total cost per device remains constant:

$$C_{T1}/N = [W + R \cdot (A + B) + M] \quad (19)$$

For the multilayer approach, by contrast, the total cost per device decreases with N and reaches a minimum defined by the cost of growth system and the cost of source materials for growth of a single device layer:

$$C_{T2}/N = (p \cdot W + R \cdot A)/N + [R \cdot (B + B') + M + M']$$

$$\cong [R\cdot(B + B') + M + M'] \text{ (for large N)} \quad (20)$$

Another feature apparent from eqns. (11) and (15) is that for the multilayer approach, the cost of the wafer, compared to the total cost, becomes negligible for N sufficiently large:

$$C_{W2}/C_{T2} = p\cdot W/[p\cdot W + R\cdot(A + B\cdot N + B'\cdot N) + (M + M')\cdot N] \quad (21)$$

By contrast, the wafer cost remains a fixed, large fraction of the total cost in the standard approach:

$$C_{W1}/C_{T1} = W\cdot N/[W + R\cdot(A + B) + M]\cdot N = W/[W + R\cdot (A + B) + M] \quad (22)$$

Next, we examine quantitative costs and throughputs for device examples in MESFETs and solar cells. The following are estimates for the key parameters, determined from information provided by *Epiworks*:

- A = 60 min.
- R = $125/h.
- W = $100 (for 4 inch diameter).
- p = 0.25

We assume that the thickness of the sacrificial layer is 20 nm, as demonstrated to be experimentally feasible in the new 40 layer system that we added in revisions.

The growth time (B) per device can be estimated from the total thicknesses of GaAs and AlGaAs, and their growth rates (0.041 μm/min for GaAs; 0.065 μm/min for AlGaAs; we assume the growth rate of AlGaAs is constant with the Al composition) as summarized in Table S2.

From Table S2, B(MESFET), B(Solar cell) and B′ are as follows:

B(MESFET) = 4.9 min.

B(Solar cell) = 106.6 min.

B′ = 0.3 min.

The cost of the source materials (M) per device can be estimated from thicknesses of epilayers and their growth cost per thickness: \$2.11/μm for GaAs, \$2.20/μm for $Al_{0.95}GaAs$, and \$1.89/μm for Al_xGaAs ($0<x<0.5$).

M(MESFET) = (2.11)·(0.2) = \$0.42

M(Solar cell) = (2.11)·(4.3) + (1.89)·(0.14) = \$9.34

M′ = (2.20)·(0.02) = \$0.04

With these key parameters obtained above, we examine quantitative costs and throughputs for device examples in MESFETs and solar cells.

For MESFETs,

$$C_{T1} = [W + R\cdot(A + B) + M]\cdot N$$
$$= [100 + 125/60\cdot(60 + 4.9) + 0.42]\cdot N = \mathbf{\$235.63\cdot N} \quad (23)$$

$$C_{T2} = p\cdot W + R\cdot(A + B\cdot N + B'\cdot N) + (M + M')\cdot N$$
$$= p\cdot W + R\cdot A + R\cdot B\cdot N + R\cdot B'\cdot N + (M + M')\cdot N$$
$$= 0.25\cdot 100 + 125/60\cdot 60 + 125/60\cdot 4.9\cdot N + 125/60\cdot 0.3\cdot N + 0.46\cdot N$$
$$= \mathbf{\$11.29\cdot N + \$150} \quad (24)$$

$$C_{T1}\text{-}C_{T2} = (W + R\cdot A - R\cdot B' - M')\cdot N - p\cdot W - R\cdot A$$
$$= (100 + 125/60\cdot 60 - 125/60\cdot 0.3 - 0.04)\cdot N - 0.25\cdot 100 - 125/60\cdot 60$$
$$= \mathbf{\$224.34\cdot N - \$150} \quad (25)$$

$$C_{T1}/N = [W + R\cdot(A + B) + M]$$
$$= [100 + 125/60\cdot(60 + 4.9) + 0.42] = \mathbf{\$235.63} \quad (26)$$

$$C_{T2}/N = (p\cdot W + R\cdot A)/N + [R\cdot(B + B') + M + M']$$
$$= (0.25\cdot 100 + 125/60\cdot 60)/N + [125/60\cdot(4.9 + 0.3) + 0.42 + 0.04]$$
$$= \mathbf{\$150/N + \$11.29} \quad (27)$$

$$C_{W1}/C_{T1} = W\cdot N/[W + R\cdot(A + B) + M]\cdot N = W/[W + R\cdot(A + B) + M]$$
$$= 100/[100 + 125/60\cdot(60 + 4.9) + 0.42]$$
$$= \mathbf{0.424} \quad (28)$$

$$C_{W2}/C_{T2} = p\cdot W/[p\cdot W + R\cdot(A + B\cdot N + B'\cdot N) + (M + M')\cdot N]$$
$$= 0.25\cdot 100/[0.25\cdot 100 + 125/60\cdot 60 + (125/60\cdot 5.2 + 0.46)\cdot N$$
$$= \mathbf{25/(11.29\cdot N + 150)} \quad (29)$$

$$TP_1 = 1/(A + B) = \mathbf{1/(60 + 4.9)\ min^{-1}} \quad (30)$$

$$TP_2 = 1/(A/N + B + B') = \mathbf{1/(60/N + 5.2)\ min^{-1}} \quad (31)$$

For solar cells,

$$C_{T1} = [W + R\cdot(A + B) + M]\cdot N$$
$$= [100 + 125/60\cdot(60 + 106.6) + 9.34]\cdot N = \mathbf{\$456.42\cdot N} \quad (32)$$

$$C_{T2} = p\cdot W + R\cdot(A + B\cdot N + B'\cdot N) + (M + M')\cdot N$$
$$= p\cdot W + R\cdot A + R\cdot B\cdot N + R\cdot B'\cdot N + (M + M')\cdot N$$
$$= 0.25\cdot 100 + 125/60\cdot 60 + 125/60\cdot 106.6\cdot N + 125/60\cdot 0.3\cdot N + 9.37\cdot N$$
$$= \mathbf{\$232.08\cdot N + \$150} \quad (33)$$

$$C_{T1}\text{-}C_{T2} = \mathbf{\$224.34\cdot N - \$150} \quad (34)$$

Note the cost difference is the same as the case for MESFET.

$$C_{T1}/N = [W + R\cdot(A + B) + M]$$
$$= [100 + 125/60\cdot(60 + 106.6) + 9.34] = \mathbf{\$456.42} \quad (35)$$

$$C_{T2}/N = (p\cdot W + R\cdot A)/N + [R\cdot(B + B') + M + M']$$
$$= (0.25\cdot 100 + 125/60\cdot 60)/N + [125/60\cdot(106.6 + 0.3) + 9.34 + 0.04]$$
$$= \mathbf{\$150/N + \$232.08} \quad (36)$$

$$C_{W1}/C_{T1} = W/[W + R\cdot(A + B) + M]$$
$$= 100/[100 + 125/60\cdot(60 + 106.6) + 9.34]$$
$$= \mathbf{0.219} \quad (37)$$

$$C_{W2}/C_{T2} = p\cdot W/[p\cdot W + R\cdot(A + B\cdot N + B'\cdot N) + (M + M')\cdot N]$$
$$= 0.25\cdot 100/[0.25\cdot 100 + 125/60\cdot 60 + (125/60\cdot 106.9 + 9.37)\cdot N]$$
$$= \mathbf{25/(232.08\cdot N + 150)} \quad (38)$$

$$TP_1 = 1/(A + B) = \mathbf{1/(60 + 106.6)\ min^{-1}} \quad (39)$$

$$TP_2 = 1/(A/N + B + B') = \mathbf{1/(60/N + 106.9)\ min^{-1}} \quad (40)$$

As shown in Figure S20(a), the total cost benefit (C_{T1}-C_{T2}) of the multilayer approach increases linearly with number of device layers (N), independent of device specifications. In the system of relatively thin epilayer devices such as MESFET, the total cost for device material obtained using the multilayer approach, for the case of the new, experimentally demonstrated 40 layer system, is reduced by more than 15 times that for the standard approach as shown in Figure S20(b). This reduction equals to a 93.6% decrease in cost.

The total cost per device (C_{T2}/N) of the multilayer approach also decreases with N, and reaches a minimum at large N as illustrated in Figure S20(c). This minimum value corresponds to the cost of growth system and source materials during the growth itself. In the 40 layer system of MESFETs, the total cost per device decreases to 6.4% of the total cost per device in the standard approach, with a minimum that is 4.8%.

The ratio of the wafer cost to the total cost in the multilayer approach decreases with N and becomes negligible for N sufficiently large as shown in eqns. (29) and (38). For the 40 layer system of MESFETs, the percentage of the cost associated with the wafer (i.e. the ratio of wafer cost to total cost, times 100%) decreases from 42.4% (eqn. (28)) for the standard

approach, to only 4.2% for the multilayer approach.

Lastly, the throughput (TP) of the growth system increases with N for the multilayer approach. Figure S20(d) shows the ratio of the throughputs (TP_2/TP_1), as a function of N. For the 40 layer system of MESFETs, the throughput of the multilayer approach increases by nearly a factor of ten over the standard approach.

In summary, this analysis of cost quantifies many key aspects of the multilayer approach, as follows.

- The total cost benefit increases linearly with number of device layers (N), independent of device specifications. In the limit of large N and thin sacrificial layers, the cost benefit compared to the standard approach equals N times the sum of the cost of wafer substrate and the cost of growth system for loading and unloading processes.

- The total cost per device decreases with N, and reaches a minimum at large N that corresponds to the cost of the source materials and the usage of the growth system during the growth period itself.

- The percentage cost associated with the wafer decreases with N and becomes negligible for large N.

- The throughput of the growth system increases with N.

- For the experimentally demonstrated 40 layer system of MESFETs for RF electronics, the multilayer approach reduces the cost of the device material by more than 15 times and increases the throughput by nearly 10 times, compared to the standard approach.

- For both MESFETs and solar cells, the multilayer approach reduces the fractional cost associated with the wafer from a significant value (i.e. ~40% and ~22%, respectively) to a negligible one (i.e. ~4% for N = 40, and ~3% for N =3, respectively) compared to the standard approach.

- For both MESFETS and solar cells, the limit of large N referenced above obtains at modest values of N~5-10.

Technical issues of multilayer epitaxial growth

The practical limit on how many layers of the active structure can be epitaxially grown is set by factors that deteriorate as the stack becomes thicker, including layer morphologies, doping profiles and differential stresses. Carefully managing these effects can enable successful growth of thick layers with many repeats. As an example, the morphology of high composition $Al_xGa_{1-x}As$ layers degrades with increasing thickness as a result of point defects and impurities. Nevertheless, by reducing the AlGaAs thickness, we can achieve large numbers of layers, demonstrated to 40 repeats in the Fig. 1. Doping profiles can also change during the growth, due to thermally activated diffusion associated with high concentration gradients, or to p-n junction induced diffusion. In the MESFET structure, the active layer is doped with Si, which has a very small diffusion constant in GaAs. For this stack, even very long growth times are not expected to affect the doping profiles. The challenges are more pronounced for more complex device stacks, such as those used for the solar cells. Here, the Zn clearly diffuses for prolonged growth times. A solution to this problem might involve a change to less diffusive C for the p-type dopant, or the use of intentionally compensated Zn concentration and profile throughout the stack. Warping or bowing can occur in thick films due to strains induced by lattice and/or thermal mismatch or by thickness and/or temperature nonuniformities across the wafer. For the examples presented here, we did not observe problems associated with bowing, likely because our structures are all lattice matched, our wafers and printed device elements are both relatively small.

Metallization schemes for GaAs solar cells

The metallization schemes presented in this manuscript, including choice of materials and grid designs, illustrate the concepts in functioning systems; they are not optimized for a particular application or for low-cost implementation[1-2].

Total area efficiency vs. active area efficiency

The total area efficiency is lower than the active area efficiency by about 18% for the reported designs. With improved lithography, we believe that we can reduce this gap to

about 11%. This value decreases further to 2.75%, for example, with an increase in cell size from 500 μm to 1000 μm. These general approaches can be used in concentrating or non-concentrating systems. The current cells serve as demonstrators and are not optimized for a particular application.

Studies of the size scaling of cell performance

We performed scaling studies involving performance measurements on a range of cell sizes (no ARC), from 200 x 200 μm^2 to 2 x 2 mm^2. The cells had square geometries with edge lengths, *d*, of 200, 300, 400, 500, 600, 800, 1000, 2000 μm). Two metal contacts on opposite edges had dimensions of *d* x 40 μm^2, as schematically shown in Fig. S18(a). Figure S18(b) shows the efficiencies based on the active area (i.e. excluding contact areas) and the total area (i.e. including contact areas) of cells as a function of cell size (i.e. *d*). The active area efficiencies slightly increase as *d* increases from 200 μm to 600 μm and then slightly decrease for *d* larger than 600 μm. The total area efficiencies increase with the cell size due to increased fraction of the active area over the total area (in other words, due to decreased fraction of metal contact areas). The active area efficiency approaches the total area efficiency as the cell size increases. Similar trends are observed for V_{oc} (Figure S18 (c)). We speculate that the slight degradation in performance as *d* decreases below 600 μm is due, in some part, to the effect of the edge recombination. The slight degradation as *d* increases beyond 600 μm results partly from non-optimized metal grid designs. Both effects change the efficiency by only ~1%.

Fabrication of GaAs solar cells with conventional dimensions by transfer printing

The etching, liftoff and printing schemes apply equally well to larger devices. To demonstrate this capability, we formed large solar cells (~10 mm x ~10 mm) with a simple metal grid design. Figure S19(a) shows an image of such a cell printed on a glass substrate. In related experiments, we also demonstrated even larger printed cells (25.4 mm x 25.4 mm) on a Si wafer. An image of two such cells, without contacts, appears in Figure S19(b). Sizes in this range are comparable to those of conventional devices, thereby enabling the use of established contact schemes and other design aspects.

Solar cell designs in Figure 4

Current designs of 1J solar cells in Fig. 4 are for the purpose of demonstration. With suitable cell configurations and module designs, the ideas can be useful for high or low concentration applications, on flexible or rigid substrates.

Commercial development of printing tools

Commercial efforts are already underway at small and large companies to develop transfer printing and single layer schemes for applications in photovoltaics, display and other areas of semiconductor manufacture. Figure S21 shows printing tools of the latest generation for commercial applications. In its current configuration, the tools for transfer printing are capable of manipulating millions of silicon integrated circuits and III-V dies, with sizes ranging from microns to millimeters and thicknesses between tens of nanometers and several microns, with diverse types of substrates including 2-8 inch wafers and up to Gen 2.5 display-type glass, with yields >99.5%[3-5].

Cost estimates for a concentrator based embodiment of transfer printing for PVs

Detailed costing information for a concentrator based embodiment of transfer printing technique was generated as part of a successful, peer-reviewed proposal to the *Solar America Initiative* of the *Department of Energy*, in their *Energy Efficiency and Renewable Energy (EERE) Division*. A short excerpt and a table of on cost from this proposal appear below.

The proposed project contributes to the goals of SETP by developing a fabrication process and module that meets the low-end of the DOE's target Levelized Cost of Energy (LCOE) of $0.05/kWh for utility-scale photovoltaics. The key elements for reducing the module manufacturing cost to $0.30/Wp, enabling a $0.50/Wp module price and $1.50/Wp installed concentrator photovoltaic (CPV) system price, include (i) low cost growth and processing strategies that minimize the wafer and materials costs in GaAs, a high-efficiency cell being used by many groups for utility-scale CPV systems, (ii) micro transfer printing (μTP) methods to directly transfer and distribute μ-cells of GaAs (as small as 10 μm per side) over large-area (m^2) foreign substrates, (iv) direct ink writing (DIW) techniques to create electrical interconnects to the μ-cells, and (v) soft embossing procedures to form high quality μ-optic concentrators matched to the μ-cells. This approach has the ability to achieve costs of $0.30/Wp in high volume production, as shown below, where the projected manufacturing cost for the transfer printing process is $15/$m^2$ module. This latter

estimate is based on an annual cost-of-ownership for the printing system (including annual depreciation, operator and maintenance labor, electricity, facilities and consumables) is less than $600,000. The system can fully process a 1 m^2 module with 70 "prints" from a 150 mm wafer in less than 10 minutes, producing more than 40,000 1 m^2 modules per year and resulting in a printing cost per m^2 module of less than of less than $15.

Module size (1 m^2)	1,000,000	mm^2	*Assumptions shown in yellow*
Solar incidence	1,000	W/m^2	
Wafer size	150	mm	
Total wafer area	17,671	mm^2	
Inscribed hexagone area as % of total	83%		
Total transfer area	14,614	mm^2	
Number of transferred hexagones	70		
Solar cell area as % of usable area	95%		*For etch streets / holes, etc.*
Module efficiency	25%		
Module power output	238	W	
Cost per transferred area	$40		
Cell cost per module without concentration	$2,800		$0.28 per cm^2 cell cost
Concentration ratio	500		
Manufacturing Cost Per 1 m^2 module			
Cell cost	$6	8%	
Printing cost	$15	21%	
Micro-optical concentrator & encapsulation	$20	28%	
Interconnects	$10	14%	
Anti-reflective coating deposition	$10	14%	
Assembly cost + test and sort	$10	14%	
Total module assembly cost	$71	100%	
$ / W_p	**$0.30**		

High performance multijunction solar cells via transfer printing

Some recent, unpublished outcomes of measurements at the *National Renewable Energy Laboratory* on liftoff and printed 3J cells from *Semprius* indicate efficiencies in the 35-37% range at concentrations of ~600x.

Supplementary References

1 Oktyabrsky, S., Aboelfotoh, M. O., Narayan, J. & Woodall, J. M. Cu_3Ge ohmic contacts to n-type GaAs. *J. Electron. Mater.* **25**, 1662-1672 (1996).

2 Rey-Stolle, I., Galiana, B. & Algora, C. Assessment of a low-cost gold-free metallization for III-V high concentrator solar cells. *Sol. Energ. Mat. Sol. C.* **91**, 847-850 (2007).

3 Benkendorfer, K., Menard, E. & Carr, J. Printing cuts the cost of uniting III-Vs with silicon CMOS. *Compound Semiconductors*, 16-18 (June 2007).

4 Hamer, J. *et al.* AMOLED displays using transfer-printed integrated circuits. *SID Symposium Digest of Technical Papers* **40**, 947-950 (2009).

5 Bower, C., Menard, E., Bonafede, S. & Burroughs, S. in *Electronic Components and Technology Conference, ECTC 2009.*

Supplementary Figures and Legends

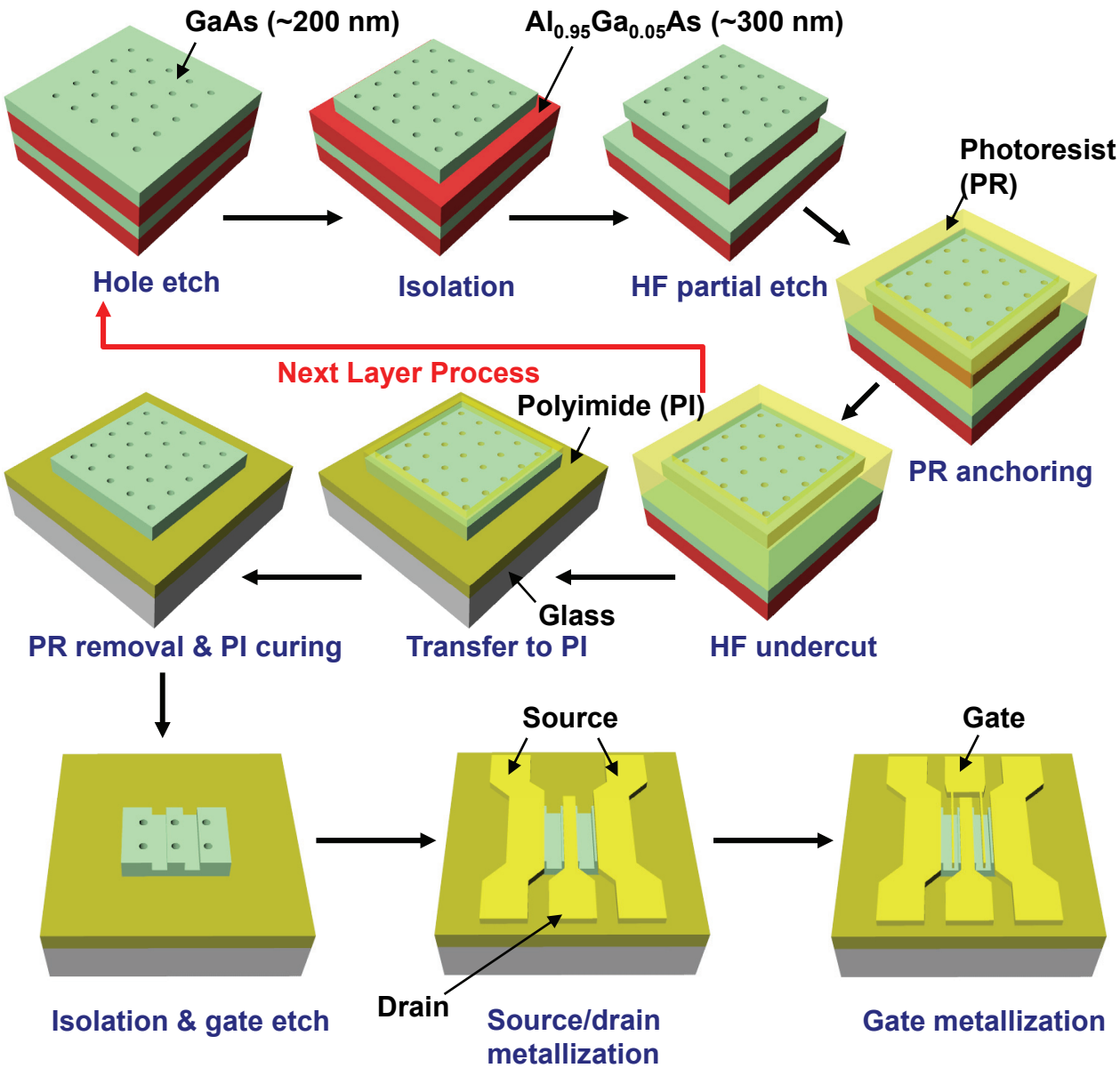


Figure S1: Schematic illustration of processing steps for transfer printing of GaAs/AlAs multilayers for MESFETs on a glass substrate.

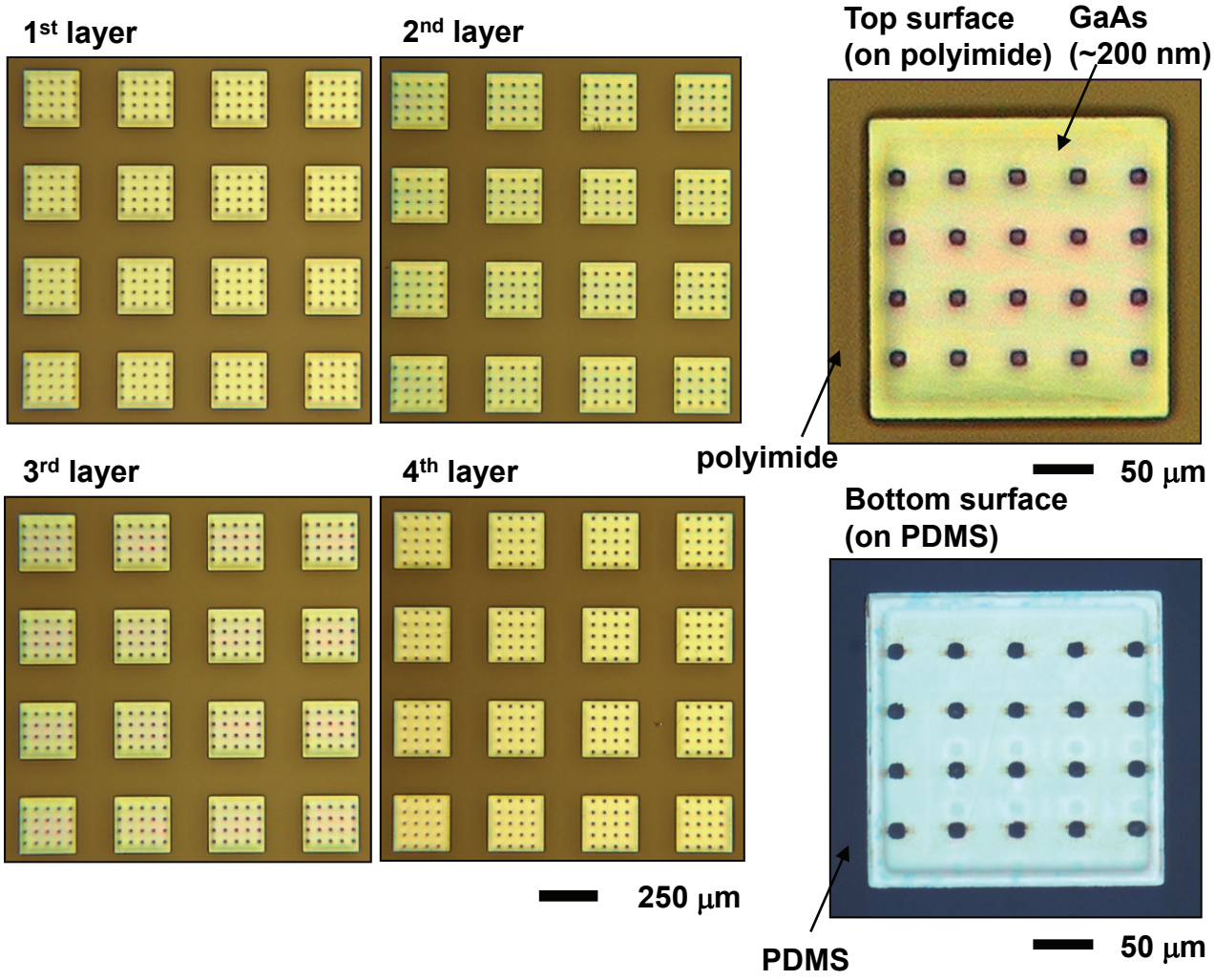


Figure S2: Optical micrographs of printed arrays of GaAs from 1st, 2nd, 3rd and 4th epilayers on a polyimide coated glass substrate. Inset shows magnified image of top (on polyimide) and bottom surfaces (on PDMS stamp) of a GaAs membrane.

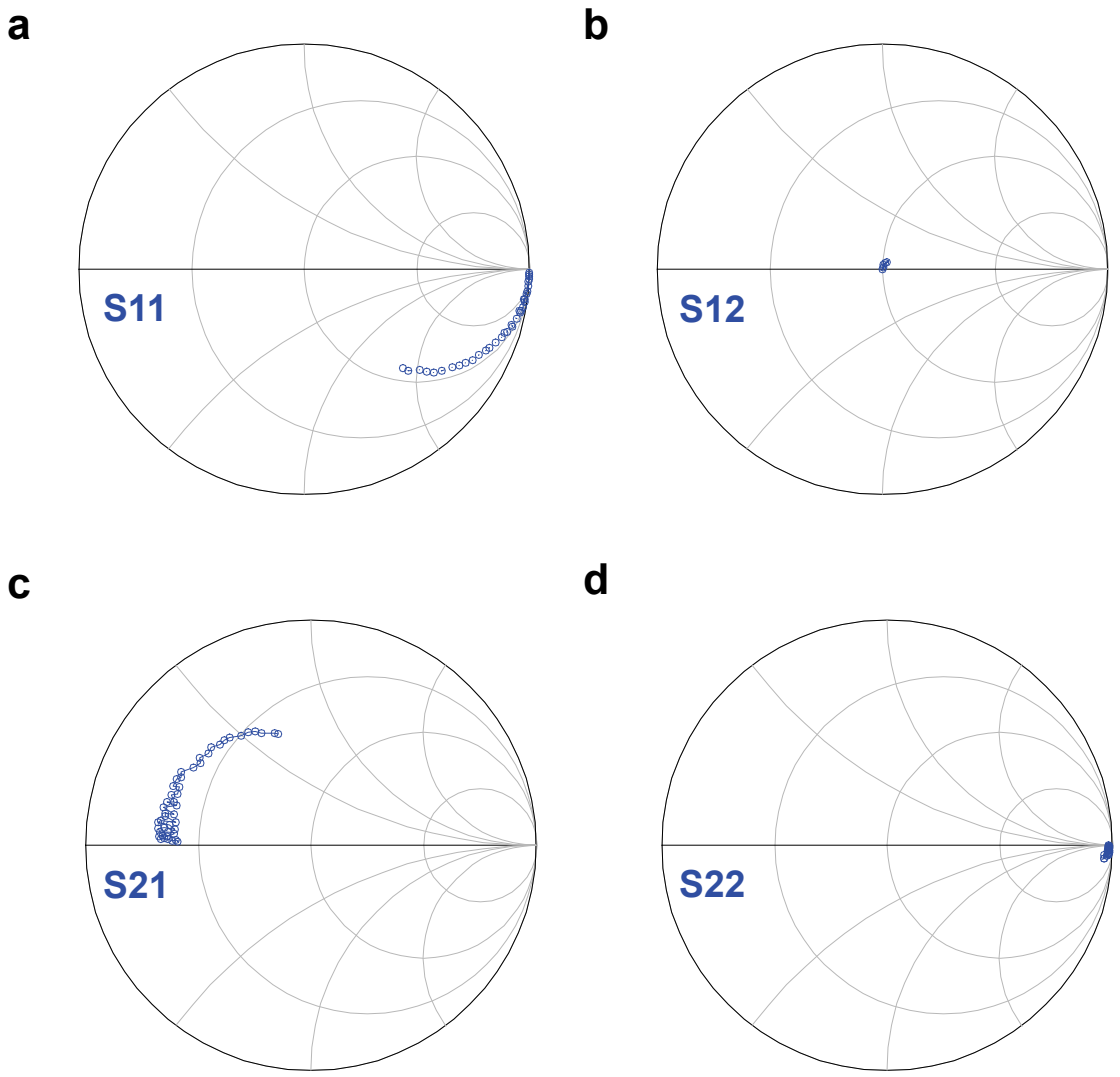


Figure S3: Smith chart of measured S-parameters over the frequency range between 30 MHz and 3 GHz: **a,** S11, **b,** S12, **c,** S21 and **d,** S22.

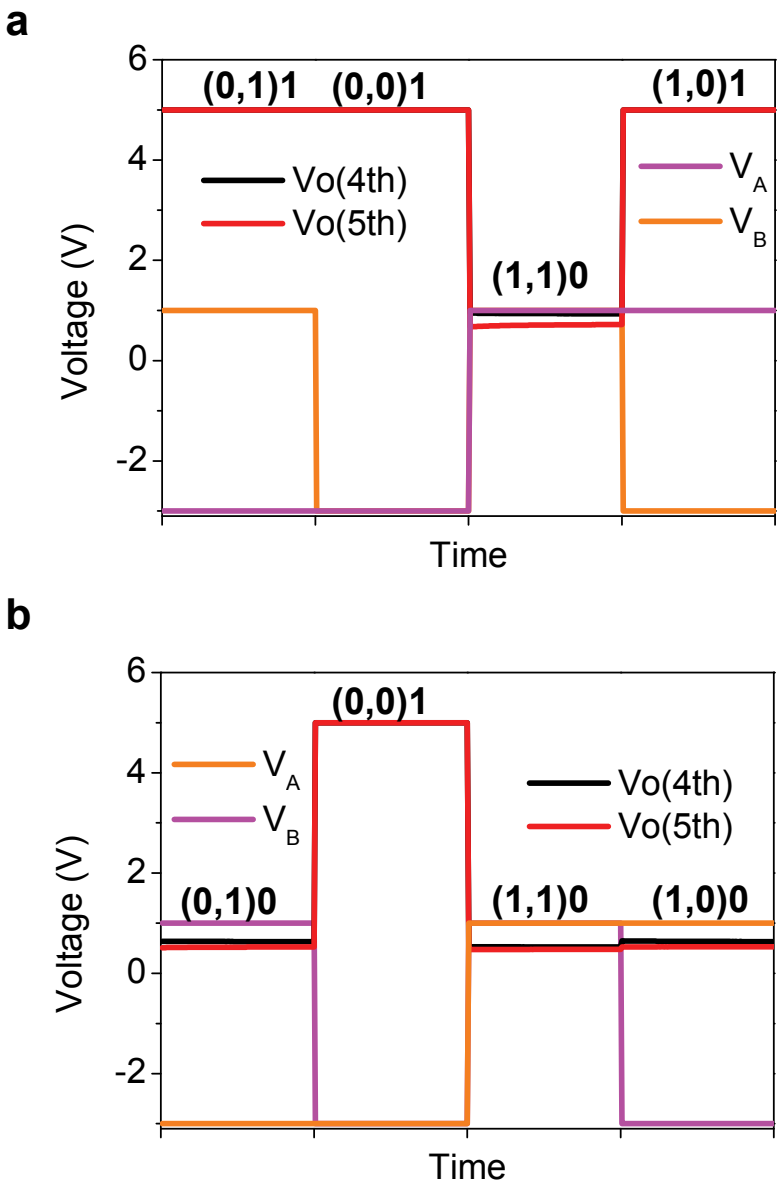


Figure S4: **a,** Output-input characteristics of NAND gate for 4th and 5th layer devices. **b,** Output-input characteristics of NOR gate for 4th and 5th layer devices.

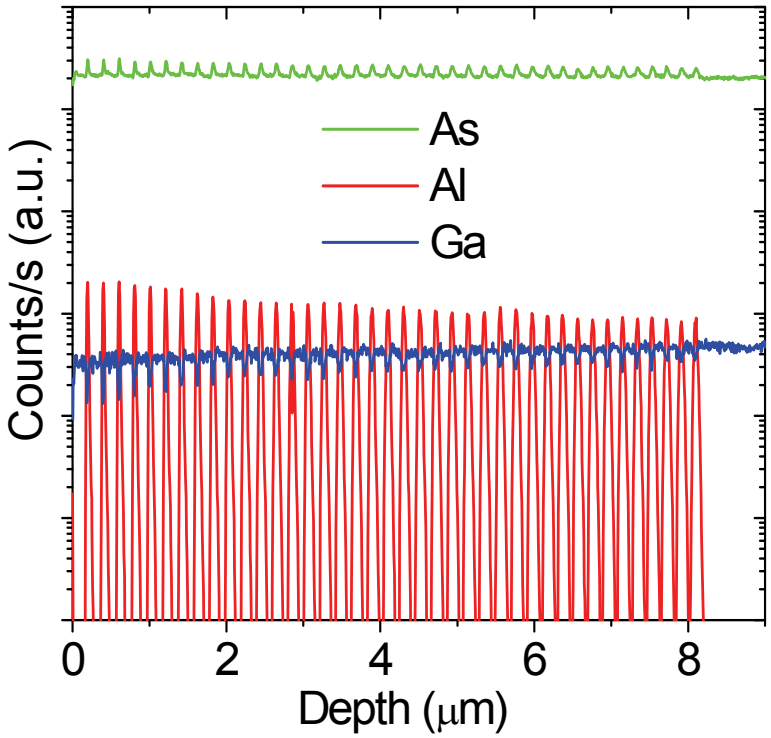


Figure S5: SIMS profile of a 40 repeat multilayer stack (Figure 1e) of GaAs (200 nm)/$Al_{0.95}Ga_{0.05}As$ (20 nm).

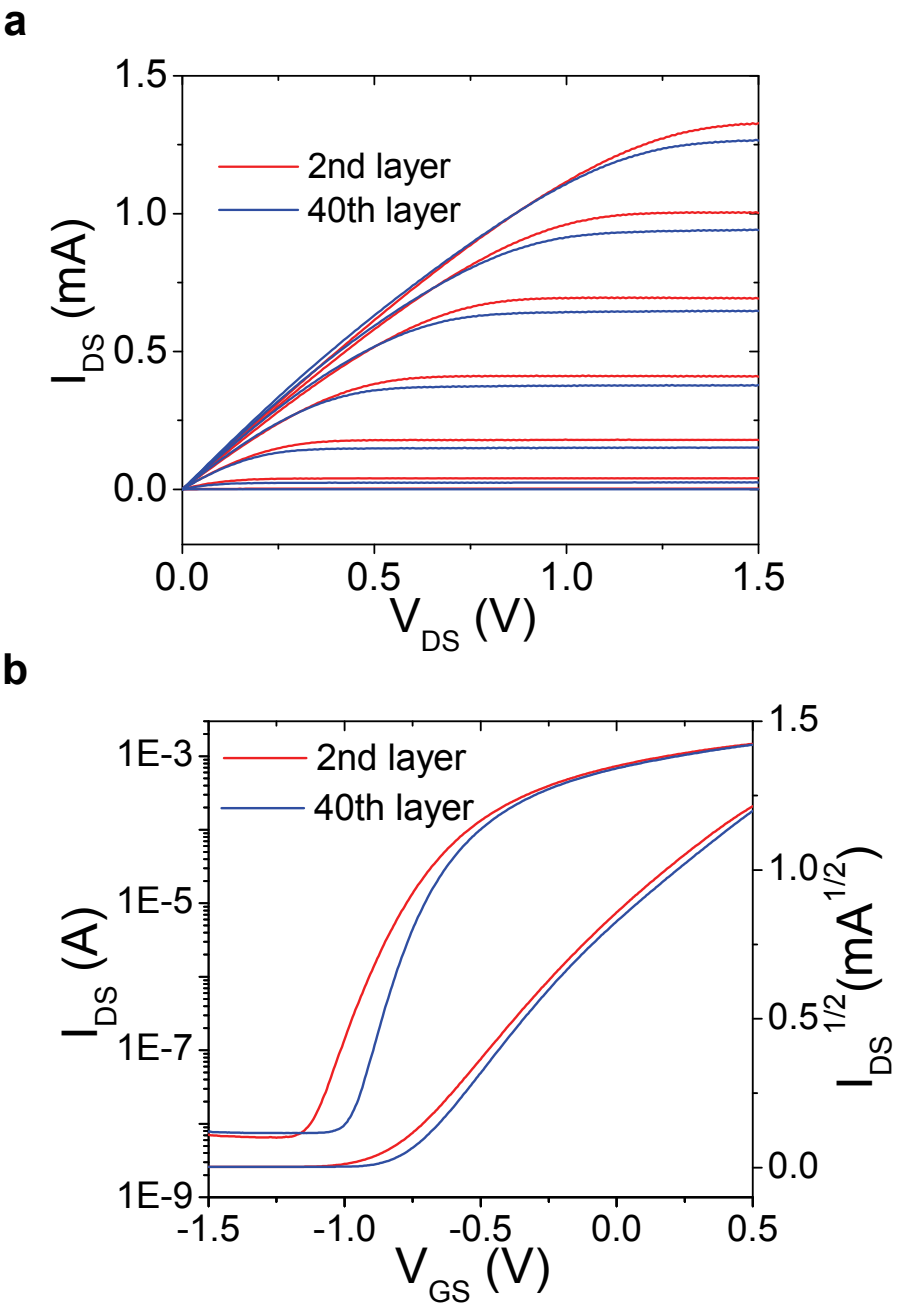
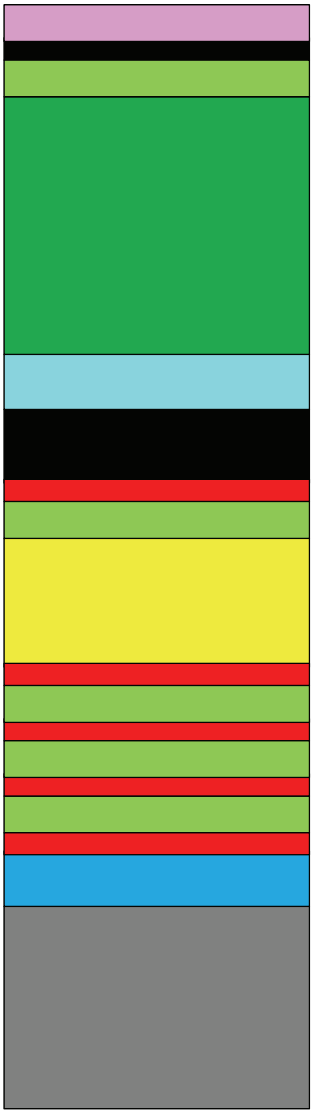


Figure S6: **a,** V_{DS} vs. I_{DS} curves of MESFETs fabricated from 2nd (red line) and 40th (blue line) layer of 40 repeat multilayer stack measured at V_{GS} = 0.8, 0.6, 0.4, 0.2, 0, -0.2, -0.4V, from top to bottom. **b,** Corresponding I_{DS} vs. V_{GS} transfer curves of MESFET for 2nd (red) and 40th (blue) layer devices at V_{DS} = 1.5 V.



18. p-type GaAs top contact layer 0.2 μm, Zn-doped, $4x10^{19}$ cm^{-3}

17. p-type $Al_{0.4}Ga_{0.6}As$ window layer 0.04 μm, Zn-doped, $2x10^{18}$ cm^{-3}

16. p-type GaAs emitter layer 0.1 μm, Zn-doped, $2x10^{18}$ cm^{-3}

15. n-type GaAs base layer 2.0 μm, Si-doped, $3x10^{17}$ cm^{-3}

14. n-type $Al_{0.4}Ga_{0.6}As$ BSF layer 0.1 μm, Si-doped, $3.5x10^{18}$ cm^{-3}

13. n-type GaAs contact layer 1.0 μm, Si-doped, $5x10^{18}$ cm^{-3}

12. $Al_{0.95}Ga_{0.05}As$ sacrificial release layer 0.02 μm

11. n-type GaAs 0.05 μm, Si-doped, $8x10^{16}$ cm^{-3}

10. undoped GaAs 0.5 μm

9. $Al_{0.95}Ga_{0.05}As$ sacrificial release layer 0.02 μm

8. n-type GaAs 0.2 μm, Si-doped, $4x10^{17}$ cm^{-3}

7. $Al_{0.95}Ga_{0.05}As$ sacrificial release layer 0.02 μm

6. n-type GaAs 0.2 μm, Si-doped, $4x10^{17}$ cm^{-3}

5. $Al_{0.95}Ga_{0.05}As$ sacrificial release layer 0.02 μm

4. n-type GaAs 0.2 μm, Si-doped, $4x10^{17}$ cm^{-3}

3. $Al_{0.95}Ga_{0.05}As$ sacrificial release layer 0.02 μm

2. GaAs buffer layer 0.2 μm

1. semi-insulating <100> GaAs substrate (2° off towards the nearest [111] plane)

Figure S7: Schematic illustration of a heterogeneous multilayer stack composed of three layers of MESFET, a NIR detector layer and a single junction (1J) solar cell layer. Each of device layers is separated by $Al_{0.95}Ga_{0.05}As$ (20 nm).

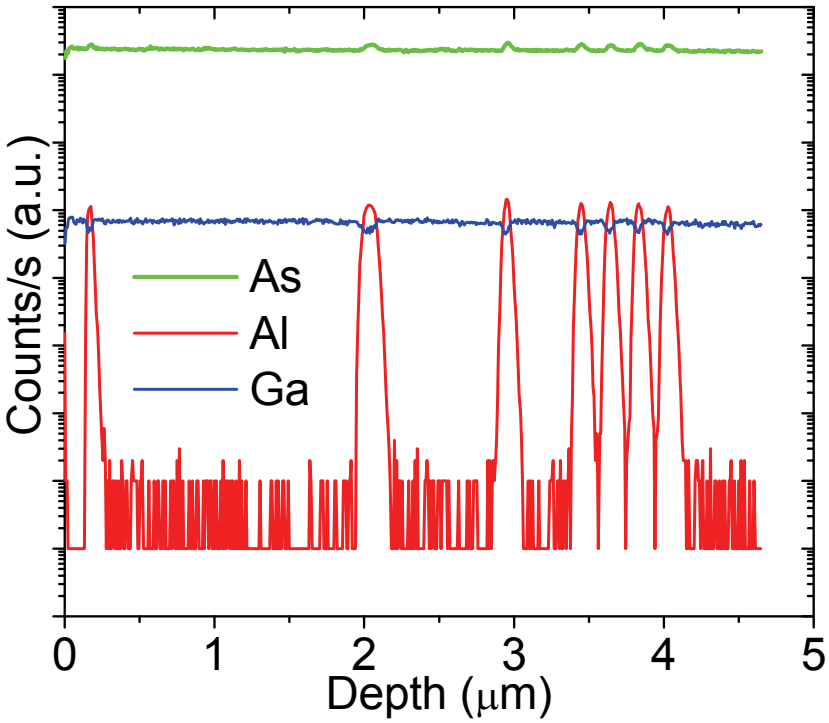


Figure S8: SIMS profile of a heterogeneous multilayer stack (Figure 1f and Figure S7).

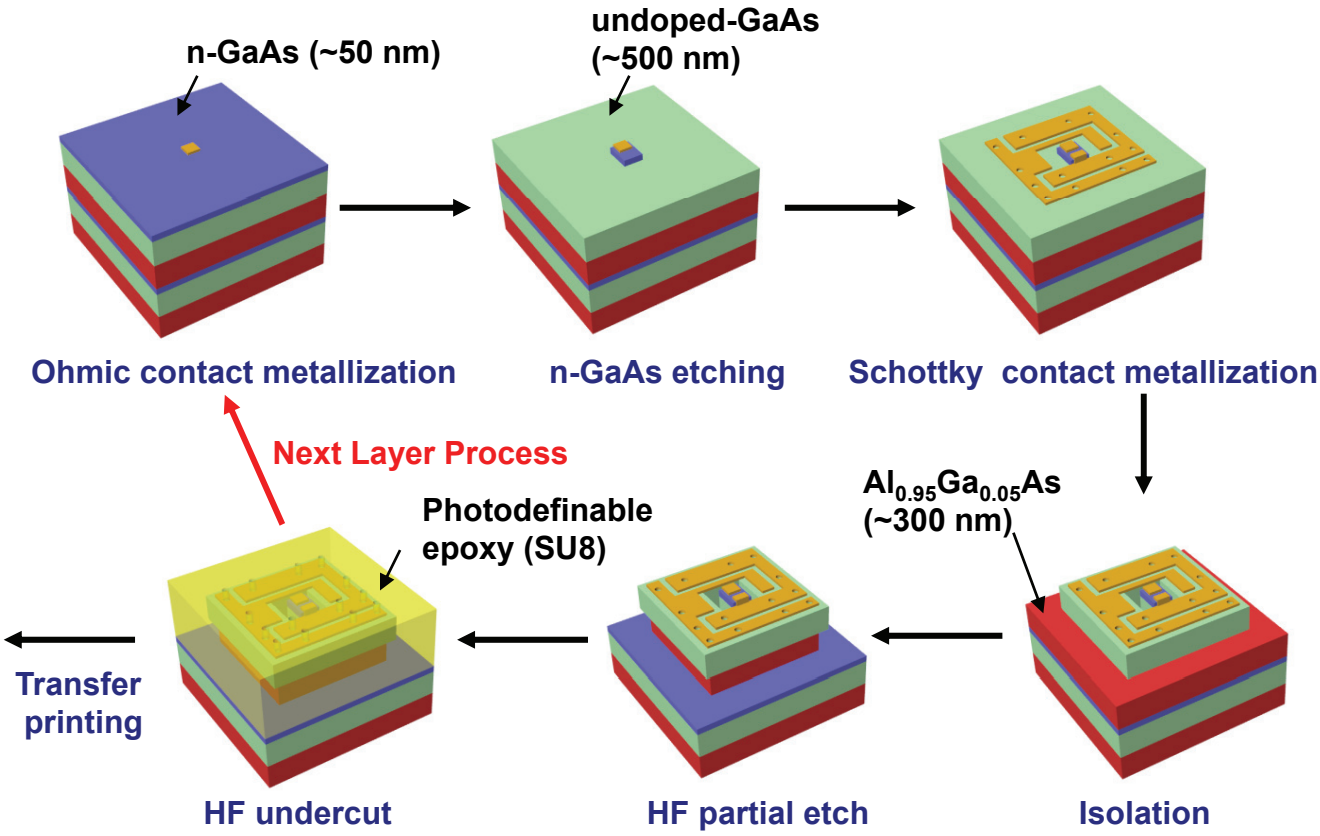
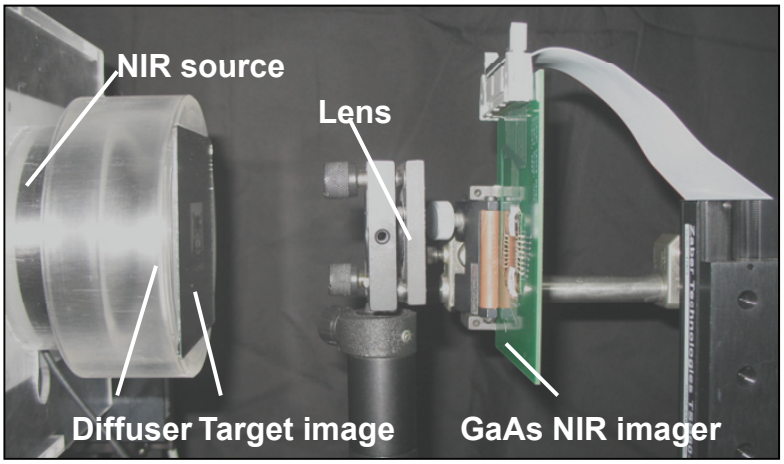


Figure S9: Schematic illustration of processing steps for delineation, metallization, undercut etching and transfer printing of multilayer GaAs MSM NIR imager.

a



b

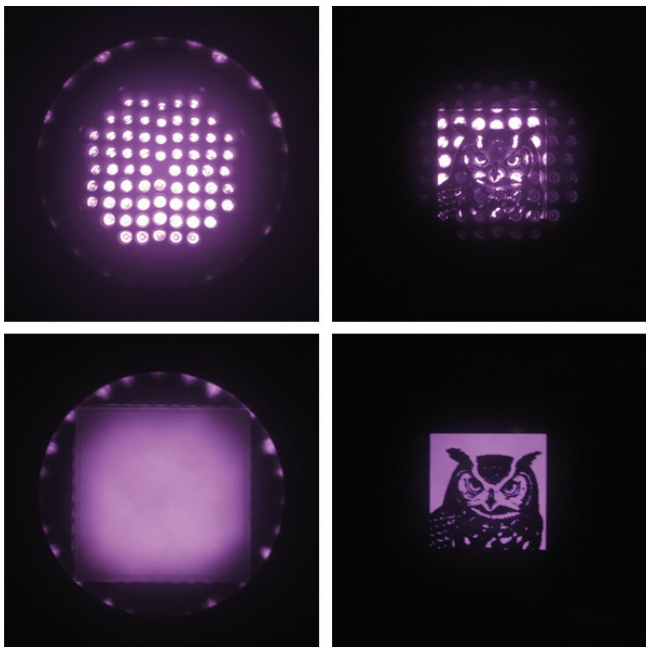
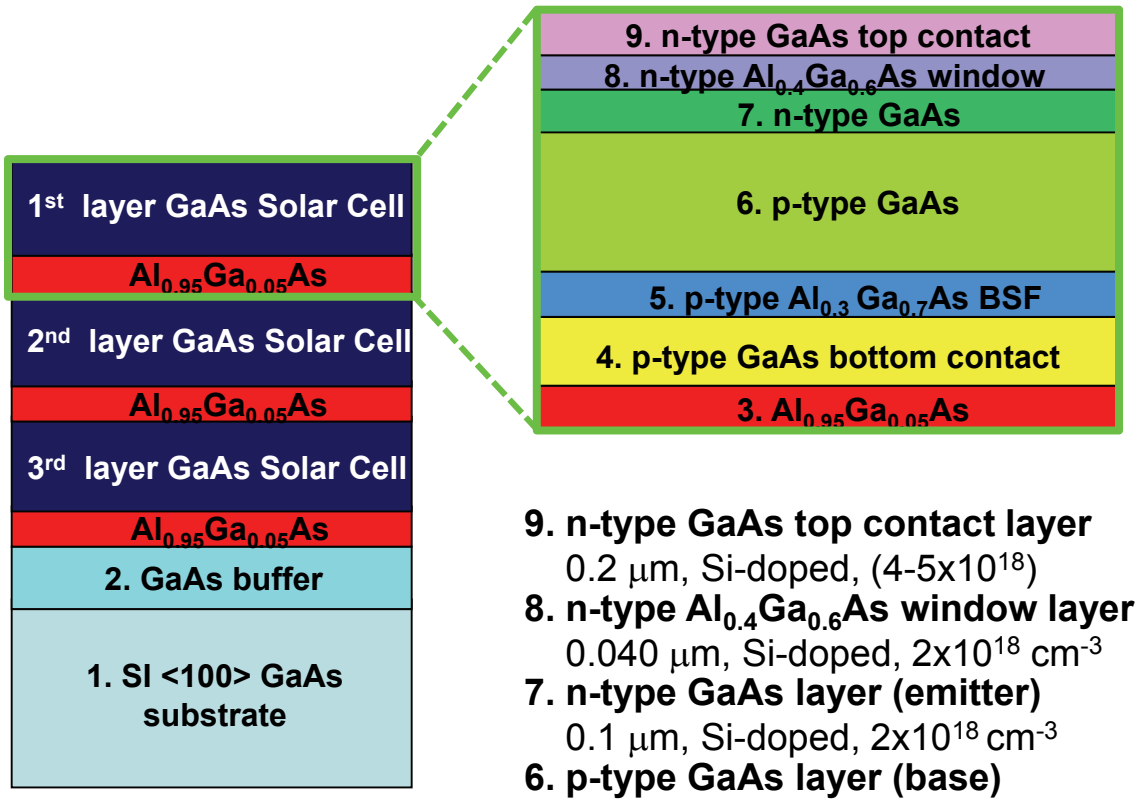


Figure S10: **a,** Photograph of the optical setup for image acquisition of GaAs MSM NIR imagers. **b,** Photographs of a NIR source and a target image at different illumination conditions: infrared LEDs only (upper left), target image in front of infrared LEDs (upper right), diffuser in front of infrared LEDs (lower left), target image in front of diffuser with infrared LEDs at the backside (lower right).



9. n-type GaAs top contact layer
0.2 μm, Si-doped, (4-5x10^{18})
8. n-type $Al_{0.4}Ga_{0.6}As$ window layer
0.040 μm, Si-doped, 2x10^{18} cm^{-3}
7. n-type GaAs layer (emitter)
0.1 μm, Si-doped, 2x10^{18} cm^{-3}
6. p-type GaAs layer (base)
2 μm, Zn-doped, 3x10^{17} cm^{-3}
5. p-type $Al_{0.3}Ga_{0.7}As$ BSF layer
0.1 μm, Zn-doped, 1x10^{19} cm^{-3}
4. p-type GaAs bottom contact layer
2.0 μm, Zn-doped, 4x10^{19} cm^{-3}
3. $Al_{0.95}Ga_{0.05}As$ sacrificial release layer
1.0 μm
2. GaAs buffer layer
0.5 μm
1. Semi-insulating <100> GaAs substrate
2° off towards the nearest [111] plane

Figure S11: Schematic illustration of triple stack n-on-p type GaAs 1J solar cells and details of stack design.

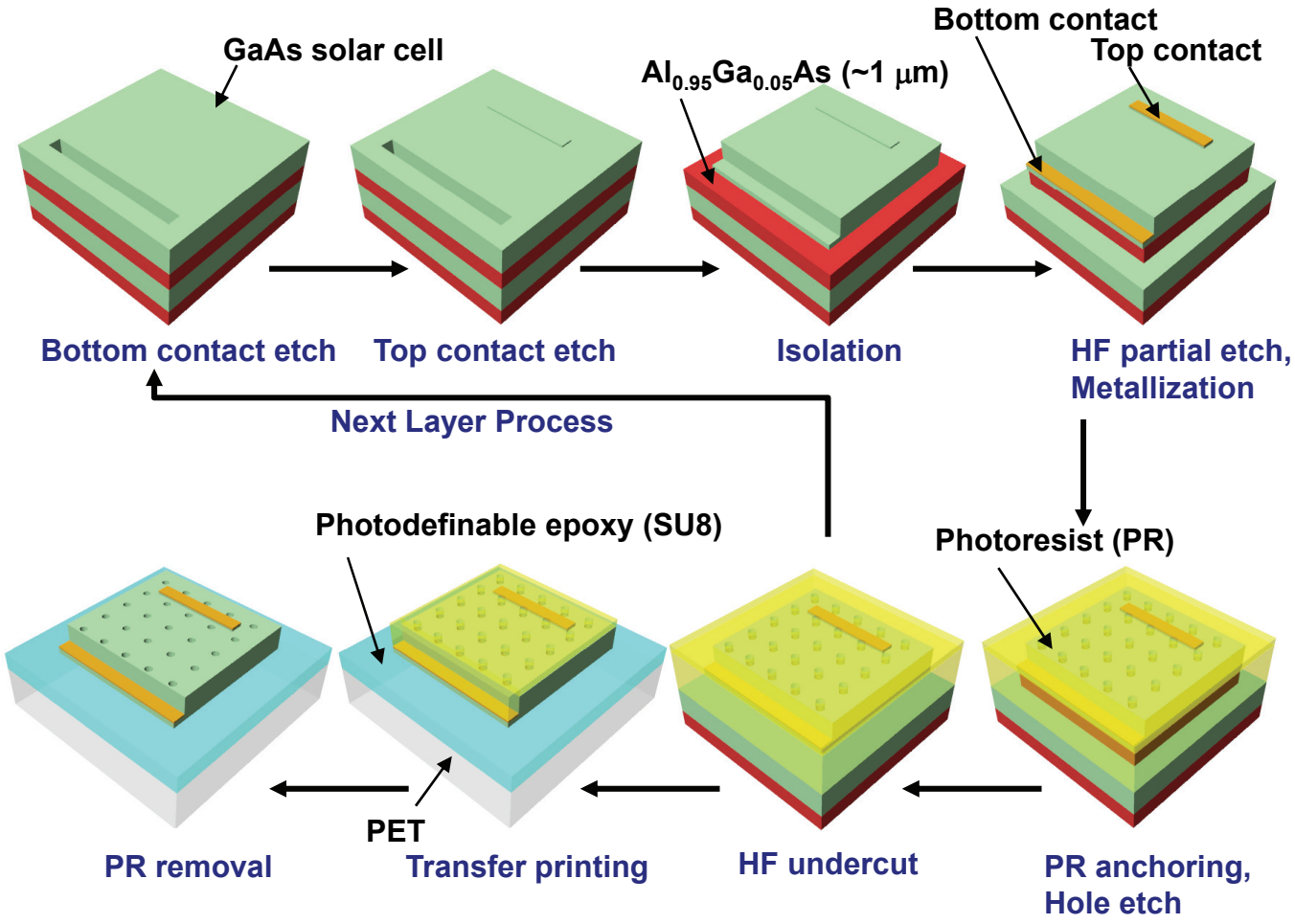


Figure S12: Schematic illustration of processing steps for delineation, metallization, undercut etching and transfer printing of multilayer GaAs 1J solar cells.

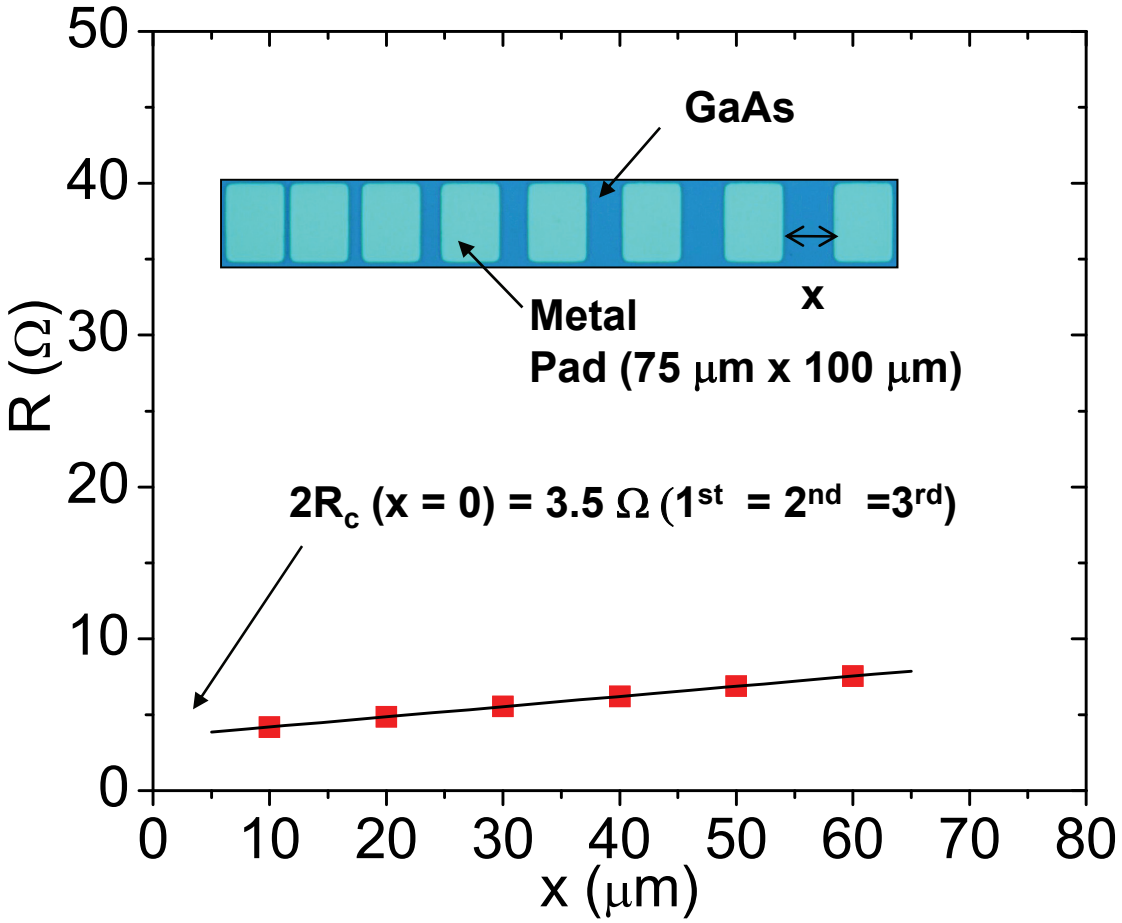


Figure S13: Plot of total resistance (R) vs. metal pad spacing (x) from transmission line model (TLM) experiment for p-type GaAs contact at 1st (top), 2nd (middle) and 3rd (bottom) layers (x = 10, 20, 30, 40, 50, 60 μm). Contact resistance (R_c) was obtained from one half of the y-intercept in the linear fit of data. Metal pads (75 μm by 100 μm) of Pt/Ti/Pt/Au (10/40/10/80 nm) were formed on a GaAs contact layer by electron-beam evaporation followed by lift-off process. The total area of GaAs contact layer where metal pads were formed is about 880 x 100 μm^2, and sheet resistances separately obtained from four point probe measurements at each layer are 16.8 Ω/□ (top), 16.7 Ω/□ (middle), 17.8 Ω/□ (bottom), respectively. TLM experiments were conducted without additional annealing. Inset shows optical image of patterned TLM metal pads on a p-type GaAs contact layer.

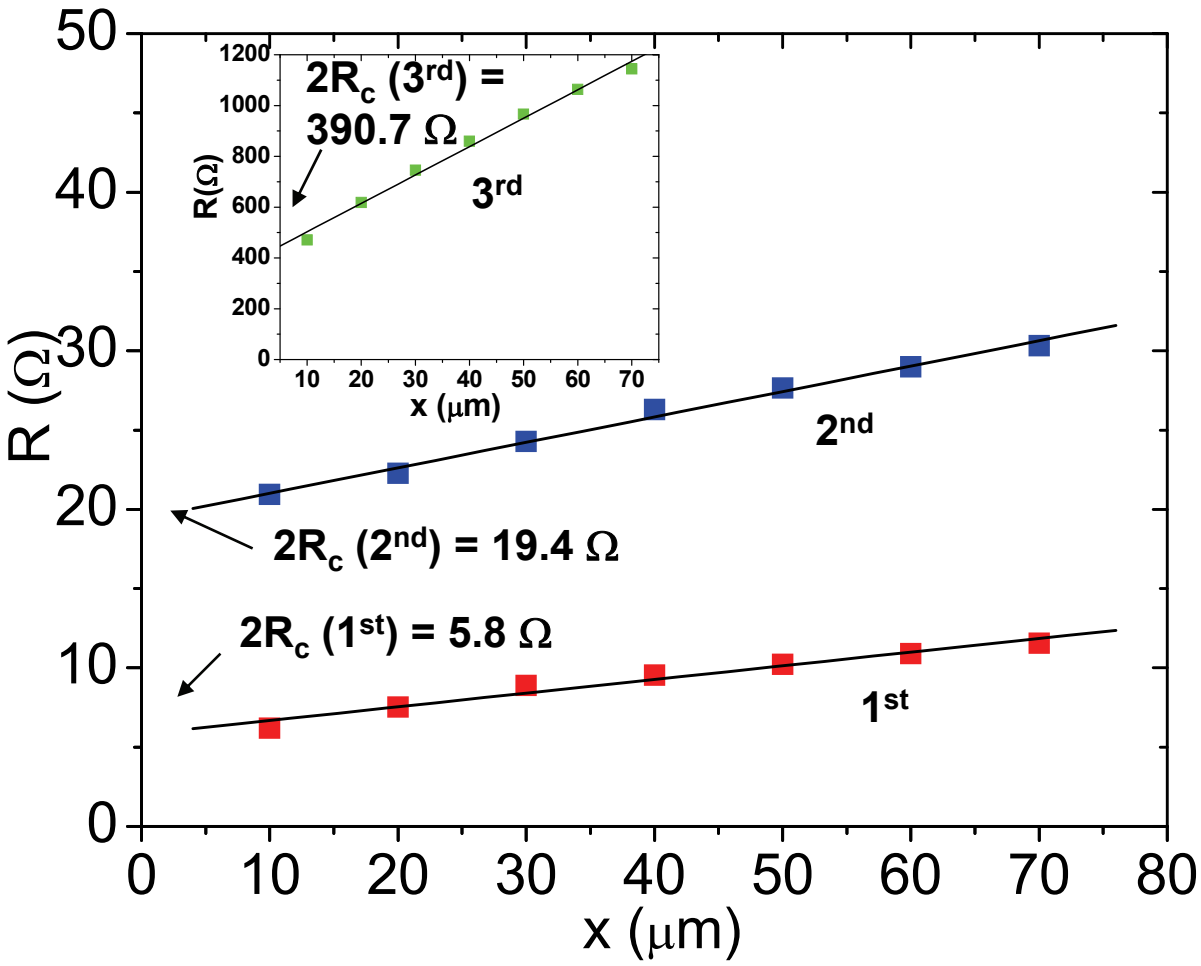


Figure S14: Plot of total resistance (*R*) vs. metal pad spacing (*x*) from TLM experiment for n-type GaAs contact at 1st (top), 2nd (middle) layers (*x* = 10, 20, 30, 40, 50, 60, 70 μm). Metal pads (75 μm by 100 μm) of Pd/Ge/Au (5/35/80 nm) were formed by electron-beam evaporation followed by lift-off process. The total area of GaAs contact layer where metal pads were formed is about 880 x 100 μm^2, and sheet resistances separately obtained from four point probe measurements at each layer are 24.1 Ω/□ (top), 51.4 Ω/□ (middle), 107.0 Ω/□ (bottom), respectively. TLM experiments were conducted after annealing at 175 °C for 1 h under N_2 atmosphere. Inset shows *Rx*-plot from the 3rd (bottom) layer.

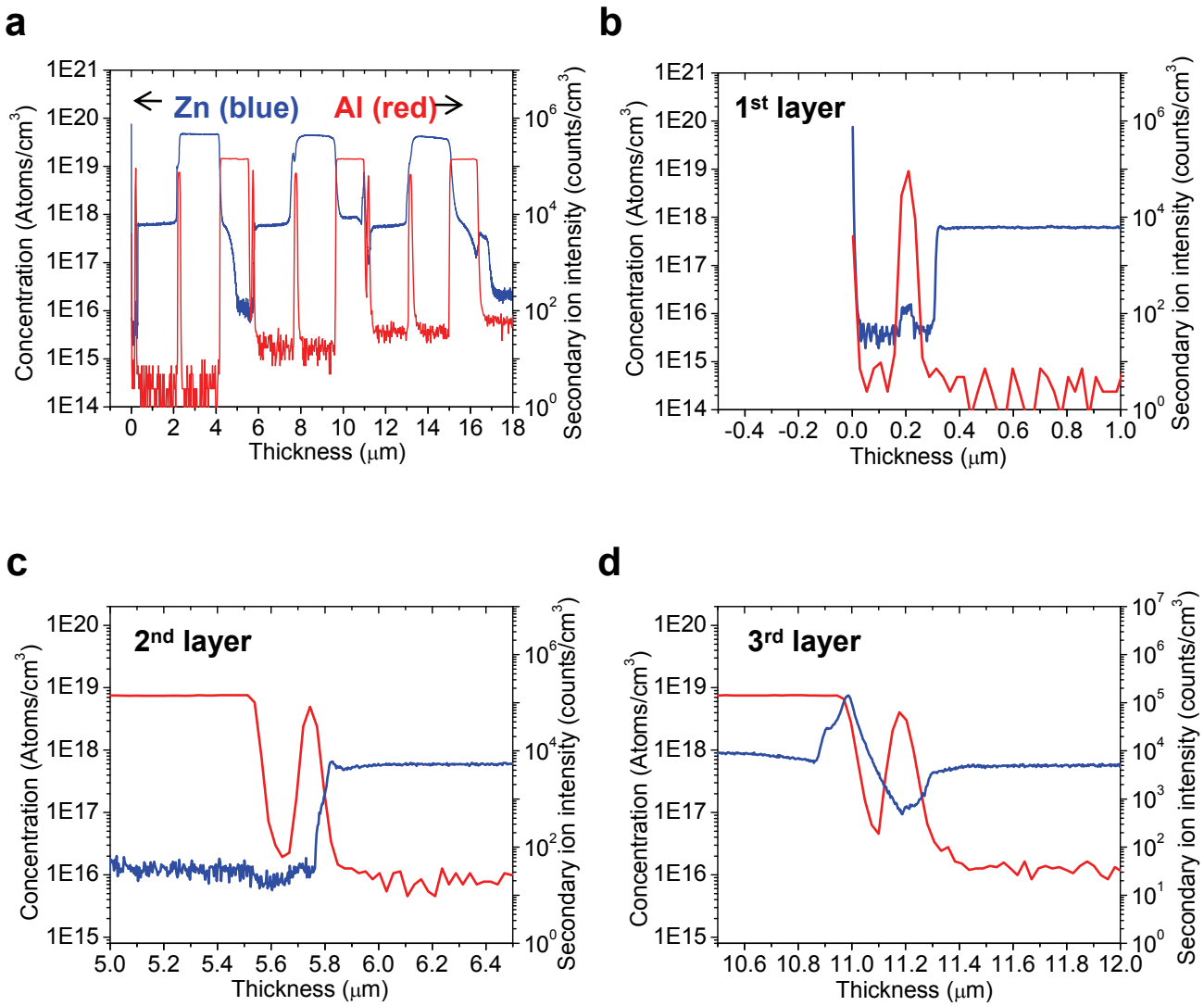


Figure S15: Secondary ion mass spectrometry (SIMS) plot for Zn (blue data) and Al (red data) with triple layer GaAs solar cells with stack design shown in Figure S11; **a,** for the entire sample thickness, and near the junction of **b,** 1st (top), **c,** 2nd (middle) and **d,** 3rd (bottom) layer devices.

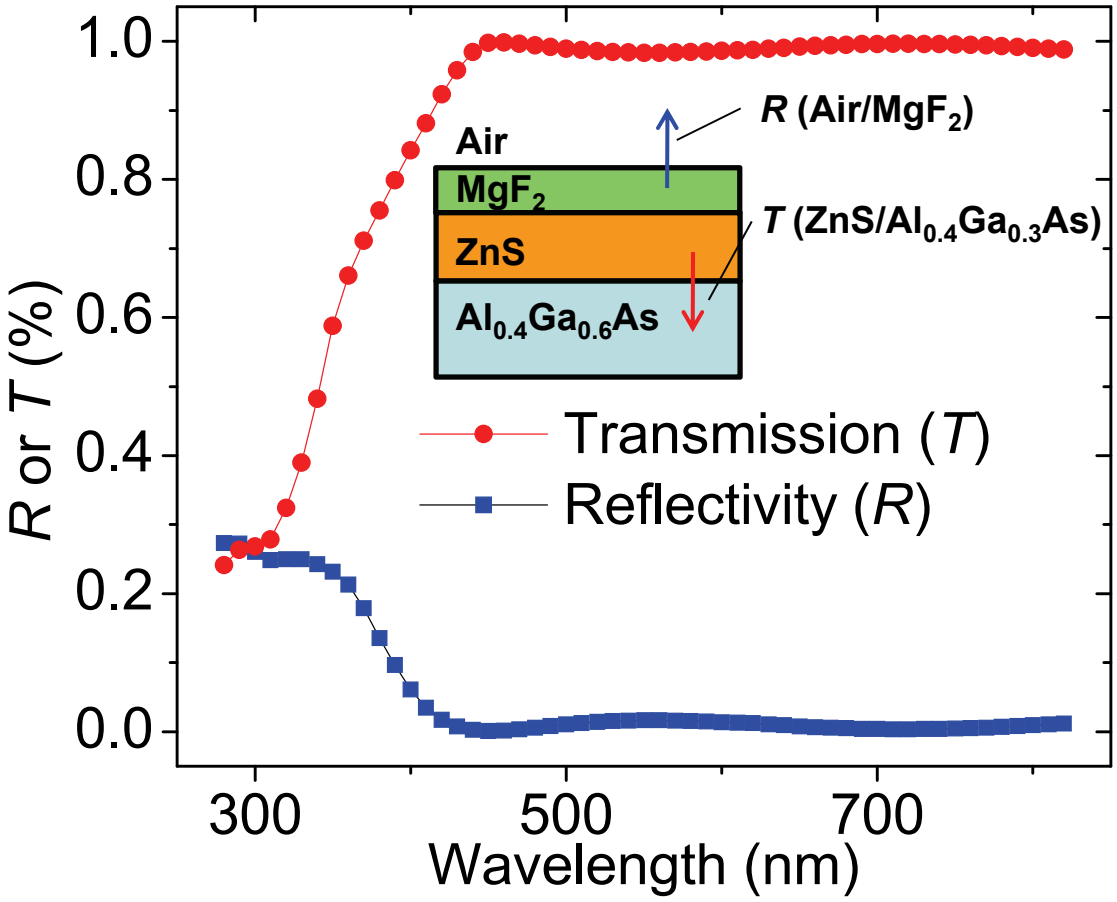


Figure S16: Calculated normal incidence transmission (*T*) and reflectivity (*R*) spectra of double layer antireflection coating of MgF_2 (thickness: 105 nm) and ZnS (thickness: 55 nm) on a substrate of $Al_{0.4}Ga_{0.6}As$ (semi-infinite). The calculated reflectivity is at the interface between air and MgF_2, while the transmission at the interface between ZnS and $Al_{0.4}Ga_{0.6}As$. Inset shows a schematic of simulated structures.

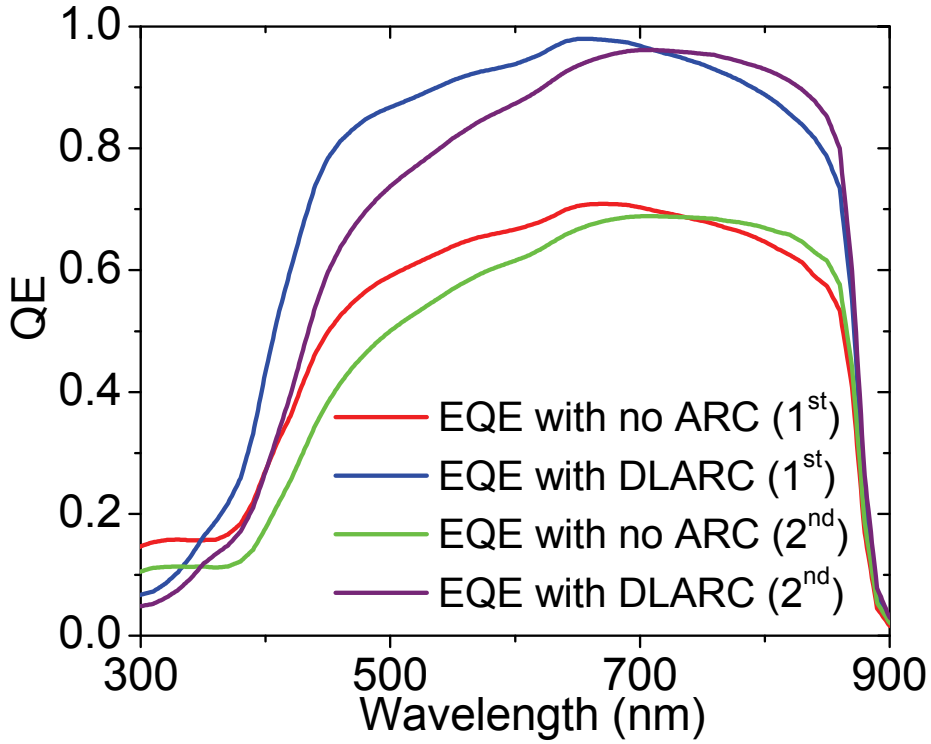


Figure S17: Plot of external quantum efficiencies (EQE) of 1st and 2nd layer devices; Red and green data points show experimentally measured EQE with no ARC for the 1st and 2nd layer devices, respectively. Blue and violet data points are calculated EQE with a double layer ARC (DLARC) of ZnS/MgF_2 described in Figure S16 for the 1st and 2nd layer devices, respectively.

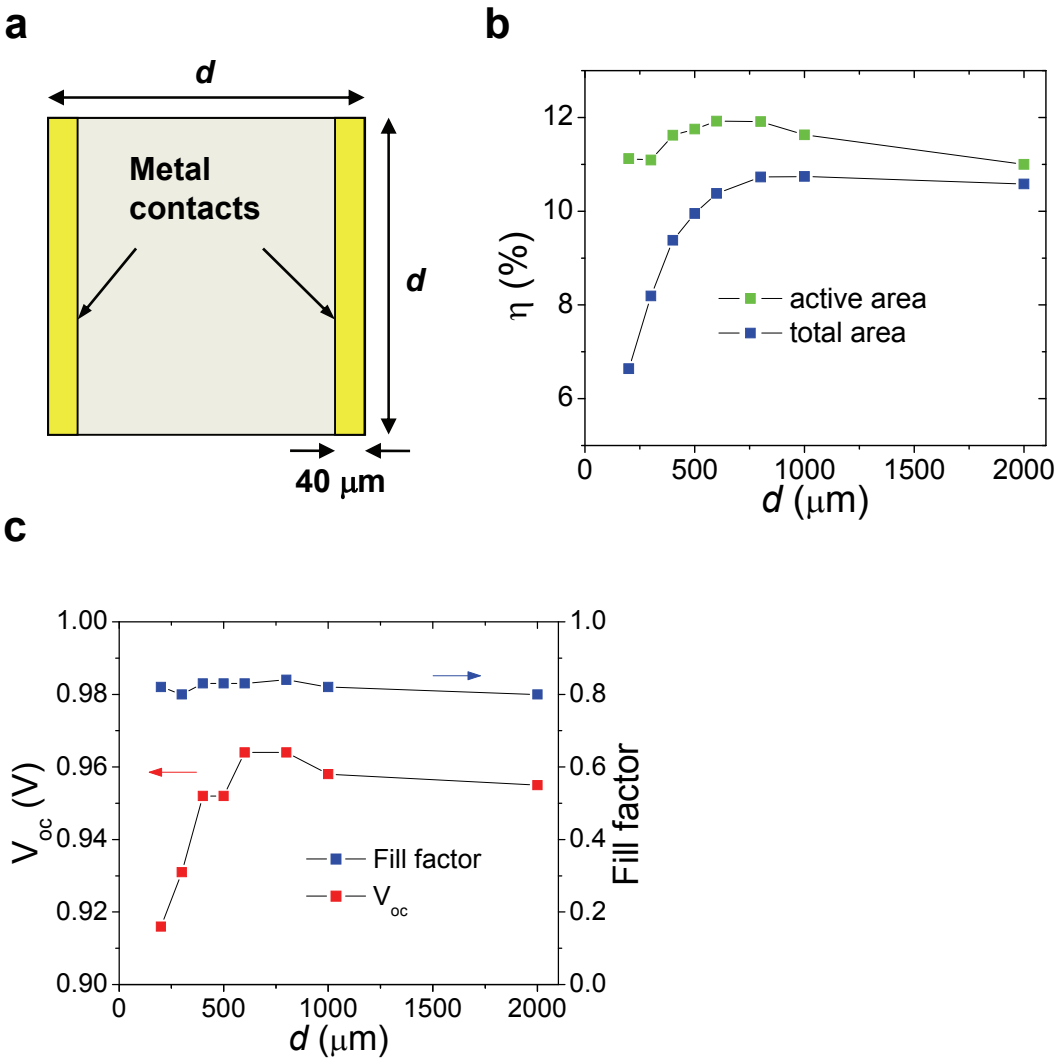
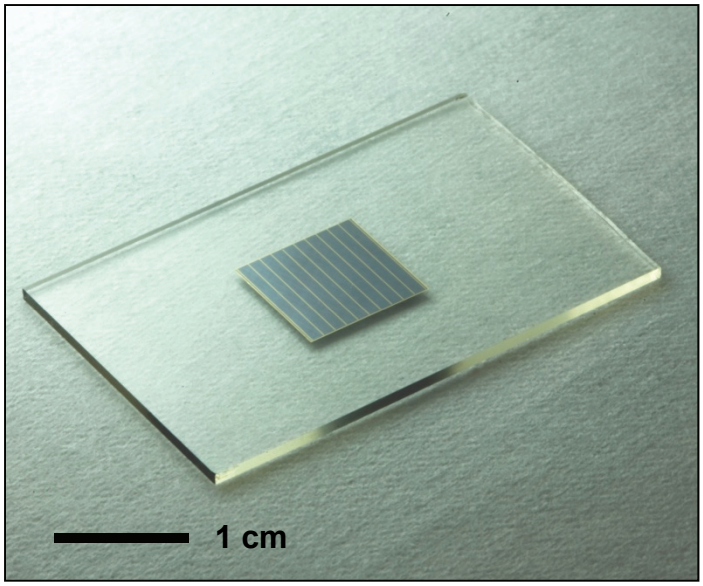


Figure S18: **a,** Schematic of the cell geometry for the scaling study of cell sizes. **b,** Active area and total area efficiencies as a function of cell size (*d*) measured under AM1.5D illumination. **c,** Fill factor and open circuit voltage (V_{oc}) as a function of cell size (*d*).

a



b

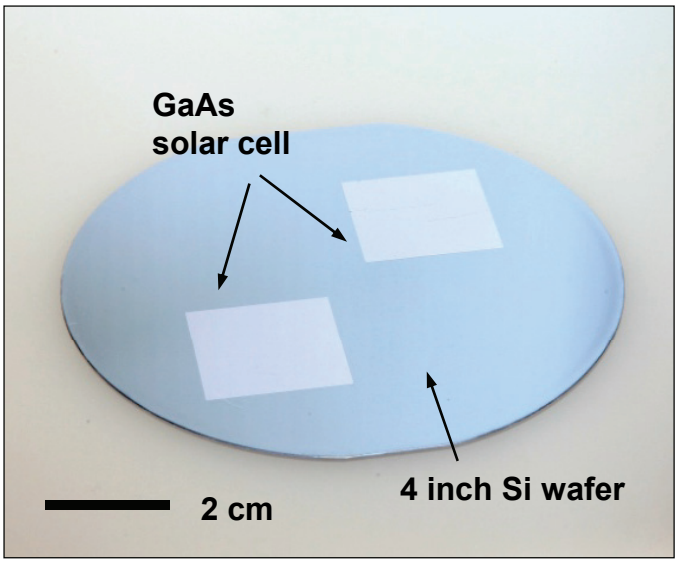


Figure S19: **a,** Image of a printed GaAs solar cell with a size ~10 x 10 mm^2 on a glass substrate, with simple, metal grid contacts. **b,** Image of two GaAs solar cells with sizes of ~25.4 x 25.4 mm^2 printed on a Si substrate.

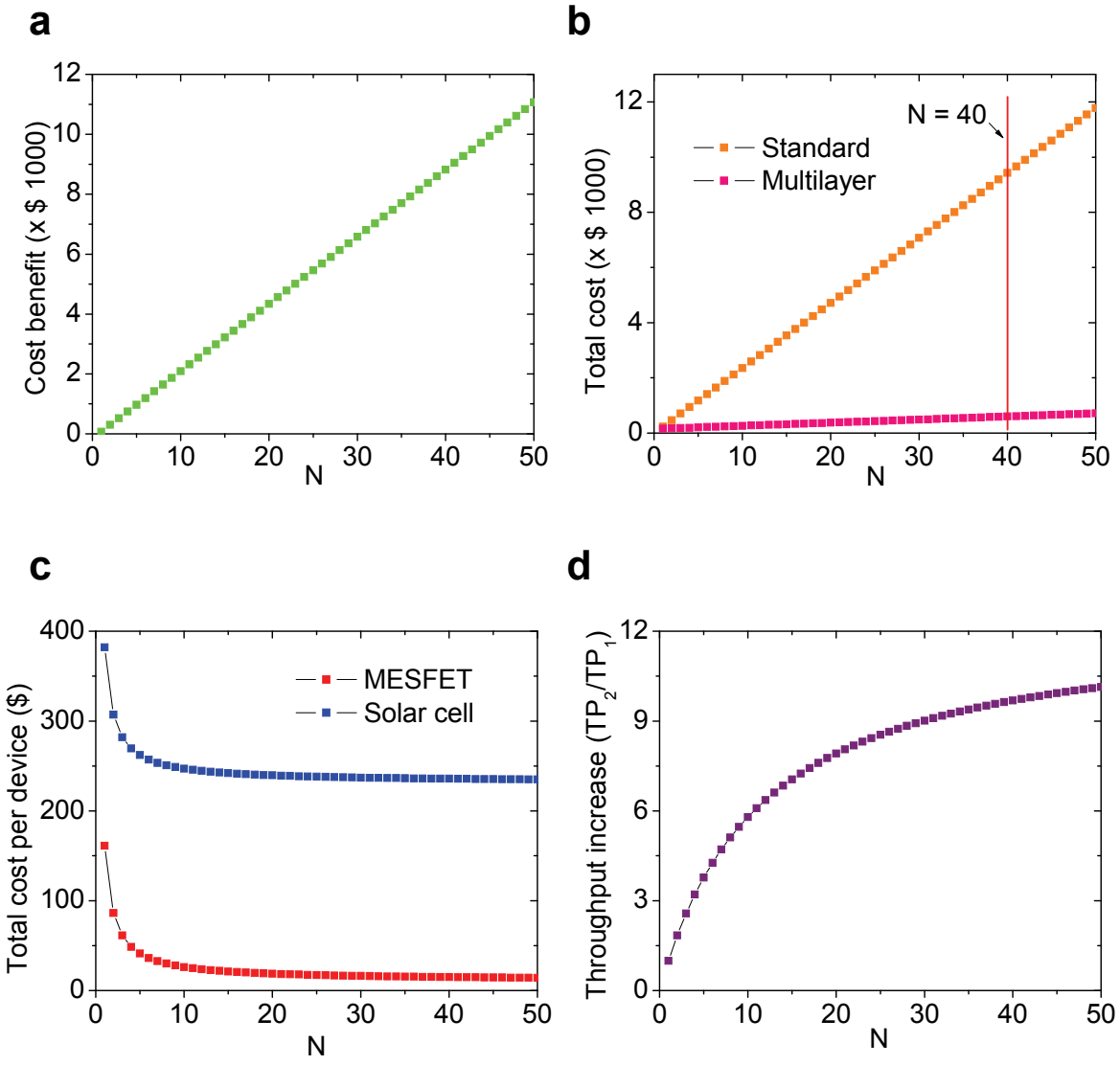


Figure S20: **a,** Total cost benefit ($C_{T1} - C_{T2}$) between standard and multilayer approaches as a function of number of device layers grown (N). **b,** Total cost for the growth of MESFETs in standard and multilayer approaches as a function of N. **c,** Total cost per device in the multilayer approach as a function of N for the cases of MESFETs and solar cells. **d,** Ratio of the throughput for the multilayer to the standard approach (TP_2/TP_1) as a function of N for the case of MESFETs.

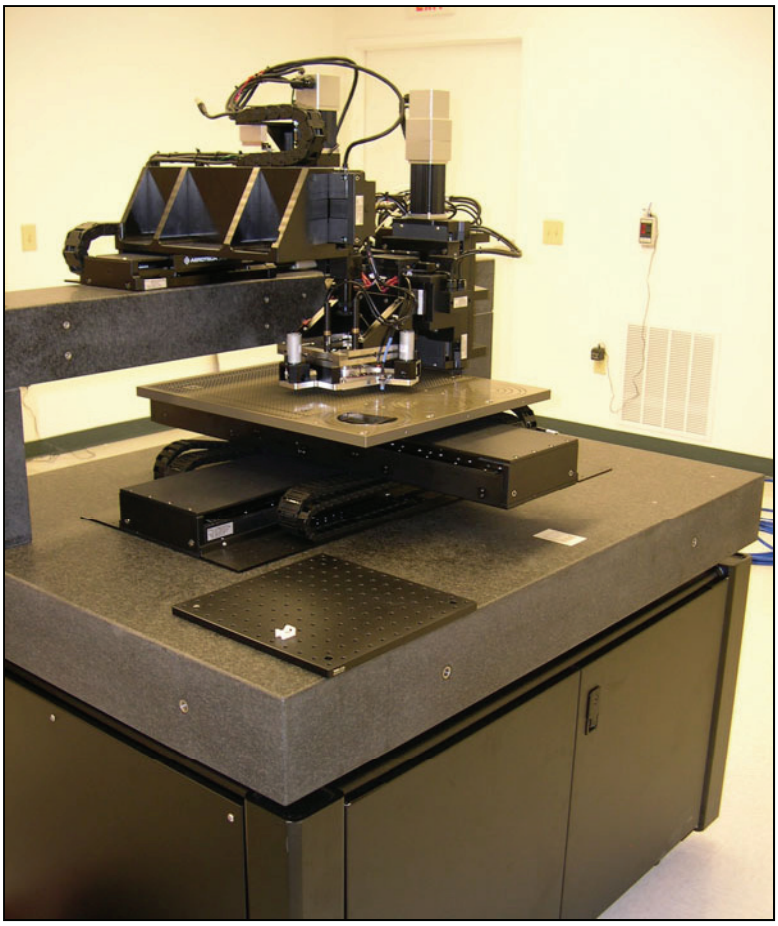


Figure S21: Image of the latest generation of transfer printer designed for populating Gen 2.5 display-type glass substrate.

Supplementary Tables

Pick-up yield (averaged over a full 6 inch SOI source wafer)	99.995%
Printing yield	99.7%
Placement accuracy (x,y) (standard deviation)	0.33 μm
Placement accuracy (θ) (standard deviation)	0.05 degree

Table S1: Technical specifications of the latest generation of transfer printer (Fig. S21) designed for populating Gen 2.5 display-type glass substrate.

	Thickness of GaAs (μm)	Growth time for GaAs (min)	Thickness of AlGaAs (μm)	Growth time for AlGaAs (min)	B (min)	B′ (min)
MESFET	0.2	4.9	0.02	0.3	**4.9**	**0.3**
Solar cell	4.3	104.4	0.16	2.5	**106.6**	**0.3**

Table S2: Total growth time of epilayers per device for MESFETs and solar cells.