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Printed Assemblies of Inorganic Light-Emitting Diodes for Deformable and Semitransparent Displays

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We have developed methods for creating microscale inorganic light-emitting diodes (LEDs) and for assembling and interconnecting them into unusual display and lighting systems. The LEDs use specialized epitaxial semiconductor layers that allow delineation and release of large collections of ultrathin devices. Diverse shapes are possible, with dimensions from micrometers to millimeters, in either flat or "wavy" configurations. Printing-based assembly methods can deposit these devices on substrates of glass, plastic, or rubber, in arbitrary spatial layouts and over areas that can be much larger than those of the growth wafer. The thin geometries of these LEDs enable them to be interconnected by conventional planar processing techniques. Displays, lighting elements, and related systems formed in this manner can offer interesting mechanical and optical properties.

Display devices represent ubiquitous, central components of nearly all consumer electronics technologies. Organic light-emitting diodes (OLEDs) are rapidly emerging as an attractive alternative to backlit liquid crystals due to their comparatively high refresh rates, contrast ratios, power efficiencies, and capacity for vibrant color rendering (*1*, *2*). Inorganic light-emitting diodes (ILEDs) can also form displays, with properties such as brightness, lifetime, and efficiency that can exceed those possible with OLEDs (*3*, *4*). These displays exist, however, only in ultralarge-area, low-resolution formats (square meters; billboard displays), limited by processing and assembly procedures that do not scale effectively to small (< ~200 μm by 200 μm), thin (< ~200 μm) light emitters or to dense, high–pixel count arrays. An ability to replace existing

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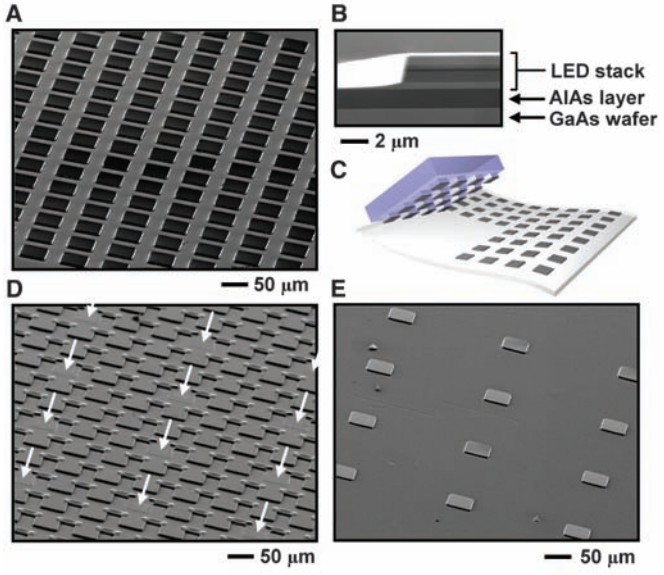

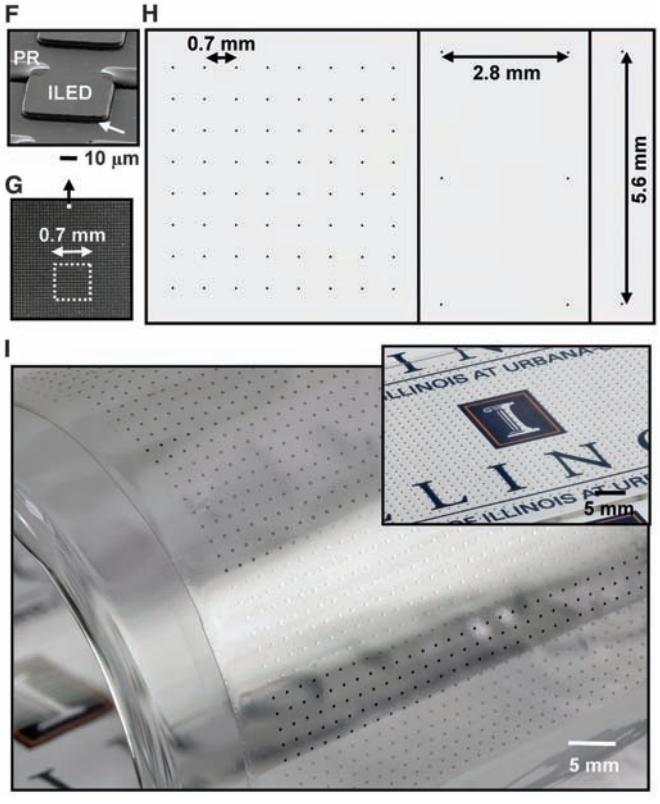

Fig. 1. (**A**) SEM image of a square array of AlInGaP LED structures (50 μm by 50 μm) created by vertical, patterned etching through an epitaxial multilayer stack grown on a GaAs wafer. (**B**) Cross-sectional SEM view of one of these structures, showing the LED semiconductor layers (quantum wells, as well as cladding, spreading, and contact layers) on a sacrificial epilayer of AlAs. (**C**) Schematic illustration of a printing-based assembly method for transferring collections of LEDs (gray) released from the GaAs wafer to a target substrate (shown here as a flexible sheet). (**D**) SEM image of the GaAs wafer after removing a set of LEDs (indicated by white arrows) with a stamp. (**E**) SEM image of a region of the target substrate printed with this stamp. (**F**) Angled-view SEM image of an individual LED (i.e., ILED) from the array in (D). A pair of "breakaway" photoresist (PR) anchors at the two far corners of the device holds it above the GaAs wafer in the suspended configuration of a diving board, for ease of liftoff with a stamp. The white arrow points to the region of removed AlAs. (**G**) SEM image of a dense collection of such devices on a piece of a GaAs wafer. The black arrow and white dot indicate, roughly, the region of this chip that corresponds to the image of (F). (**H**) Optical image of a target substrate printed with sparse arrays of devices at different spacings, derived from the chip shown in (G). (**I**) Large-scale collection of ILEDs (1600 devices, in a square array with pitch of 1.4 mm) printed onto a thin, flexible sheet of plastic, shown here wrapped onto a cylindrical glass substrate (main panel). The inset shows a similar collection of ILEDs (1600 devices, in a square array with pitch of 1.4 mm) printed onto a plate of glass. For these cases, relatively large ILEDs were selected for ease of viewing; devices with dimensions of (E) are invisible at this magnification.

methods for fabricating ILEDs (i.e., wafer sawing, serial pick-and-place, wire bonding, and packaging on a device-by-device basis) and for incorporating them into displays (i.e., robotic assembly into tiles followed by interconnection using large quantities of bulk wiring) with those that more closely resemble the planar, batch processing of OLEDs would greatly expand the application opportunities. Examples include not only ILED displays for desktop monitors, home theater systems, and instrumentation gauging, but also, when implemented in flexible or stretchable forms, wearable health monitors or diagnostics and biomedical imaging devices. In microscale sizes, such ILEDs can also yield semitransparent displays, with the potential for bidirectional emission characteristics, for vehicle navigation, heads-up displays, and related uses.

We present routes to create ultrathin, ultrasmall ILEDs in flat or "wavy" geometries and to assemble them into addressable arrays using scalable processing techniques, on substrates ranging from glass to plastic and rubber. The strategy involves four key components: (i) epitaxial semiconductor multilayers designed for lateral delineation and release from a source wafer to yield isolated arrays of ILEDs, each of which remains tethered to the wafer by polymeric "breakaway" anchor structures; (ii) printing techniques for manipulating the resulting ILEDs in schemes that enable formation of large-scale arrays on foreign substrates and in arbitrary spatial layouts; (iii) planar processing methods for establishing electrical interconnects to the devices, in direct or matrix addressable configurations; and (iv) integration strategies capable of yielding ILED displays in flexible or stretchable formats and with conventional, semitransparent, or bidirectional emission characteristics. Certain aspects build on previously reported procedures for etching and manipulating epitaxial semiconductor layers (*5*–*11*) and for fabricating flexible and stretchable electronics (*12*, *13*).

Figure 1 presents essential aspects of the first two of the components [see supporting online material (SOM) for details]. The epitaxial semiconductor layers include AlInGaP quantum well structures (6-nm-thick $In_{0.56}Ga_{0.44}P$ wells, with 6-nm-thick barriers of $Al_{0.25}Ga_{0.25}In_{0.5}P$ on top and bottom), cladding films (200-nm-thick layers of $In_{0.5}Al_{0.5}P$:Zn and $In_{0.5}Al_{0.5}P$:Si for the p and n sides, respectively), spreaders (800-nm-thick layers of $Al_{0.45}Ga_{0.55}As$:C and $Al_{0.45}Ga_{0.55}As$:Si for the p and n sides, respectively), and contacts (5-nm-thick layer of GaAs:C and 500-nm-thick layer of GaAs:Si for the p and n sides, respectively), for a total thickness of ~2.523 μm, all grown on AlAs (1500-nm-thick layer of $Al_{0.96}Ga_{0.04}As$:Si) on a GaAs substrate (fig. S1). The AlAs can be removed by etching with hydrofluoric (HF) acid, in procedures that do not alter the overlying layers or the underlying substrate. The process for defining the ILEDs first involves forming a pattern of vertical trenches through the epitaxial layers by inductively coupled plasma reactive ion etching through a mask of SiO_2 defined photolithographically (fig. S2). This step determines the lateral geometries of the devices (fig. S2). Figure 1, A and B, shows top and cross-sectional scanning electron microscope (SEM) images collected after this etching process for a representative case, where the device islands in Fig. 1 are 50 μm by 50 μm. Creating a pattern of photoresist posts (i.e., "breakaway" anchors) located at two of the four corners of each island, followed by immersion in concentrated HF, leads to the undercut release of an organized array of ILEDs. The anchors hold the devices in their lithographically defined locations to prevent lift-off into the etching bath, even after complete undercut (fig. S2). Next, an automated printing tool (fig. S3) brings a soft elastomeric stamp with features of relief embossed onto its surface into aligned contact with a selected set of these ILEDs. Peeling the stamp away fractures the photoresist anchors and leaves the devices adhered via Van der Waals interactions to the raised regions of relief. Figure 1, C and D, shows schematic illustrations of the printing process and an SEM image of an array of anchored ILEDs on the source wafer after one cycle of printing (fig. S4). The white arrows in Fig. 1D highlight the collection of ILEDs removed by this process, corresponding to every third device along the two orthogonal axes of the square array. Figure 1E provides an SEM image of these devices printed onto a glass substrate. The engineering design of the breakaway anchors is such that they are sufficiently robust to hold the ILEDs in their

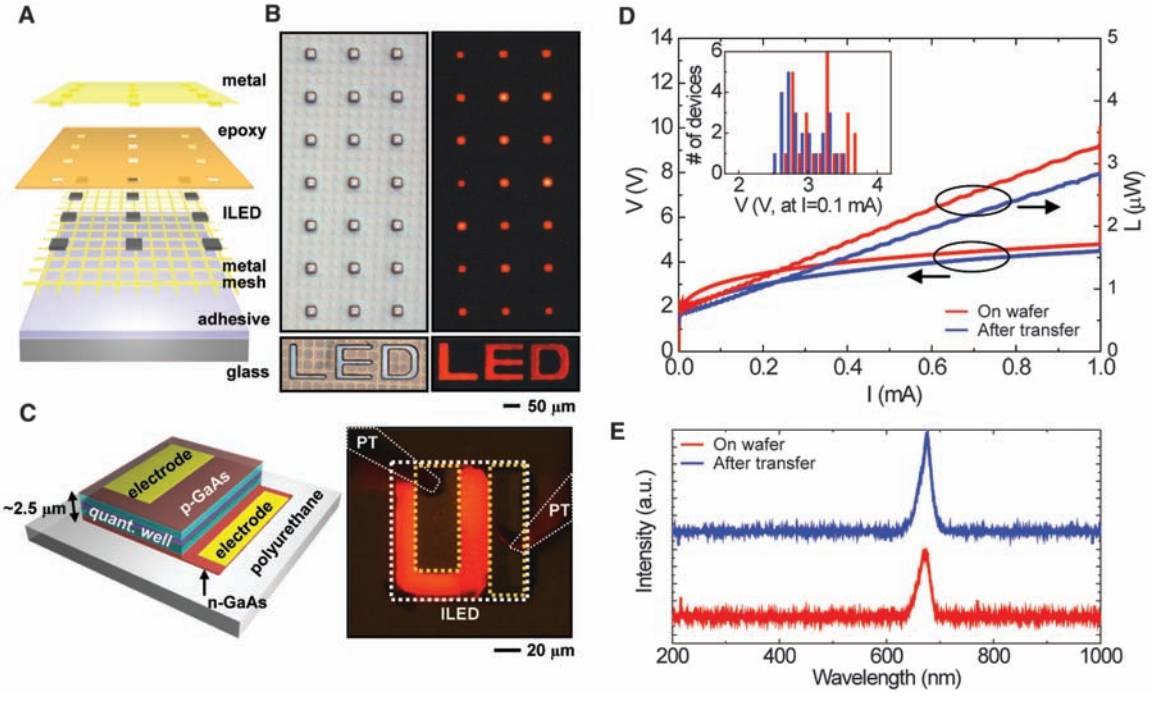

Fig. 2. (**A**) Exploded view schematic illustration of an array of ILEDs contacted by a metal mesh (bottom; n contacts) and a metal film (top; p contacts). A thin adhesive layer of PDMS facilitates printing onto the glass substrate. A photopatterned layer of epoxy on top of the devices prevents shorting of the top film to the bottom mesh. (**B**) Optical micrographs of an array of ILEDs (top: 25 μm by 25 μm, square geometries; bottom: characters "LED") in their off state with frontside illumination (left) and in their on state without illumination (right). (**C**) Schematic illustration of an ILED with integrated ohmic contacts (left) and optical image of an operating device (right), showing uniform emission characteristics at all regions not directly blocked by the contacts or probe tips. The areas delineated by yellow and white dashed boxes correspond to the contact electrodes and the device periphery, respectively. The regions labeled "PT" correspond to the probe tips used to evaluate the device operation. (**D**) Current-voltage-emission characteristics of a representative device before undercut etching on the GaAs wafer, and after transfer printing onto a polyurethane-coated glass slide. The inset provides a histogram of the bias voltages needed to produce currents of 0.1 mA in a collection of devices. (**E**) Spectral characteristics of emission for a typical device on the wafer and after transfer printing.

lithographically defined locations during the undercut etching and drying processes but sufficiently fragile to enable high-yield liftoff during printing. Three key design aspects are the use of (i) a pair of anchors on the same side of each ILED, to yield, after undercut, suspended, "diving board" layouts (Fig. 1F) that enable transfer of torques large enough to fracture the photoresist upon peel-back of the stamp; (ii) stamps with relief structures that are slightly smaller than the ILEDs and are offset from the centers of the devices to maximize these torques and also to minimize overlap with the anchors; and (iii) photoresist structures that fracture more readily than the semiconductor material. This type of anchoring scheme (i.e., heterogeneous anchoring) is much more efficient in active materials utilization and versatile in design choices than corresponding methods demonstrated previously for transistors (*12*) and solar cells (*14*), where peripheral parts of the devices themselves serve as the anchors (i.e., homogeneous anchoring). Conventional wafer dicing and pick-and-place methods are not suitable for devices with the thicknesses and dimensions in the range reported here, due to challenges associated with wafer utilization, device fragility, and size. Such techniques also lack the high-throughput, parallel operation of the type of printing methods described above.

Figure 1G shows a micrograph of a densely packed array of anchored, undercut ILEDs on a source wafer. Figure 1H shows sparse assemblies of these devices formed by printing in a step-and-repeat fashion from this wafer to a glass substrate, coated with a thin (~10 μm) layer of poly(dimethylsiloxane) (PDMS) to promote dry, conformal adhesion (details are in the SOM). As examples of high yields, large areas, and compatibility with plastic substrates, Fig. 1I presents images of collections of ILEDs printed onto a thin sheet of polyethylene terephthalate (PET, 50 μm thick), shown as wrapped around a cylindrical glass support (1600 devices, in a square array with pitch of 1.4 mm; radius of cylinder ~25 mm) and onto a plate of glass (inset; 1600 devices, in a square array with pitch of 1.4 mm). The overall fabrication yields, including delineation and undercut of the ILEDs and subsequent printing of them onto the target substrates, were 100% in both cases. The devices were selected to have sizes (i.e., 250 μm by 250 μm) large enough to be visible in the images; those with sizes of Fig. 1D are too small to be seen clearly at these scales.

Establishing electrical connections to these printed ILEDs yields lighting elements or addressable displays. The small thickness (~2.5 μm) of the devices enables the use of conventional thin-film processing, thereby providing a route to displays and related devices that is simpler, more scalable, and applicable to much smaller pixel geometries than established wire bonding and packaging techniques. To demonstrate the most basic scheme, we printed a collection of devices onto a thin, metal mesh on a transparent substrate, to form bottom contacts, and then established separate top contacts using a planar lithographic process (fig. S5). Figure 2, A and B, shows an exploded view schematic illustration and optical micrograph of an array of small, square devices (~25 μm by 25 μm), as well as those with shapes that spell "LED." The results indicate bright emission, even out to the edges of the devices, consistent with the relatively low surface recombination velocity in AlInGaP materials (*15*, *16*). For improved performance, ohmic contacts can be implemented by using established metallization and annealing schemes (*17*, *18*). One strategy involves additional processing on the source wafer to yield released devices with integrated ohmic contacts, suitable for printing and interconnection even on low-temperature substrates such as plastic or rubber. An alternative is to use low-temperature approaches to establish the ohmics directly on such substrates. For this work, we pursued the second strategy, using processes that involve temperatures below 175°C (see SOM for details and fig. S6 for transmission-line model analysis of the contact resistances). Figure 2C shows the layout of an ILED with ohmic contacts printed onto a thin layer of polyurethane on a glass substrate, and an optical micrograph of emission from a directly probed device. Figure 2, D and E, presents electrical and optical characteristics of a set of such devices, recorded on the wafer before undercut etching and after printing. The processing in this case used a passivation scheme to eliminate moderate degradation in performance associated with the HF etching step on unprotected devices (fig. S7). The resulting current-voltage-emission behavior of the printed devices is comparable to that of the devices on the wafer (see SOM for processing details and for statistics on devices with two different sizes).

Figure 3A provides a schematic illustration of an interconnect scheme for passive matrix addressing. Photolithography and electron beam evaporation define patterned metal electrodes [Ti (20 nm)/Au (300 nm)] that connect p and n contacts (nonohmic for the cases of Figs. 3 and 4) of devices in common columns and rows, respec-

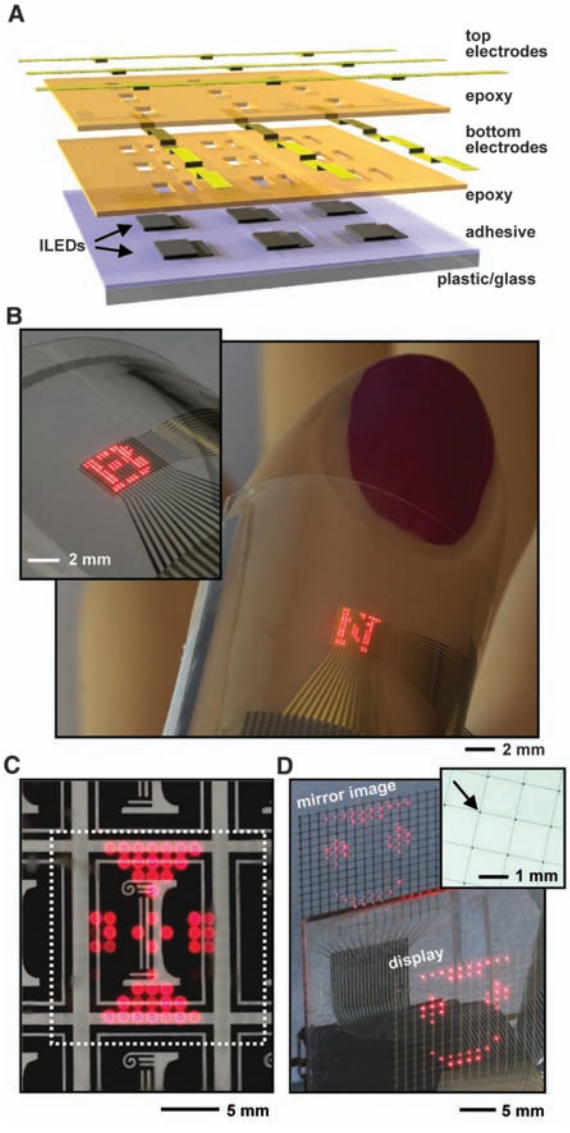

Fig. 3. (**A**) Schematic illustration of a planar scheme for interconnecting a printed array of ILEDs in a passive matrix layout. Coordinated control of voltages applied to the row and column electrodes allows operation in a passive matrix display mode. (**B**) Images of a flexible display that incorporates a 16 by 16 array of ILEDs in the layout shown in (A), on a sheet of plastic (PET), wrapped around the thumb of a mannequin hand (main panel; human scale; radius ~8 mm) and a cylindrical glass tube (inset; radius ~12 mm). External interface to control electronics occurs through ribbon cables bonded to column and row electrodes that emerge from the periphery of the display. (**C**) Image of a comparatively large, semitransparent display that uses a similar layout but with a sparse array of ILEDs on a glass substrate. The camera is focused on the paper in the background; the white dashed box illustrates the perimeter of the active region of the display. (**D**) Image of a similar device (bottom right) displaying a different pattern in front of a mirror (upper left), to illustrate the bidirectional emission property. In this system, the ILEDs represent only ~0.8% of the total area. The inset shows a magnified view of a region of the display in its off state, to illustrate the small areal coverage of the devices. The black arrow points to one of the ILEDs, which is barely visible at this magnification.

tively. Two spin-cast, photopatterned layers of epoxy (1.2 μm thick) provide openings to these contacts; the top layer electrically separates the column and row electrodes at their crossing points. Connecting terminal pads at the ends of these electrode lines to external computer control systems via ribbon cables that use anisotropic conductive films (ACFs) enables passive matrix addressing (see SOM and fig. S8 for details). Figure 3B shows images of a small display that uses this design, formed on a thin sheet of plastic (PET, 50 μm thick) with a layer of a photocurable polyurethane as an adhesive. The ILEDs have dimensions of 100 μm by 100 μm and are configured into a 16 by 16 square array. The yields on the individual pixels for the case of Fig. 3B are 100%; at the level of the display, one column and two rows do not function, due to breaks in the contacts to the ACF ribbon cable [fig. S9; see SOM and fig. S10 for an example of similar display with even smaller ILEDs (50 μm by 50 μm)]. Such systems can be bent to radii of curvature of ~7 mm, with no observable degradation, even for several hundred cycles of bending (fig. S11). Analytical calculation shows that even at the minimum bend radius investigated here, the maximum strain in the ILED is 0.21%, with a somewhat smaller strain (0.19%) in the quantum well region (see SOM for details). Analysis using literature parameters to determine the dependence of the bandgap on strain (*19*–*22*) suggests changes in emission wavelength of ~2.4 nm for the smallest bend radius (see SOM for details).

As shown in Fig. 1, step-and-repeat printing can yield systems that cover areas much larger than those of the constituent ILEDs or the source wafer. One important outcome is the ability to form displays that can offer an effectively high level of transparency, where only the ILEDs (and the electrodes, if they are not made with transparent conductors) are opaque. Figure 3, C and D, shows examples of a 16 by 16 array, formed on glass. Here the area of the display is ~325 mm^2; the cumulative area of all the ILEDs is only ~2.5 mm^2, corresponding to less than ~1% of the display area. Figure 3C illustrates the operation of such a system positioned above a sheet of paper with printed logos; the focus of the image is on the paper, thereby illustrating a practical level of transparency for application in a heads-up display, for example. Figure 3D shows the same device (lower right), operating in front of a mirror (upper left) to demonstrate bidirectional emission characteristics. The inset provides a magnified view of a region of this display, in its off state to show the small sizes of the ILEDs compared to the unit cells. These layouts are critically important for many applications, due to the efficient utilization of the LED material, for reduced cost. For the examples shown, we achieved ~98% yields on the individual devices, and ~80% yields on the interconnections, limited by breaks in the metal lines and failed contacts to the ACF ribbon cable (fig. S12).

The devices and integration methods reported here are compatible with strategies to produce stretchable electronics (*12*, *13*), thereby providing a route to conformable displays and lighting systems of the type that might be interesting for integration with the human body and other curvilinear, deformable surfaces, all of which demand more than simple bending (e.g., Fig. 3B). Figure 4A shows an example of a stretchable ILED with the shape of a ribbon. This device was formed by transfer printing and bonding to a prestrained, rubber substrate of PDMS. Relaxing the prestrain creates a device with a "wavy," sinusoidal profile; this structure responds elastically to applied strain with a physics similar to that of an accordion bellows (*12*, *23*) to yield a stretchable ILED device. The top panels provide finite element simulation of the mechanics of the system in compressed (left) and stretched (right) configurations. The results indicate maximum strains in the ILED and the quantum well region of 0.36 and 0.053%, respectively (see SOM for details). The bottom panels show optical micrographs in the off (top) and on (bottom) states, with and without external illumination, respectively, in configurations similar to those illustrated in fig. S18A. The emission characteristics show no noticeable change in color with applied strain or associated changes in device geometry from "wavy" to flat (see SOM and figs. S13 and S14 for details). This observation is consistent with a calculated change in emission wavelength of less than ~0.7 nm based on our computed strain values and analysis similar to that performed for the flexible display (see SOM for details).

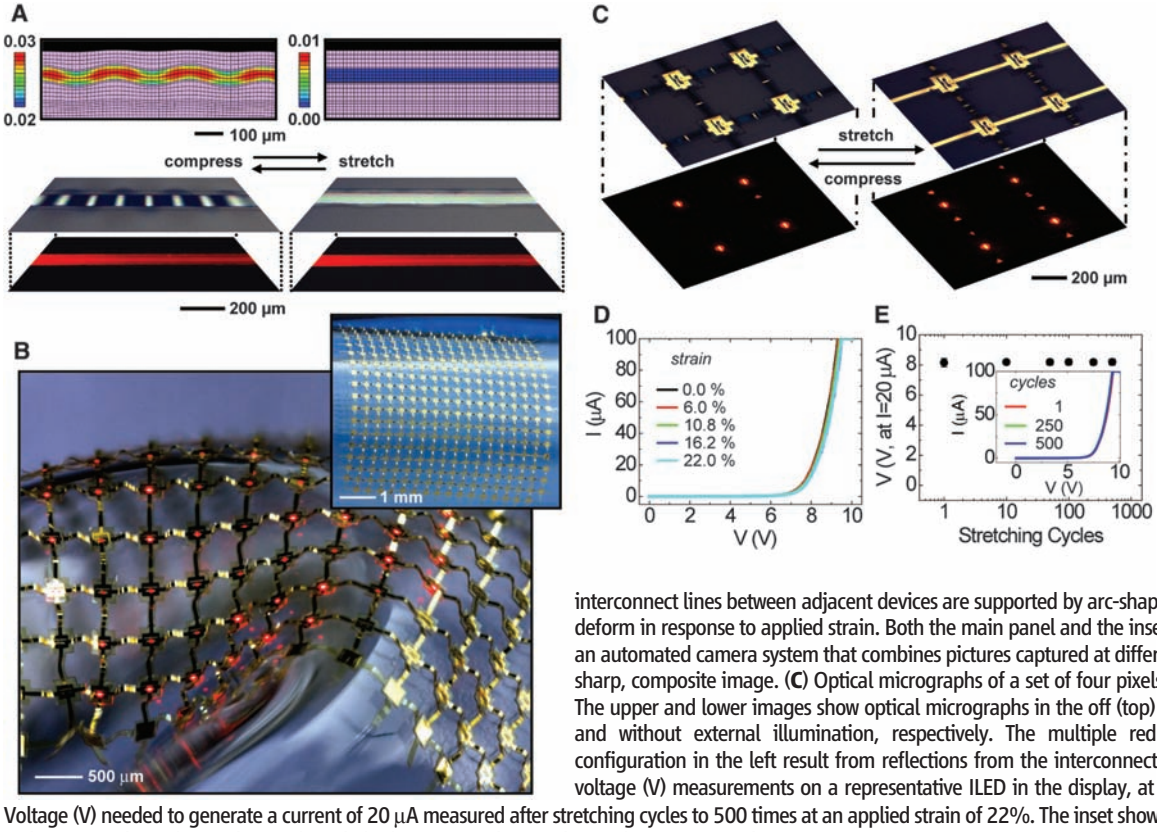

Fig. 4. (**A**) Color plots of the strain distributions (in percent) at the quantum well region and the corresponding finite element mesh used for simulation (top) and optical micrographs (bottom) of a stretchable ILED on a rubber substrate in unstrained and strained states. The bottom panels show optical micrographs in the off (top) and on (bottom) states, with and without external illumination, respectively. (**B**) Passive matrix, stretchable ILED display that uses a noncoplanar mesh configuration, on a rubber substrate. Here, interconnect lines between adjacent devices are supported by arc-shaped bridge structures that can deform in response to applied strain. Both the main panel and the inset images were collected with an automated camera system that combines pictures captured at different focal depths to provide a sharp, composite image. (**C**) Optical micrographs of a set of four pixels in the display shown in (B). The upper and lower images show optical micrographs in the off (top) and on (bottom) states, with and without external illumination, respectively. The multiple red spots in the case of the configuration in the left result from reflections from the interconnection bridges. (**D**) Current (I)–voltage (V) measurements on a representative ILED in the display, at different applied strains. (**E**) Voltage (V) needed to generate a current of 20 μA measured after stretching cycles to 500 times at an applied strain of 22%. The inset shows the *I*-*V* behavior after these cycling tests. These devices have relatively high turn-on voltages, due to the use of nonohmic contacts.

The "wavy" strategy of Fig. 4A can accommodate only a relatively modest range of applied strains (i.e., up to a few percent, for the designs reported here). A path to displays with high levels of stretchability uses non-coplanar mesh designs adapted from schemes reported for integrated circuits (*13*). Figure 4B presents optical micrographs of such a system, composed of a 16 by 16 square array of ILEDs bonded to a PDMS substrate and interconnected by electrodes supported by arc-shaped bridges, with a fraction of the pixels turned on (overall yield >80%) (see SOM and fig. S15 for details). The shapes of these bridges change in response to deformations of the display, in a way that isolates the ILEDs from any significant strains (figs. S16 and S17). In particular, calculation shows that for strains of 24%, as defined by the change in separation between inner edges of adjacent device islands, the maximum strains in the ILED and quantum well are only 0.17 and 0.026%, respectively. The computed change in emission wavelength is less than ~0.3 nm (see SOM for details). Figure 4C provides optical micrographs of four pixels in this display, in their off and on states, with (top) and without (bottom) external illumination, respectively, in compressed and stretched configurations. The images show the expected reduction in the heights of the arc-shaped bridges that lie in the direction of the applied tensile force (i.e., along the interconnects that run from lower left to upper right), together with an increase in the heights of the bridges in the orthogonal direction, due to the Poisson effect. This mechanical response is fully elastic—the bending-induced strains in the interconnects are small, the strains in the ILEDs are negligible, and the strain in the PDMS is well within its linear response regime. The data in Fig. 4, D and E, are consistent with this mechanics, as are the associated mechanics calculations. In particular, the current-voltage characteristics of a typical device do not change in a measurable way for applied strains up to ~22%, and we observe no degradation on cycling up to a few hundred times (500 times). Recent work demonstrates the use of smaller collections of large, conventional ILEDs in deformable devices that use different designs (*24*, *25*).

The schemes reported here for creating thin, small inorganic LEDs and for integrating them into display and lighting devices create design options that are unavailable with conventional procedures. The planar processing approaches for interconnect resemble those that are now used for organic devices and, for example, large-area electronics for liquid crystal displays, thereby conferring onto inorganic LED technologies many of the associated practical advantages. In large-area, high–pixel count systems (e.g., 1 million pixels per square meter), the ability to use LEDs with sizes much smaller than those of the individual pixels is critically important to achieve efficient utilization of the epitaxial semiconductor material, for reasonable cost. The minimum sizes of devices reported here are limited only by the resolution and registration associated with manual tools for photolithography.

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Supporting Online Material

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Materials and Methods
Figs. S1 to S19
References

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Visualization of Fermi's Golden Rule Through Imaging of Light Emission from Atomic Silver Chains

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Atomic-scale spatial imaging of one-dimensional chains of silver atoms allows Fermi's golden rule, a fundamental principle governing optical transitions, to be visualized. We used a scanning tunneling microscope (STM) to assemble a silver atom chain on a nickel-aluminum alloy surface. Photon emission was induced with electrons from the tip of the STM. The emission was spatially resolved with subnanometer resolution by changing the tip position along the chain. The number and positions of the emission maxima in the photon images match those of the nodes in the differential conductance images of particle-in-a-box states. This surprising correlation between the emission maxima and nodes in the density of states is a manifestation of Fermi's golden rule in real space for radiative transitions and provides an understanding of the mechanism of STM-induced light emission.

The scanning tunneling microscope (STM), which is based on the tunneling effect, has been used to visualize various quantum phenomena in real space, including the quantum corral (*1*), quantum mirage (*2*), and particle-in-a-box states (*3*, *4*). All of these demonstrations involved the localization of the electron density of states in confined nanostructures. Light emission from the STM junction reveals a different kind of quantum phenomenon that involves the optical transitions and inelastic electron tunneling (IET) processes in single molecules (*5*, *6*) and nanostructures (*7*). Furthermore, photon intensity imaging with atomic resolution has been demonstrated (*8*–*10*). The spatial resolution in these optical experiments originates from the precision of the STM in injecting electrons in a confined space, although the emitted photons are collected in the far field. This atomic-scale optical detection can reveal aspects of the molecules and nanostructures that are hidden when probed with other techniques.

Imaging of STM light emission has not yet been directly correlated with the underlying elec-

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Supporting Online Material for

Printed Assemblies of Inorganic Light-Emitting Diodes for Deformable and Semitransparent Displays

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SUPPLEMENTARY ONLINE MATERIAL

"Printed Assemblies of Microscale Inorganic Light Emitting Diodes for Deformable and Semitransparent Displays"

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MATERIALS AND METHODS

The materials and methods for this project, including epitaxial semiconductor multilayer design, polymeric anchor structures, large scale printing techniques, and electrical interconnection in direct or matrix addressable configurations, are described in the following, for the flexible display, the large area display, the array of inorganic light emitting diode (ILED) devices with ultrasmall sizes/arbitrary shapes, the wavy ribbon devices, and the stretchable display.

Preparation of ILEDs

Figure S1 shows the epi-stack design for our ILEDs, capable of release from a source wafer by undercut etching, grown on a GaAs wafer (Epiworks, Inc.). The sequence of processing steps used to retrieve ILEDs array appears below. Polymeric anchor structures support the ILEDs during undercut etching of the $Al_{0.96}Ga_{0.04}As$ sacrificial layer (fig. S2).

Processing Scheme for Preparing ILEDs from a Source Wafer

Delineating the ILEDs

1. Clean an epi-stack ILED wafer chip (acetone, isopropyl alcohol (IPA), deionized (DI) water).

2. Deposit 800 nm SiO_2 by plasma enhanced chemical vapor deposition (plasma enhanced chemical vapor deposition (PECVD); PlasmaTherm SLR).

3. Pretreat with hexamethyldisilazane (HMDS) for 1 min.

4. Pattern photoresist (PR; Clariant AZ5214, 3000 rpm, 30 sec) with 365 nm optical lithography through an iron oxide mask (Karl Suss MJB3). Develop in aqueous base developer (Clariant AZ327 MIF) and bake on hot plate ($110^{o}C$, 3 min).

5. Etch oxide with buffered oxide etchant (BOE; Fisher, 130 sec).

6. Etch with an inductively coupled plasma reactive ion etcher (ICP-RIE; Unaxis SLR 770 System, 2 mTorr, Cl_2 4 sccm, H_2 2 sccm, Ar 4 sccm, RF1: 100 W, RF2: 500 W, ~21 min).

Undercut etching of the ILEDs

7. Clean the processed wafer chip from step 6 above with HF (Fisher, 49%, diluted 10:1, 2 sec).

8. Pattern PR and bake at $110^{o}C$ for 5 min to form polymeric anchors at the corners of the μ-ILEDs.

9. Dip the wafer chip in diluted HF (Fisher, 49%, diluted 100:1) for an appropriate time (μ-ILEDs with 50 μm x 50 μm dimension: ~4 hrs, 100 μm x 100 μm: ~5.5 hrs) to remove the $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the ILEDs. Rinse by-product using DI water at 1.5 hr intervals.

Device Fabrication

Processing Scheme for ILED devices of Fig. 2A

Schematic illustration of these steps appears in fig. S5.

Preparing a substrate with metal mesh

1. Deposit 300 nm SiO_2 with PECVD onto a silicon wafer

2. Pretreat surface with HMDS for 1 min, and then pattern PR.

3. Deposit 7/70 nm of Cr/Au by electron beam evaporation.

4. Lift-off PR in acetone to yield a pattern of Cr/Au in the geometry of a mesh.

5. Etch oxide with HF (49%, 38 sec).

6. Transfer print mesh to a glass substrate coated with poly(dimethylsiloxane) (PDMS; Sylgard 184, Dow Corning, spun at 600 rpm/5 sec, 3000 rpm/30 sec, cured in oven at $70^{o}C$ for 90 min) formed by mixing the base and curing agent with a ratio of 10:1 followed by thermal curing.

Printing the ILEDs

7. Liftoff ILEDs using a flat PDMS stamp formed by mixing the base and curing agent with a ratio of 8.5:1.5, and then thermally cure.

8. Print ILEDs onto the glass substrate with Cr/Au mesh (n-contact).

9. Remove PR by washing in acetone.

Forming the interlayer and p-contact metallization

10. Spin coat the substrate from step 9 with a photodefinable epoxy (SU8-2, Microchem, spun at 1,500 rpm for 30 s). Soft bake at $65^{o}C$ and $95^{o}C$ for 1 min and 1.5min, respectively.

11. Pattern epoxy by exposing to ultraviolet (UV) light in a mask aligner for 14 sec, baking at $95^{o}C$ for 2 min, developing (SU8 developer, Microchem) for 15 sec, rising (IPA), and curing ($110^{o}C$, 35 min, slow cooling).

12. Pattern PR.

13. Deposit 7 nm of Pd-Au by sputtering.

14. Lift-off PR in acetone to leave a thin layer of Pd-Au on the top surfaces of the ILEDs (p-contact).

Processing Scheme for ILED devices with ohmic contacts of Fig. 2C

Preparing the substrate

1. Clean a glass slide (25 mm X 25 mm) (acetone, IPA, DI water)

2. Expose to ultraviolet induced ozone (UVO) for 5 min.

3. Spin coat with polyurethane (NOA61; Norland Products Inc., spun at 5000 rpm/60 sec).

Delineating the ILEDs

4. Clean an epi-stack ILED wafer chip (acetone, IPA, DI water).

5. Deposit 800 nm SiO_2 with PECVD.

6. Pretreat with HMDS for 1 min.

7. Pattern PR and bake on hot plate ($110^{o}C$, 3 min).

8. Etch oxide with BOE (130 sec).

9. Etch with ICP-RIE (2 mTorr, Cl_2 4 sccm, H_2 2 sccm, Ar 4 sccm, RF1: 100 W, RF2: 500 W, ~16 min) to expose $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the ILEDs.

Forming a passivation layer and undercut etching of the ILEDs

10. Clean the processed wafer chip from step 9 above (acetone, IPA, DI water).

11. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at 65^oC and 110^oC each for 1 min and 1 min, respectively.

12. Pattern epoxy by exposing to UV, baking, developing, rising (IPA), and curing. The pattern includes a passivation structure to protect μ-ILEDs and an anchor structure to suspend ILEDs during the undercut etching.

13. Dip the wafer chip in diluted HF (49%, diluted 100:1) for ~2 hrs to remove the $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the μ-ILEDs.

Printing the ILEDs

14. Liftoff ILEDs using a flat PDMS stamp formed by mixing the base and curing agent with a ratio of 10:1, followed by thermal curing. Contact 'inked' stamp against the substrate from step 13.

15. Retrieve the stamp after UV exposure (through the stamp) for 20 min. Cure the polyurethane layer by UV exposure for 2 hours.

Defining the n-contact regions

16. Reactive ion etch (RIE; PlasmaTherm 790 Series, 50 mTorr, 20 sccm O_2, 100 W, ~12 min) to remove the epoxy on the top surface of the ILEDs.

17. Pattern PR and bake at 110^oC for 2 min.

18. Wet etch C-doped p-GaAs/p-spreader($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (volume ratio 1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader ($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

19. Remove PR by washing in acetone.

Defining the n-ohmic contact metallization

20. Pattern PR.

21. Clean the surface of n-GaAs with HCl : DI water (1:1) for 30 sec.

22. Deposit 5/35/70 nm of Pd/Ge/Au by electron beam evaporation.

23. Lift-off PR in acetone to remain Pd/Ge/Au on the top surface of n-GaAs.

24. Anneal at 175 ^oC for 60min under N_2 ambient

Defining the p-ohmic contact metallization

25. Pattern PR.

26. Clean the surface of p-GaAs with HCl : DI water (1:1) for 30 sec.

27. Deposit 10/40/10/70 nm of Pt/Ti/Pt/Au by electron beam evaporation.

28. Lift-off PR in acetone to remain Pt/Ti/Pt/Au on the top surface of p-GaAs.

Processing Scheme for Flexible ILED Displays of Fig. 3B

Preparing the substrate

1. Clean a glass slide (30 mm X 30 mm) (acetone, IPA, DI water).

2. Treat with ultraviolet induced ozone (UVO) for 5 min.

3. Spin coat with PDMS (spun at 600 rpm/5 sec, 3000 rpm/30 sec), formed by mixing the base curing agent with a ratio of 10:1.

4. Cure PDMS in an oven ($70\,^{o}C$, 90 min).

5. Clean a sheet of polyethylene terephthalate (PET; Grafix DURA-LAR, 32 mm X 32 mm X 50 μm) (IPA, DI water).

6. Laminate the PET sheet onto the PDMS coated glass slide, as a carrier for the following processing steps.

7. Spin coat with polyurethane (NOA61; Norland Products Inc., spun at 5000 rpm/60 sec).

Printing the ILEDs

8. Liftoff an array of ILEDs (16x16 array of devices with dimensisons of 100μm x 100μm) using a flat PDMS stamp. Contact 'inked' stamp against the substrate from step 7.

9. Retrieve the stamp after UV exposure (through the stamp) for 20 min.

10. Remove PR by washing in acetone and then cure the polyurethane layer by UV exposure for 2 hours.

Defining the n-contact regions

11. Reactive ion etch (RIE; PlasmaTherm 790 Series, 50 mTorr, 20 sccm O_2, 100 W, 8 min) to remove the polyurethane layer covering the ILEDs.

12. Pattern PR and bake at 110^oC for 2 min.

13. Wet etch C-doped p-GaAs/p-spreader($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (volume ratio 1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader ($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

14. Remove PR by washing in acetone.

Defining the n-contact metallization

15. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at 65^oC and 110^oC each for 1 min and 1 min, respectively.

16. Pattern epoxy by exposing to UV, baking, developing, rising (IPA), and curing.

17. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

18. Pattern PR and bake at 110^oC for 2 min.

19. Wet etch Ti/Au for 45/90 sec by BOE and Au etchant (Transene, Inc.).

20. Remove PR by washing in acetone.

Defining the p-contacts and p-contact metallization

21. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at 65^oC and 110^oC for 1 min and 1 min, respectively.

22. Pattern epoxy by exposing to UV, developing, rising, and curing.

23. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

24. Pattern PR and bake at $110^{o}C$ for 2 min.

25. Wet etch Ti/Au for 45/90s by BOE and Au etchant.

26. Remove PR by washing in acetone.

Forming an encapsulation layer

27. Spin coat with epoxy (SU8-5, Microchem, spun at 3,000 rpm for 30 s). Soft bake at $65^{o}C$ and $110^{o}C$ for 1 min and 1.5min, respectively.

28. Pattern epoxy by exposing to UV for 14 sec, baking at $95^{o}C$ for 2 min, developing (SU8 developer) for 18 sec, rising (IPA), and curing ($110^{o}C$, 35 min, slow cooling)

<u>Processing Scheme for Large Area ILEDs Displays of Fig. 3, C and D</u>

Preparing the substrate

1. Clean a glass slide (50 mm X 50 mm) (acetone, IPA, DI water)

2. Deposit 50 nm of Ti by electron beam evaporation.

3. Pattern PR and bake on a hot plate ($110^{o}C$, 2 min) to form guide lines to assist in registration of ILEDs printed with an automated printer system.

4. Wet etch Ti with BOE (70 sec).

5. Remove PR by washing in acetone.

6. Expose to ultraviolet induced ozone (UVO) for 15 min.

7. Spin coat with PDMS (spun at 600 rpm/5 sec, 2500 rpm/30 sec) formed by mixing the base and curing agent with a ratio of 10:1.

8. Cure PDMS in an oven ($70^{o}C$, 90 min)

Printing the ILEDs

9. Selectively liftoff ILEDs (100μm x 100μm lateral dimensions) using a composite stamp in automated printing machine (fig. S3, S4) and print them onto the substrate from step 8, in a step and repeat fashion to form a 16x16 array.

10. Remove PR by washing in acetone.

Patterning the p-contact metallization

11. Spin coat with epoxy (SU8-2, spun at 1,500 rpm for 30 s). Soft bake at $65^{o}C$ and $110^{o}C$ for 1 min and 1min, respectively.

12. Pattern epoxy by exposing to UV, baking, developing, rising, and curing.

13. Deposit 10/70 nm of Ti/Au by electron beam evaporation.

14. Pattern PR and bake at $110^{o}C$ for 2 min.

15. Wet etch Ti/Au with BOE and gold etchant for 35/20 sec.

16. Remove PR by washing in acetone.

17. Reactive ion etch (RIE, 50 mTorr, 20 sccm O_2, 100 W, 13 min) to remove remaining epoxy around the sidewalls of the ILEDs (fig. S8).

Defining the n-contact regions

18. Pattern PR and bake at $110^{o}C$ for 2 min.

19. Wet etch C-doped p-GaAs/p-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

20. Remove PR by washing in acetone.

Patterning the n-contact metallization

21. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at 65^oC and 110^oC for 1 min and 1 min, respectively.

22. Pattern epoxy by exposing to UV, baking, developing, rising, and curing.

23. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

24. Pattern PR and bake at 110^oC for 2 min.

25. Wet etch Ti/Au for 45/90 sec with BOE and Au etchant.

26. Remove PR by acetone rinse.

Defining the p-contact regions and metallization

27. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at 65^oC and 110^oC for 1 min and 1 min, respectively.

28. Pattern epoxy with exposing UV, developing, rising, and curing.

29. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

30. Pattern PR and bake at 110^oC for 2 min.

31. Wet etch Ti/Au for 45/90s by BOE and Au etchant.

32. Remove PR by acetone.

Forming an encapsulation layer

33. Spin coat with epoxy (SU8-5, spun at 3,000 rpm for 30 s). Soft bake at $65^{o}C$ and $110^{o}C$ for 1 min and 1.5min, respectively.

34. Pattern epoxy by exposing to UV, baking, developing, rising, and curing.

Processing Scheme for stretchable ILEDs of Fig. 4A

Exploded view schematic illustration of the processing step appears in fig. S14.

Preparing ribbon shaped ILEDs

1. Clean an epi-stack ILED wafer chip (acetone, IPA, DI water).

2. Pattern PR and bake for 2 min.

3. Wet etch C-doped p-GaAs/p-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 35 sec to expose $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the μ-ILEDs.

4. Remove PR by washing in acetone.

Forming an encapsulation layer and undercut etching

5. Pattern PR on the top surface of the ribbons.

6. Deposit 3/15 nm of Ti/Au by electron beam evaporation.

7. Lift-off PR in acetone to remain Ti/Au on the top surface of the ribbons

8. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at $65^{o}C$ and $95^{o}C$ for 1 min and 1.5min, respectively.

9. Pattern epoxy by exposing to UV, baking, developing, rising (IPA), and curing.

10. Dip the ILED in diluted HF (100:1) for 1 hr to release the ribbons from the wafer.

11. Rinse in DI water for 5 min.

12. Print ribbons onto a pre-strained substrate of PDMS with prepatterned metal lines.

Processing Scheme for Stretchable ILED Display of Fig. 4, B and C

Schematic illustration of the processing steps appears in fig. S16.

Preparing the carrier substrate

1. Clean a glass slide (25 mm X 25 mm) (acetone, IPA, DI water).

2. UVO treatment for 5 min.

3. Spin coat with PMMA (A2, Microchem, spun at 3,000rpm for 30 sec).

4. Anneal at $180^{o}C$ for 3 min.

5. Spin coat with polyimide (PI, poly(pyromellitic dianhydride-co-4,4´ -oxydianiline), amic acid solution, Sigma-Aldrich, spun at 4,000 rpm for 60 sec).

6. Anneal at $110^{o}C$ for 3 min and $150^{o}C$ for 10 min.

7. Anneal at $250^{o}C$ for 50 min in N_2 atmosphere.

8. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at $65^{o}C$ and $95^{o}C$ for 1 min and 1 min, respectively.

Printing the ILEDs

9. Liftoff ILEDs (16x16 array of devices with dimensions of 50 μm x 50 μm) using a flat PDMS stamp and contact the 'inked' stamp with the substrate from step 8.

10. Remove the stamp after UV exposure (through the stamp) for 60 sec and baking at $110^{o}C$ for 10 min.

11. Remove PR by washing with acetone. Fully cure the epoxy layer at $150^{o}C$ for 20 min.

Forming the sidewall region

12. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at $65^{o}C$ and $95^{o}C$ for 1 min and 1 min, respectively.

13. Expose to UV for 14 sec and bake at $110^{o}C$ for 1 min.

14. Anneal at $150^{o}C$ for 20 min.

15. Reactive ion etch (RIE; PlasmaTherm 790 Series, 50 mTorr, 20 sccm O_2, 100 W, 13 min) to remove remaining epoxy around the sidewalls of the ILEDs.

Defining the n-contact regions

16. Pattern PR and bake at $110^{o}C$ for 5 min.

17. Wet etch C-doped p-GaAs/p-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

18. Remove PR by washing with acetone.

Defining the n- and p-contact metallization

19. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at $65^{o}C$ and $95^{o}C$ for 1 min and 2 min, respectively.

20. Pattern epoxy by exposing to UV for 14 sec, developing for 15 sec, rising, and curing ($110^{o}C$, 35 min, slow cooling).

21. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

22. Pattern PR and bake at $110^{o}C$ for 2 min to define n-contact electrodes, designed as line patterns connected to n-GaAs, and p-contact electrodes, designed as line patterns that avoid crossing over the n-contact electrodes (fig. S16).

23. Wet etch Ti/Au for 45/90 sec by BOE and Au etchant.

24. Remove PR by washing with acetone.

Interconnecting the p-contact metallization

25. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at $65^{o}C$ and $95^{o}C$ for 1 min and 2min, respectively.

26. Pattern epoxy by exposing to UV, developing, rising, and curing.

27. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

28. Pattern PR and bake at $110^{o}C$ for 2 min.

29. Wet etch Ti/Au for 45/90 sec by BOE and Au etchant.

30. Remove PR by washing with acetone.

Forming and encapsulation layer

31. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at $65^{o}C$ and $95^{o}C$ for 1 min and 1.5min, respectively.

32. Pattern epoxy by exposing to UV, developing, rising, and curing.

Forming the island/bridge structures

33. Deposit 150 nm SiO_2 by PECVD.

34. Pattern PR and bake at $110^{o}C$ for 2 min.

35. RIE (50 mTorr, CF_4/O_2 40/1.2 sccm, 150 W, 8 min) to etch SiO_2.

36. RIE (150 mTorr, O_2 20 sccm, 150 W, 50 min) to etch epoxy/PI layers.

37. Etch oxide with BOE (20 sec).

Transferring the mesh

38. Immerse the ILEDs array mesh from step 37 in acetone ($80^{o}C$) for ~10 min to dissolve the PMMA.

39. Lift off the mesh using a PDMS stamp formed by mixing a base and agent with a ratio of 8.5:1.5.

40. Selectively deposit 5/30 nm of Ti/SiO_2 by electron beam evaporation on the bottom of island regions through a shadow mask.

41. Transfer the ILED mesh to a biaxially pre-strained PDMS substrate.

42. Anneal in an oven at $70^{o}C$ and release the strain.

Measurement of Emission Spectra

Emission spectra were measured using a spectrometer (Oceanoptics, HR4000) which enabled signal collected through an optical fiber directly mounted in an electrical probing station.

Measurement of Surface Profile of Wavy ILEDs

The wavelength and amplitude of stretchable ILEDs of fig. 4A were measured by a surface profiler (Sloan Dektak^3). A diamond stylus in contact with a sample surface scans along the length of ribbon and measures physical surface variation at different positions.

Bending Test

To evaluate the bending performance of flexible ILEDs displays, bending test were performed (fig. S12A, B). The displays were bent and released, with bend radii down to ~ 7.3 mm. The electrical properties of 32 different pixels in the display were measured and averaged to assess the performance.

Fatigue Test

To evaluate the fatigue performance of flexible ILED displays, multiple cycling tests were performed under repetitive bending and releasing up to 500 times (fig. S12C, D). Electrical measurements were performed on 16 different pixels, for a bend radius of ~ 8.8 mm.

Stretching tests were performed with mechanical stages capable of applying uniaxial strain to evaluate the performance of stretchable ILED display under repetitive stretching and releasing up to 500 times (Fig. 4). Electrical properties of 14 different pixels in the display were measured and averaged. In all cases, the testing was performed at a rate of roughly one cycle per second.

Modeling of Flexible ILED Displays of Fig. 3B

The encapsulation, electrode, ILED, adhesive and plastic shown in fig. S8 can be modeled as a composite beam subject to a bend curvature. The distance between the neutral mechanical plane and the top surface in each cross section is given by $\sum_{i=1}^{N} \bar{E}_i h_i \left(\sum_{j=1}^{i} h_j - \frac{h_i}{2} \right) \Big/ \sum_{i=1}^{N} \bar{E}_i h_i$, where N is the total number of layers, h_i is the thickness of the i^{th} layer (from the top), and $\bar{E}_i = E_i \big/ \left(1 - v_i^2\right)$ is related to the Young's modulus E_i and Poisson's ratio v_i of the i^{th} layer. The strain in the μ-ILED, including the quantum well, is given by y/R, where R is the bend radius, and y is the distance from the neutral mechanical plane. The elastic properties and layer thicknesses used for bendable display are (1) $E_{encapsulation}$ = 4.4 GPa, $v_{encapsulation}$ = 0.44, and $h_{encapsulation1}$ = 4.0 μm and $h_{encapsulation2}$ = 0.877 μm for the two encapsulation layers above and below the electrode, respectively; (2) $E_{electrode}$ = 78 GPa, $v_{electrode}$ = 0.44, and $h_{electrode}$ = 300 nm; (3) E_{ILED} = 77.5 GPa, v_{ILED} = 0.312, and h_{ILED} = 2.523 μm; (4) $E_{adhesive}$ = 1 GPa, $v_{adhesive}$ = 0.3, and $h_{adhesive}$ = 2.5 μm; and (5) $E_{plastic}$ = 4 GPa, $v_{plastic}$ = 0.44 and $h_{plastic}$ = 50 μm. These give the neutral mechanical plane 19.76 μm below the top surface. The maximum distance from the ILED is then 14.58 μm to the neutral mechanical plane, which gives the maximum strain 0.21% in the ILED for the bend radius R = 7 mm. The quantum well is 1.011 μm below the top surface of ILED (fig. S1), and is therefore 13.57 μm to the neutral mechanical plane. This gives the maximum strain 0.19% for the bent radius R = 7 mm.

Modeling and Simulation of Stretchable ILEDs of Fig. 4A: the Wavy Design

As shown in fig. S14A, the stretchable ILED consists of the encapsulation, electrode and μ-ILED, and can be modeled as a composite beam with the effective tensile stiffness $\overline{EA} = \sum_{i=1}^{3} \bar{E}_i h_i$ and bending stiffness $\overline{EI} = \sum_{i=1}^{3} \bar{E}_i h_i \left[\left(\sum_{j=1}^{i} h_j \right)^2 - \left(\sum_{j=1}^{i} h_j \right) h_i + \frac{h_i^2}{3} \right] - \frac{\left[\sum_{i=1}^{3} \bar{E}_i h_i \left(\sum_{j=1}^{i} h_j - \frac{h_i}{2} \right) \right]^2}{\overline{EA}}$, where the summation is for the 3 layers of encapsulation, electrode and ILED, h_i is the thickness of the i^{th} layer (from the top), and $\bar{E}_i = E_i \big/ \left(1 - v_i^2\right)$ is related to the Young's modulus E_i and Poisson's ratio v_i of the i^{th} layer. The distance between the neutral mechanical plane and the top surface in each cross section is given by $\sum_{i=1}^{3} \bar{E}_i h_i \left(\sum_{j=1}^{i} h_j - \frac{h_i}{2} \right) \Big/ \overline{EA}$.

The device was formed by transfer printing and bonding to a pre-strained substrate of PDMS. Relaxing the pre-strain creates a device with a 'wave' of the amplitude A and wavelength λ. The bending energy and membrane energy of the wavy device are $U_{bending} = \frac{4\pi^4 \overline{EI} L A^2}{\lambda^4}$ and $U_{membrane} = \frac{1}{2} \overline{EA} L \left[\pi^2 \left(\frac{A}{\lambda} \right)^2 + \varepsilon_{pre} \right]^2$, where L is the length of device and ε_{pre} (<0) is the compressive strain on the device upon the release of the pre-strain in the PDMS.

The strain energy in the PDMS substrate due to the sinusoidal displacement profile on its top surface is $U_{substrate} = \bar{E}_s L \frac{\pi A^2}{4\lambda}$, where $\bar{E}_s = E_s \big/ \left(1 - v_s^2\right)$ is related to the Young's modulus E_s and

Poisson's ratio v_s of the PDMS substrate. The minimization of the total energy $U_{total} = U_{bending} + U_{membrance} + U_{substrate}$ gives analytically the wave length and amplitude as

$$\lambda = 2\pi \left(\frac{4\overline{EI}}{\overline{E}_s} \right)^{1/3}, \qquad (1)$$

$$A = \frac{\lambda}{\pi} \sqrt{\left| \varepsilon_{pre} \right| - \varepsilon_{crit}}, \qquad (2)$$

where $\varepsilon_{crit} = \frac{3}{2} \left[\frac{\overline{EI}\overline{E}_s^{\,2}}{2\left(\overline{EA}\right)^3} \right]^{1/3}$ is the critical strain for buckling.

The strain in the ILED, including the quantum well, is given by $4\pi^2 \frac{A}{\lambda^2} y$, where y is the distance from the neutral mechanical plane. The elastic properties and layer thicknesses used for the device are (1) $E_{encapsulation}$ = 4.4 GPa, $v_{encapsulation}$ = 0.44, and $h_{encapsulation1}$ = 1 μm; (2) $E_{electrode}$ = 78 GPa, $v_{electrode}$ = 0.44, and $h_{electrode}$ = 10 nm; and (3) E_{ILED} = 77.5 GPa, v_{ILED} = 0.312, and h_{ILED} = 2.523 μm. These give the neutral mechanical plane 2.22 μm below the top surface. The maximum distance from the ILED is then 1.31 μm from the neutral mechanical plane, which gives the maximum strain 0.36% in the ILED for the experimentally measured wavelength 275 μm and amplitude 5.15 μm. The quantum well is 1.011 μm below the top surface of ILED (fig. S1), and is therefore 0.2 μm to the neutral mechanical plane, which gives a very small strain 0.053% in the quantum well.

The finite element method has also been used to determine the strains in the 1.0 μm-thick SU8 encapsulation, 10 nm-thick Au thin film and 2.523 μm-thick ILED on 1 mm-thick PDMS substrate. Eight-node, hexahedral brick elements (C3D8) and four-node multi-layer shell elements (S4R) in the finite element analysis software ABAQUS (2007) are used for the substrate and the thin film, respectively. The multi-layer shell is bonded to the substrate by sharing the nodes. Each layer of thin film is linear elastic, while the PDMS substrate is modeled as a hyper-elastic material. The eigenvalues and eigenmodes of the system are first obtained. The eigenmodes are then used as initial small geometrical imperfections to trigger buckling of the system. The imperfections are always small enough to ensure that the solution is accurate. As shown in fig. 4A and fig. S19, the numerical results give strains that agree very well with the analytical model.

Simulation of Stretchable ILED of Fig. 4, B and C: the Island-Bridge Design

The finite element method has also been used to determine the strains in island-bridge design of stretchable ILED shown in fig. S16. Eight-node, hexahedral brick elements (C3D8) in the finite element analysis software ABAQUS (2007) are used for the substrate, which is modeled as a hyper-elastic material. Four-node, multi-layer shell elements (S4R) are used for the islands and bridges, which are linear elastic. The islands are bonded to the substrate by sharing the nodes, but the bridges do not. Figure S20 shows the strain distribution in the top, middle and bottom surfaces of the ILED as the bridge length is reduced from 310 μm to 250 μm. The maximum strain is 0.17%, and that in the quantum well is only 0.026%.

Analysis of Flexible/Stretchable ILED System for Strain Sensitivity of Emission Wavelength

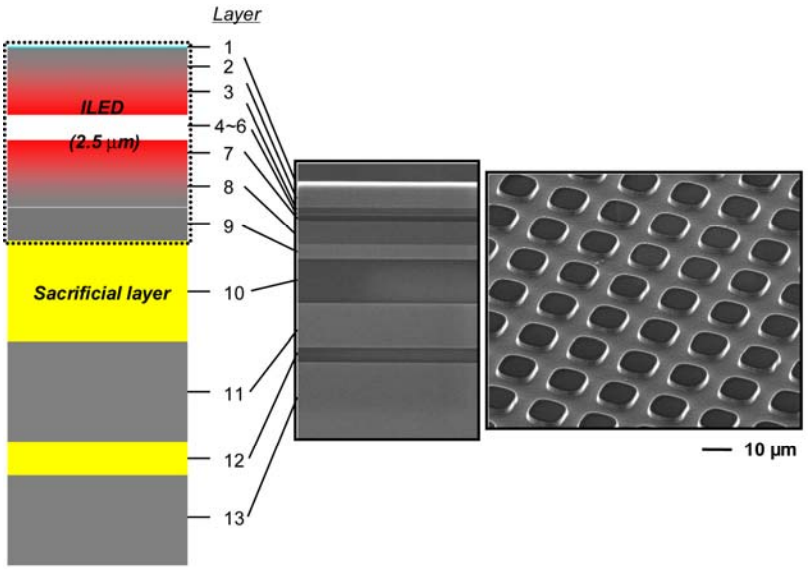
The calculated maximum uniaxial strains in the quantum well of the ILED system are 0.19% tensile in flexible ILED displays, 0.053% tensile in stretchable ILED, and 0.026% compressive in stretchable ILED displays. On the basis of the *kp* perturbation theory *(S1, 2)* for strain induced effect on semiconductor band structures, emission wavelength shift of the ILED associated with bending or stretching can be evaluated.

The bending and stretching deformations explored correspond to in-plane uniaxial stress defined as in the x direction here, and the stresses in the y and z directions are zero ($\sigma_{yy} = \sigma_{zz} = 0$) due to free contraction by Poisson's effect. Thus the strains in these directions are given by $\varepsilon_{yy} = \varepsilon_{zz} = -\nu\varepsilon_{xx}$, where $\frac{\nu}{1-\nu} = \frac{C_{12}}{C_{11}}$, and ν is Poisson's ratio, C_{11} and C_{12} are elastic stiffness constants. For the small stress range examined here, the strain induced bandgap shifts for heavy hole (HH) and light hole (LH) are given by $\delta Eg^{LH} = \delta E_H + \delta E_S$, $\delta Eg^{HH} = \delta E_H - \delta E_S$, where $\delta E_H = a\left(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}\right)$, $\delta E_S = \frac{b}{2}\left(\varepsilon_{xx} + \varepsilon_{yy} - 2\varepsilon_{zz}\right)$, and δE_H, and δE_S are the hydrostatic-pressure shift and the uniaxial stress-induced valence-band splitting, respectively *(S1-3)*, and a and b are the corresponding deformation potentials.

For the quantum well ($In_{0.56}Ga_{0.44}P$) in the ILED structure, the parameters used for the present calculation are a = -7.42 eV, b = 1.91 eV, C_{11} = 11.936x10^{11} dyne/cm^2, and C_{12} = 5.975x10^{11} dyne/cm^2 *(S4)*. Assuming HH is the ground state for the quantum well *(S4)*, the maximum

uniaxial mechanical stress induced bandgap shift in the ILED system studied here is calculated to be ~7.1 meV (or ~2.4 nm). This small shift can be considered negligible for most applications.

SUPPORTING FIGURES



Layer	Layer Name	Material	Thickness (nm)	Type	Dopant	Concentration (cm^{-3})
1	Contact	GaAs	5	P	C	1.00E+19
2	Spreader	$Al_{0.45}Ga_{0.55}As$	800	P	C	1.00E+18
3	Clad	$In_{0.5}Al_{0.5}P$	200	P	Zn	3E17 to 6E17
4	Barrier	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6	-	-	<1E16
5	Well	$In_{0.56}Ga_{0.44}P$	6	-	-	<1E16
6	Barrier	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6	-	-	<1E16
7	Clad	$In_{0.5}Al_{0.5}P$	200	N	Si	1.00E+18
8	Spreader	$Al_{0.45}Ga_{0.55}As$	800	N	Si	1.00E+18
9	Contact	GaAs	500	N	Si	4.00E+18
10		$Al_{0.96}Ga_{0.04}As$	1500	N	Si	1.00E+17
11		GaAs	1500	N	Si	1.00E+17
12		$Al_{0.96}Ga_{0.04}As$	500	N	Si	1.00E+17
13	Substrate	GaAs		N	Si	>1E18

Figure S1. Schematic illustration (left) and cross sectional scanning electron microscope (SEM) image (middle) of the epitaxial semiconductor multilayer stack on a GaAs wafer. (Right) SEM image of a square array of laterally delineated, square ILEDs on a GaAs wafer. (Bottom) Details of the epi-stack.

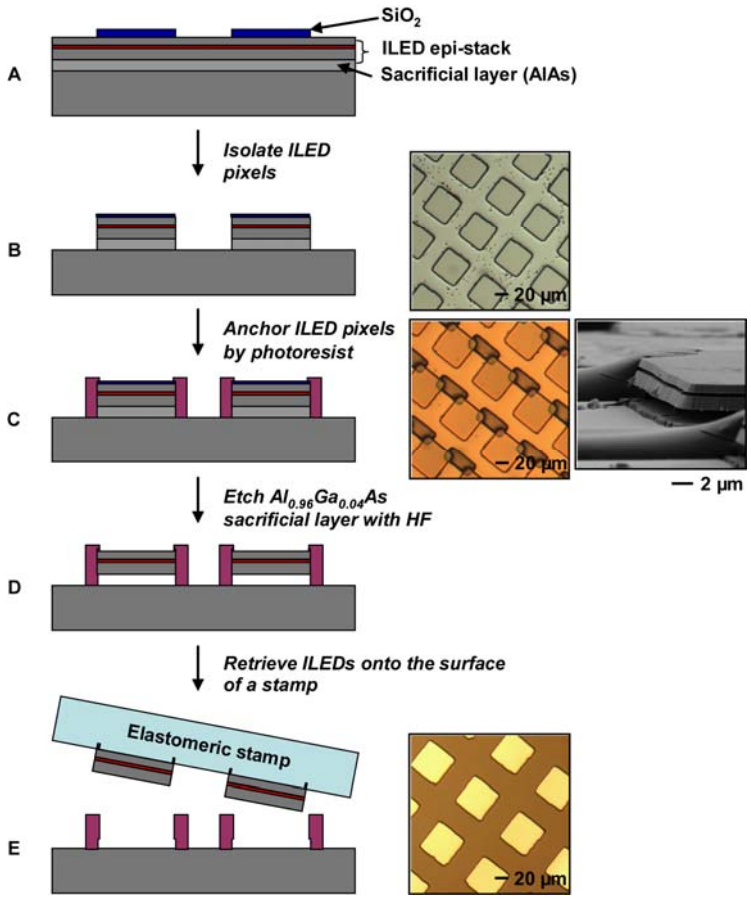


Figure S2. Schematic illustration and optical microscope/SEM images of processing steps for retrieving ILEDs from a GaAs source wafer.

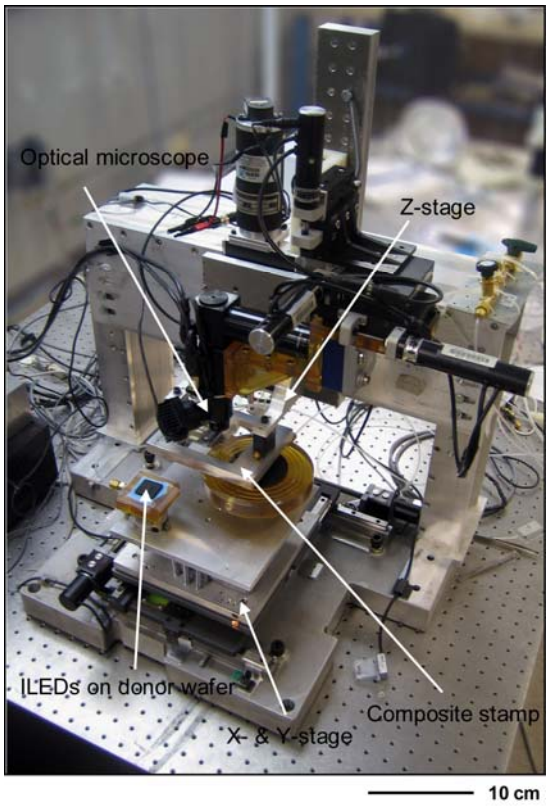


Figure S3. Picture of the automated printing machine, with key parts labeled

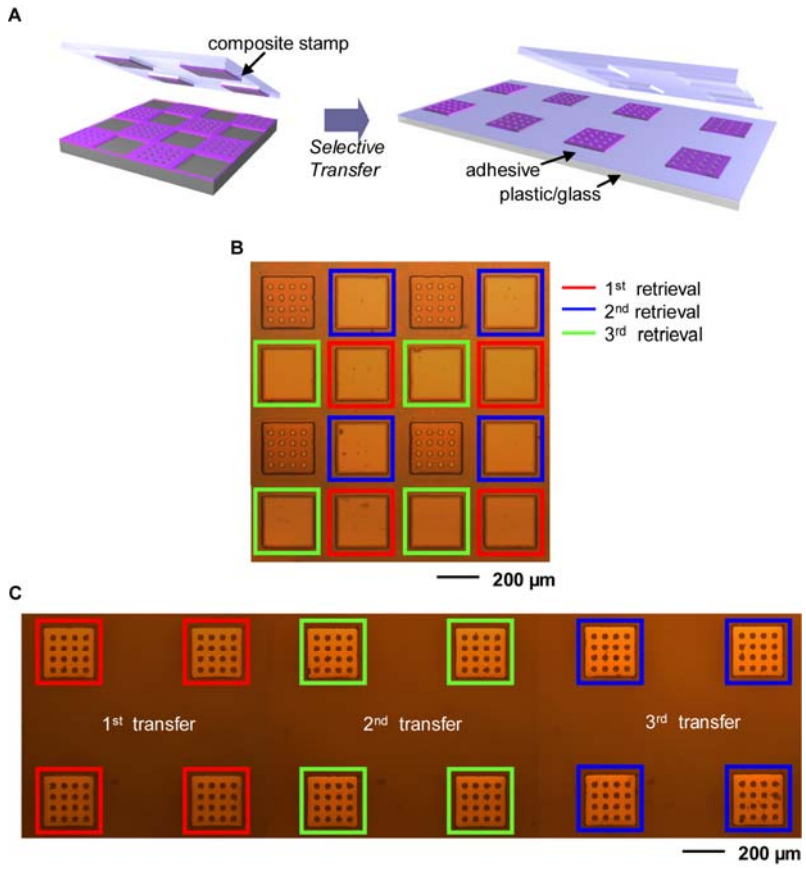


Figure S4. (A) Schematic illustration of retrieving and printing selected sets of ILEDs with a composite stamp. (B) Optical microscope image of the source wafer after three cycles of printing. (C) Optical microscope image of a substrate with sparsely printed ILEDs derived from the source wafer of (B), illustrating the concept of area expansion.

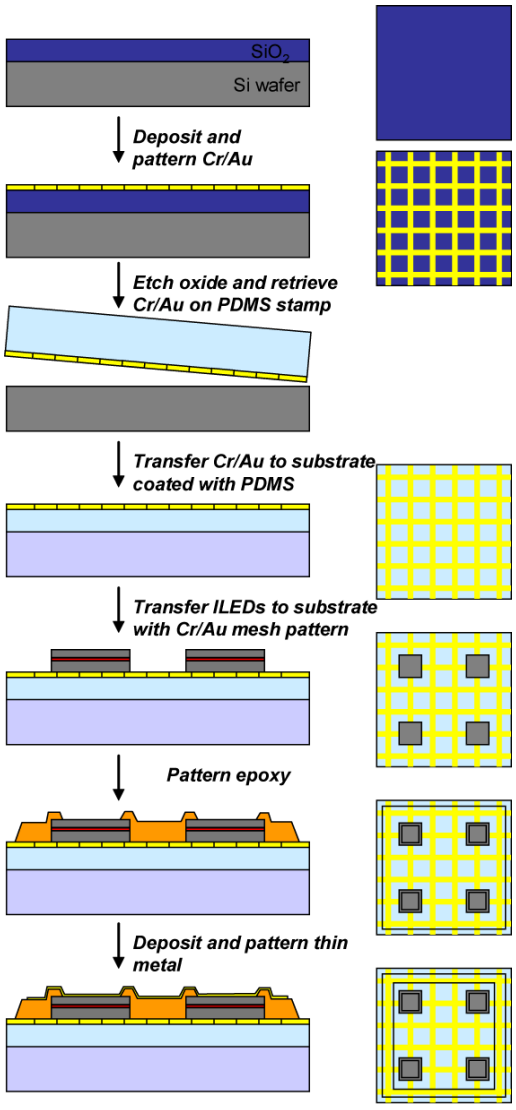


Figure S5. Schematic illustration of processing steps for ILEDs of Fig. 2A.

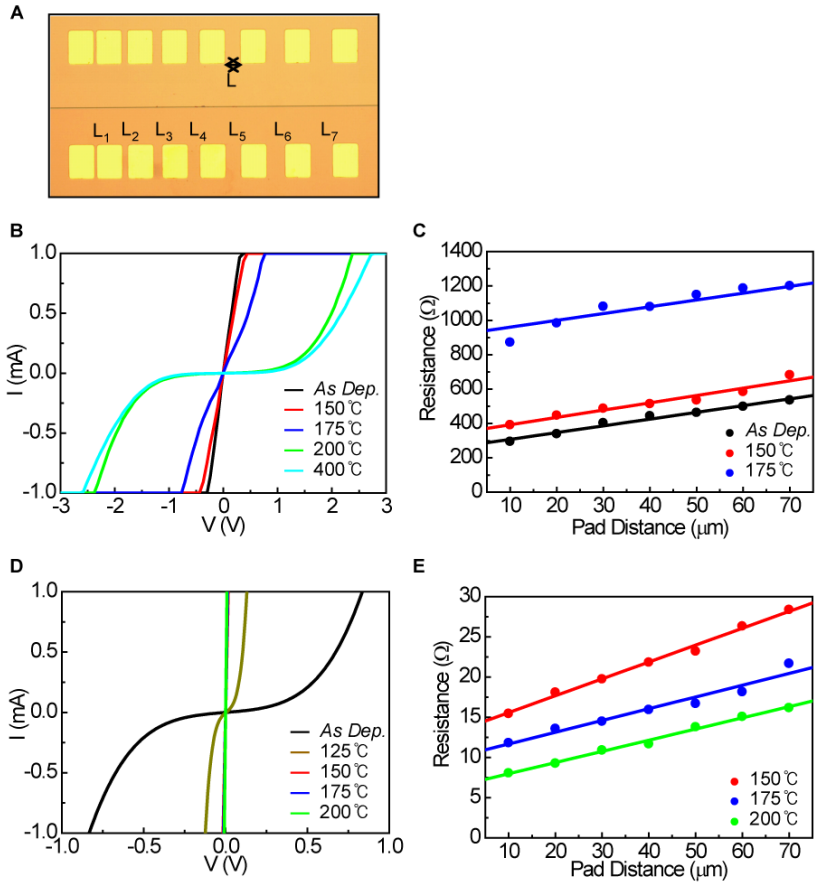


Figure S6. (A) Optical microscope image of transmission line model (TLM) patterns with gaps of L_1 = 10 μm, L_2 = 20 μm, L_3 = 30 μm, L_4 = 40 μm, L_5 = 50 μm, L_6 = 60 μm, L_7 = 70 μm. (B) I (current) – V (voltage) curves associated with p contacts (Pt/Ti/Pt/Au = 10/40/10/70 nm) as a function of annealing temperature. (C) Resistance as a function of gap length, for the p contact metallization, evaluated at different annealing temperatures. (D) I-V curves associated with n contacts (Pd/Ge/Au = 5/35/70 nm) as a function of annealing temperature. (E) Resistance as a function of gap length, for the n contact metallization, evaluated at different annealing temperatures.

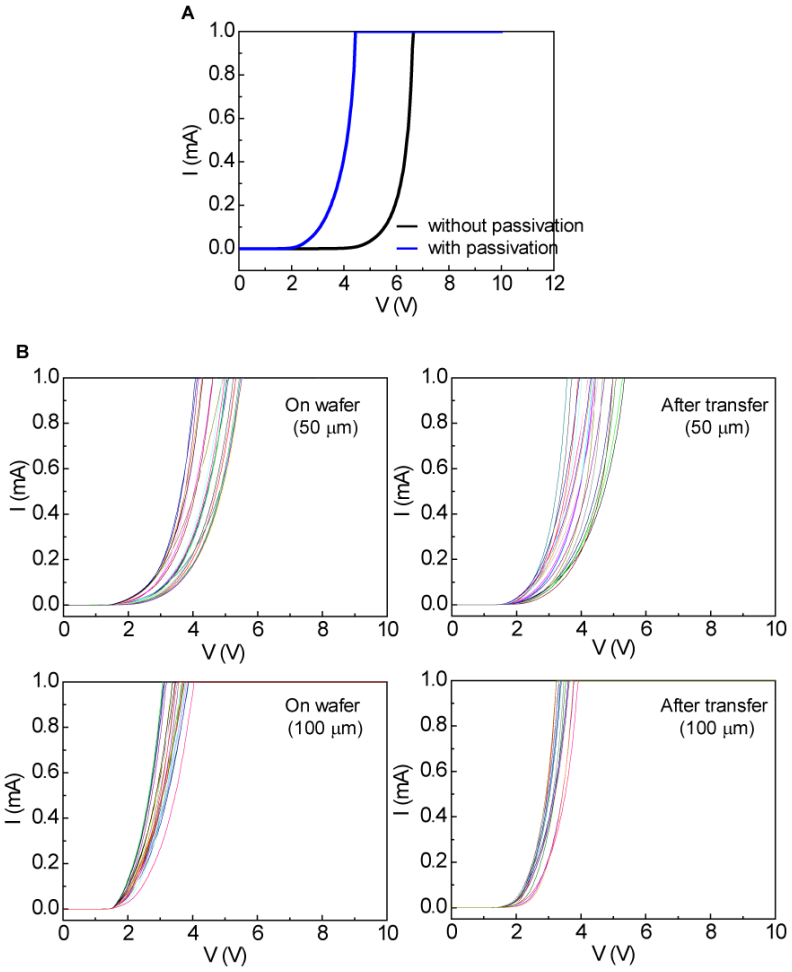


Figure S7. (A) I-V curves of ILED devices with ohmic contacts with and without a passivation scheme to protect the sidewalls during undercut etching. (B) I-V curves of ILED devices (50x50 μm and 100x100 μm) with ohmic contacts and passivation scheme, before and after transfer.

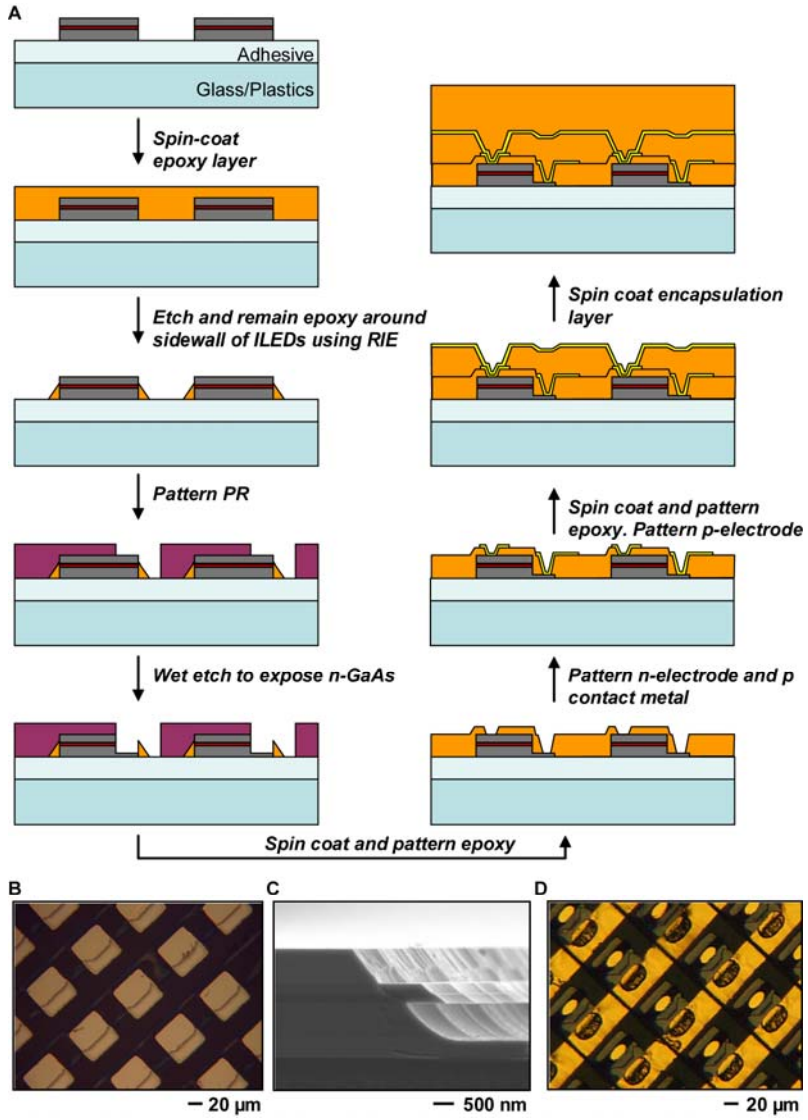


Figure S8. (A) Schematic illustration of processing steps for fabricating electrical interconnections to complete a passive matrix array. (B) Optical microscope image of an array of ILEDs array after exposing n-GaAs by wet etching. (C) Cross sectional SEM view of an ILED after exposing n-GaAs by wet etching. (D) Optical microscope image of an array of ILEDs with electrical interconnections.

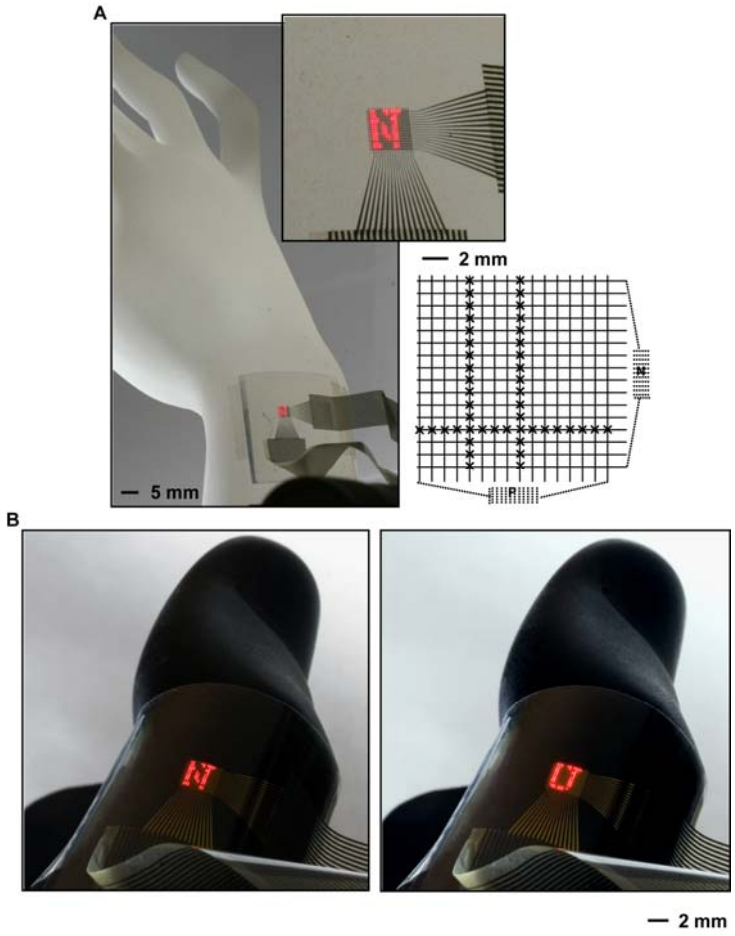


Figure S9. Optical images of a 16x16 ILED (100 μm x 100 μm with a pitch of 210 μm) display on a plastic substrate, wrapped onto the wrist (A) and finger (B, C) of mannequin. (Bottom right) a map of non-working pixels (indicated by 'x' symbols).

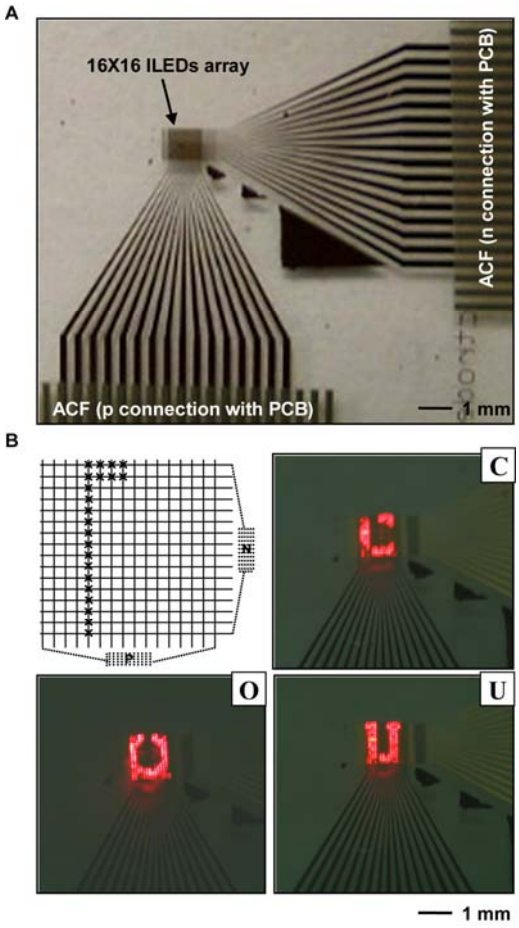


Figure S10. (A) Optical image of a 16x16 ILED (50 μm x 50 μm with a pitch of 70 μm) display on a glass substrate with ACF ribbon cable connection. (B) Optical images of the display during the operation. (Left-top) a map of non-working pixels (indicated by 'x' symbols).

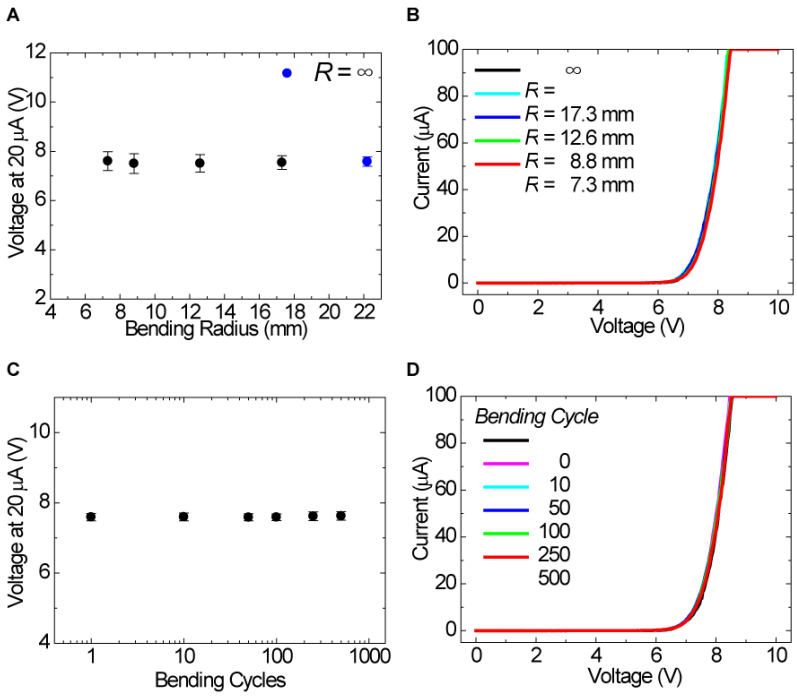


Figure S11. Electrical properties of a 16x16 ILED (100 μm x 100 μm with a pitch of 210 μm) display on a plastic substrate. (A) Plot of voltage at 20 μA and (B) I-V curves under $R = \infty$, 17.3, 12.6, 8.8, 7.3 mm. (C) Plot of voltage at 20 μA and (D) I-V curves as a function of bending cycles up to 500 times at R = 8.8 mm. The relatively high turn-on voltages are due to the use of non-ohmic contacts.

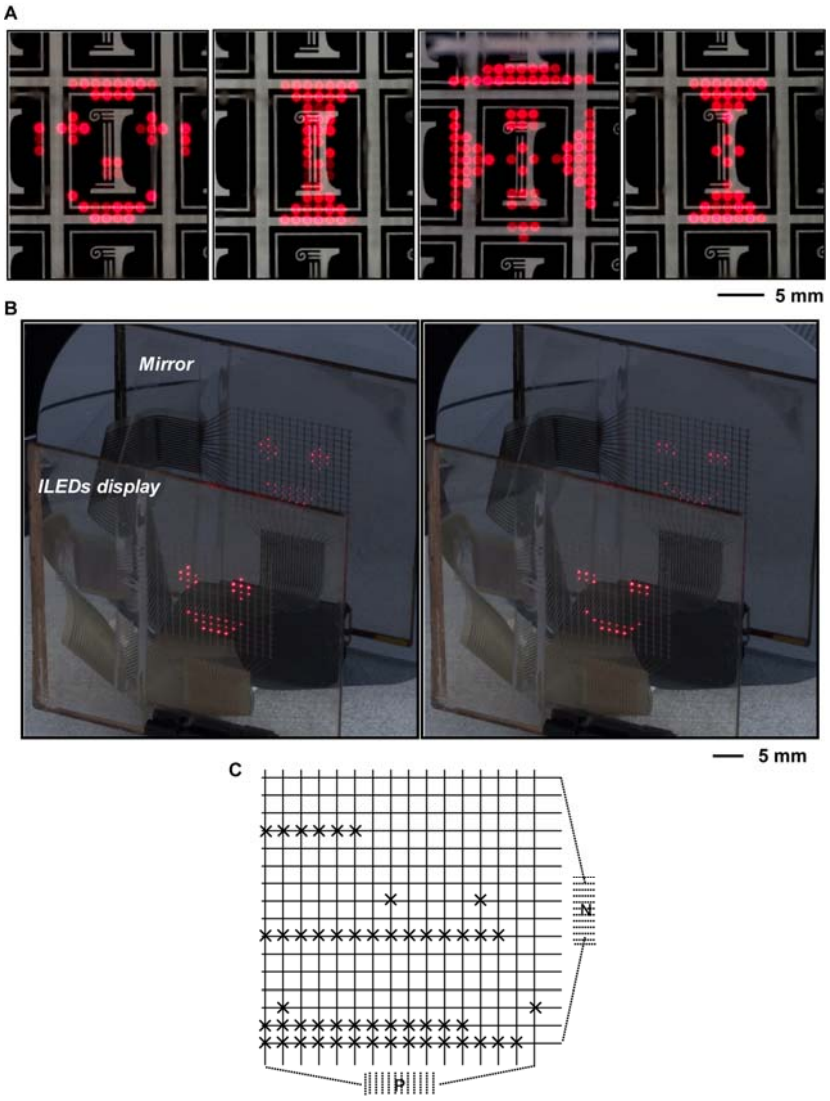


Figure S12. (A, B) Optical images of a 16x16 ILED (100 μm x 100 μm with a pitch of 1.20 mm) display on glass substrate during operation. (C) A map of non-working pixels (indicated by 'x' symbols).

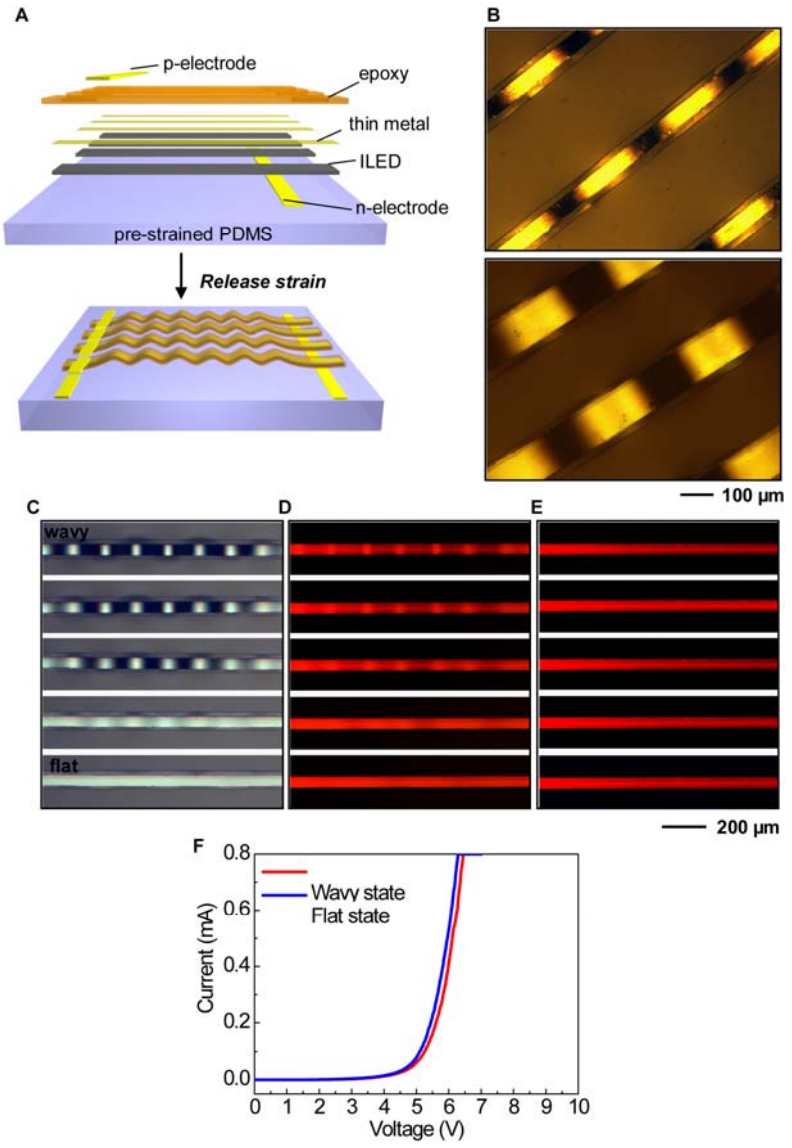


Figure S13. (A) Exploded schematic illustration of processing steps for wavy ILEDs ribbons. (B) Optical microscope image of wavy ILEDs ribbons with 50 μm and 100 μm width collected with a scanning focal technique. Optical microscope image of a wavy ILEDs ribbon in different strained states (from wavy to flat): (C) non-emission with illumination, (D) emission with illumination, (E) emission without illumination. (F) I-V curves under different strained states. The relatively high turn-on voltages are due to the use of non-ohmic contacts.

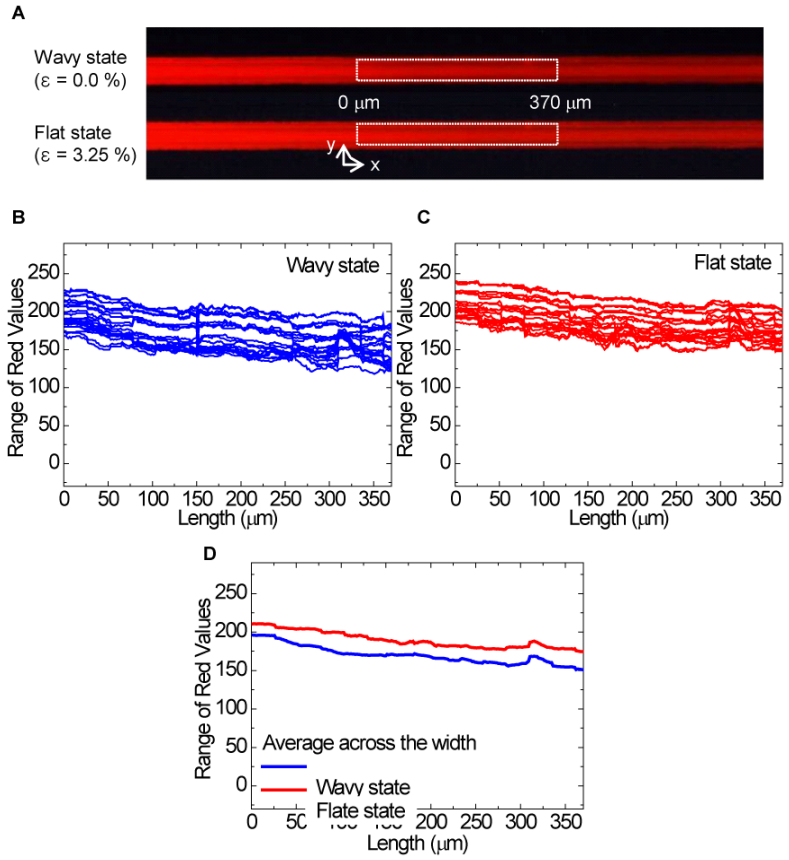


Figure S14. (A) Optical microscope images of emission, collected without illumination, from wavy ILEDs ribbons in wavy (top) and flat (bottom) configurations. Color analysis of pixels recorded in white square box of (A) using a utilities available in a commercial software package (Photoshop, Adobe Systems): range of red values of emission from (B) the wavy and (C) flat configurations, as a function of position along the ribbon length (0 = white, 255 = full red). (D) Averaged range of red values of emission across the ribbon width from (B) and (C).

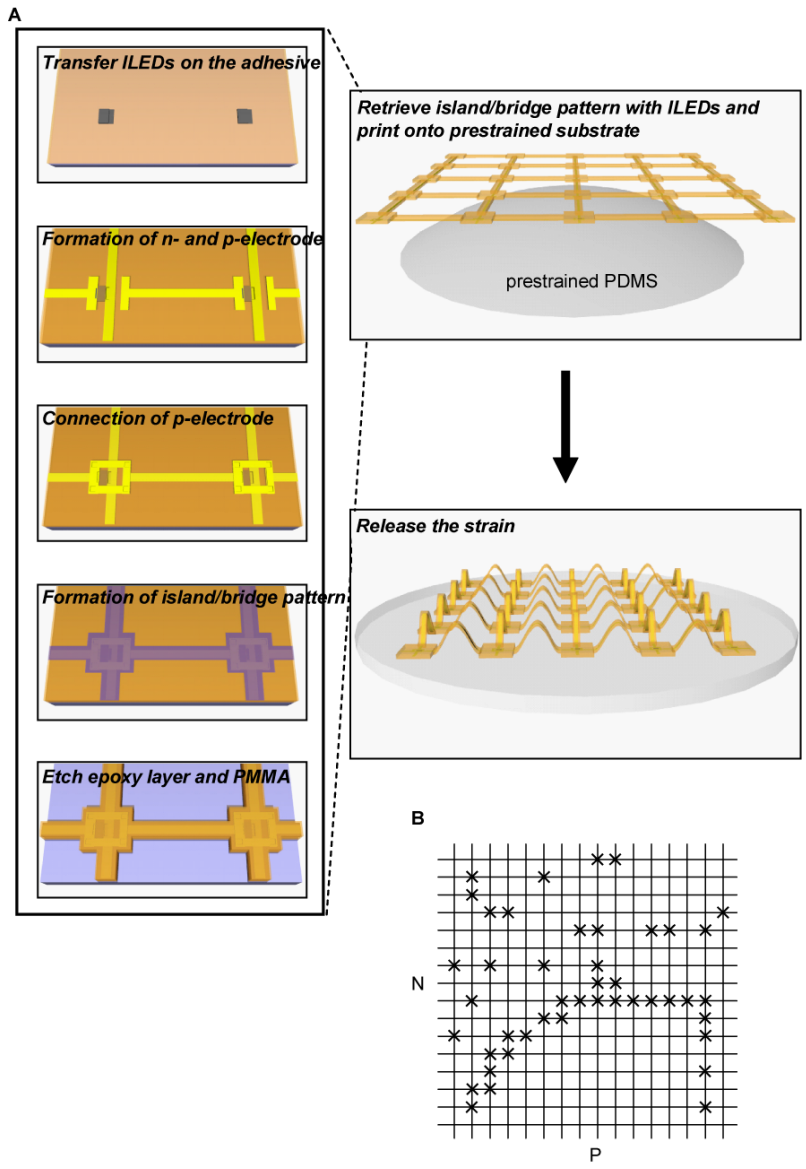


Figure S15. (A) Schematic illustration of processing steps for stretchable ILEDs display. (B) A map of non-working pixels (indicated by 'x' symbols).

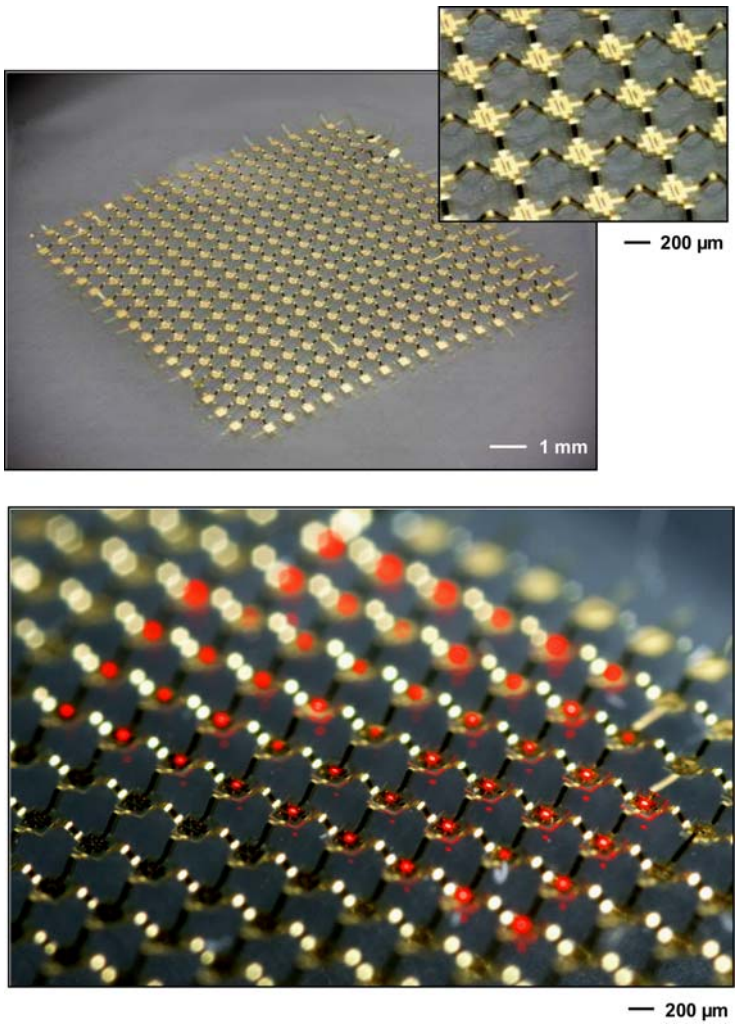


Figure S16. Optical microscope images of a passive matrix, stretchable ILEDs display that uses a non-coplanar mesh configuration, on a flat rubber substrate.

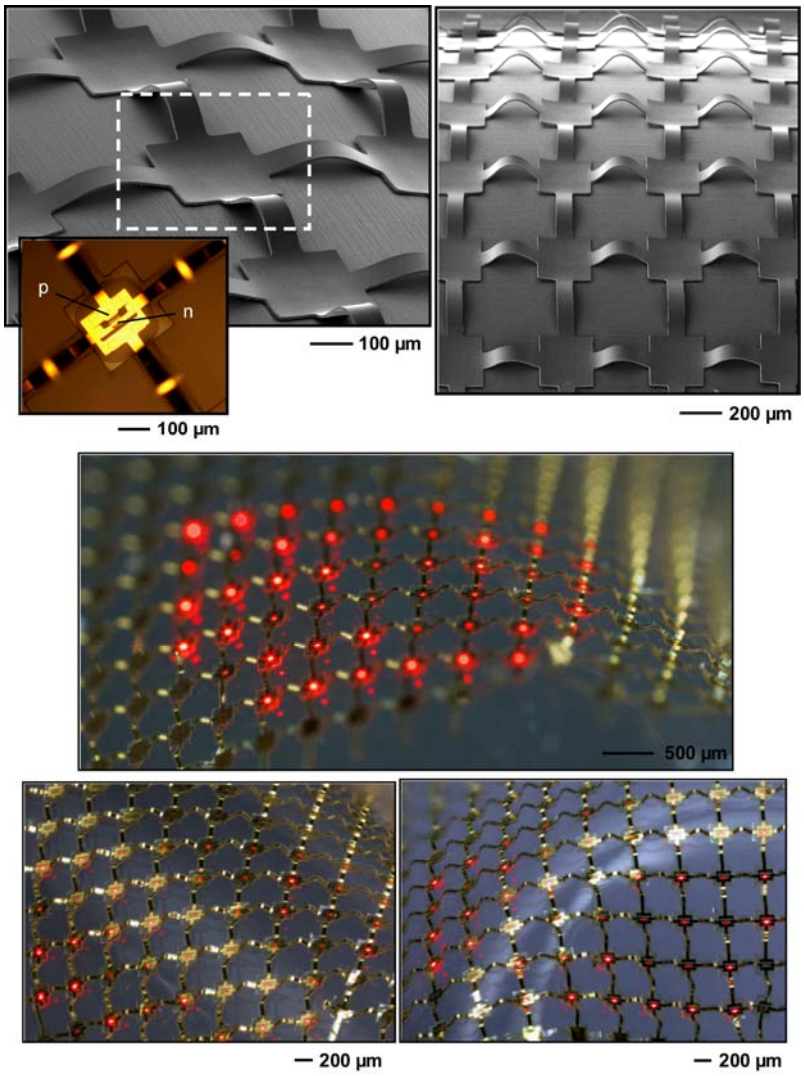


Figure S17. Optical microscope and SEM images of a passive matrix, stretchable ILEDs display that uses a non-coplanar mesh configuration, on a bent/twisted rubber substrate.

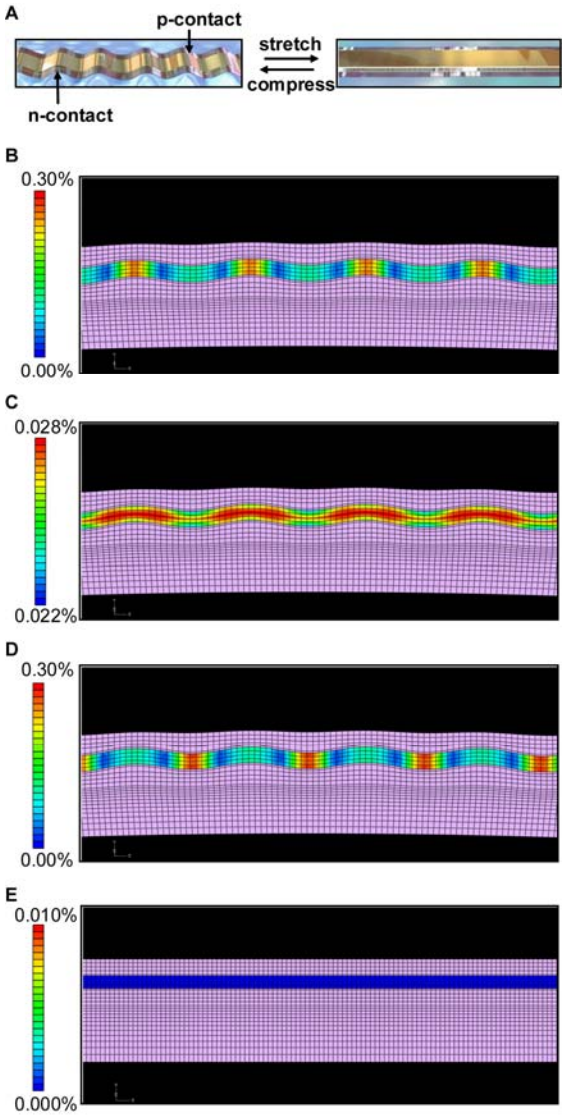


Figure S18. (A) Schematic illustrations of a stretchable ILED on a rubber substrate in compressed (left) and stretched (right) configurations. Strain distributions in the device: (B) top surface, (C) middle surface (quantum well region), (D) bottom surface in a compressed state and (E) middle surface in a stretched state.

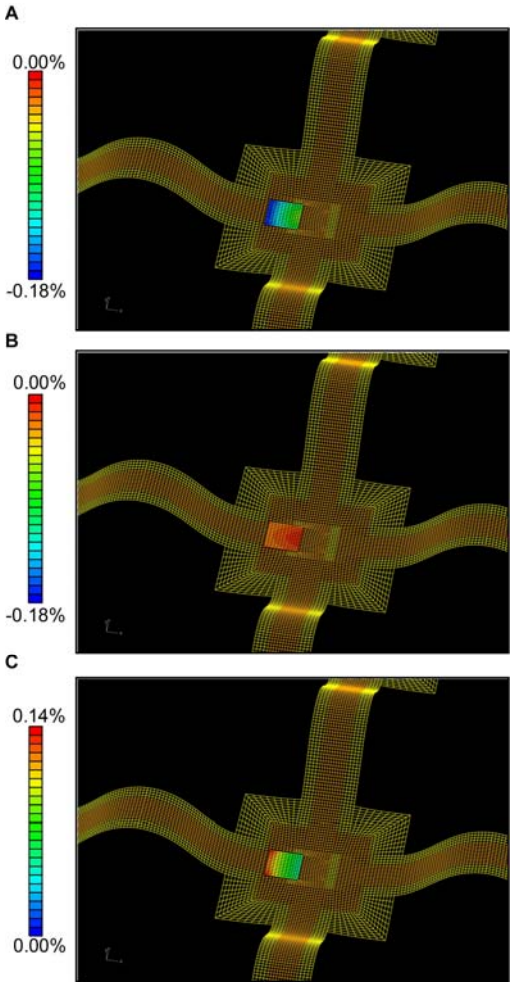


Figure S19. Strain distributions of a stretchable ILED display: (A) top surface, (B) middle surface (quantum well region), and (C) bottom surface of ILED.

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