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Review Article

Random Networks and Aligned Arrays of Single-Walled Carbon Nanotubes for Electronic Device Applications

Qing Cao[1] and John A. Rogers[1–6] (✉)

[1] Department of Chemistry, [2] Department of Materials Science and Engineering, [3] Department of Electrical and Computer Engineering, [4] Department of Mechanical Science and Engineering, [5] Frederick-Seitz Materials Research Laboratory, [6] Beckman Institute for Advanced Science and Technology, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, USA.

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ABSTRACT

Singled-walled carbon nanotubes (SWNTs), in the form of ultrathin films of random networks, aligned arrays, or anything in between, provide an unusual type of electronic material that can be integrated into circuits in a conventional, scalable fashion. The electrical, mechanical, and optical properties of such films can, in certain cases, approach the remarkable characteristics of the individual SWNTs, thereby making them attractive for applications in electronics, sensors, and other systems. This review discusses the synthesis and assembly of SWNTs into thin film architectures of various types and provides examples of their use in digital electronic circuits with levels of integration approaching 100 transistors and in analog radio frequency (RF) systems with operating frequencies up to several gigahertz, including transistor radios in which SWNT transistors provide all of the active functionality. The results represent important steps in the development of an SWNT-based electronics technology that could find utility in areas such as flexible electronics, RF analog devices and others that might complement the capabilities of established systems.

KEYWORDS

Carbon nanotubes, electronic devices, thin-film transistors

Introduction

Single-walled carbon nanotubes (SWNTs) have attracted substantial attention in the last decade due to their nanometer size, unique quasi one-dimensional (1-D) structure and excellent electrical, mechanical, optical, chemical, and thermal properties [1, 2]. Their exceptionally high mobilities and ballistic transport at room temperature [3] suggest the potential to outperform established inorganic materials for certain applications in unusual or advanced electronics systems. In addition, SWNTs demonstrate exceptional mechanical properties with reported fracture strains up to 30% [4], which is much better than that of other known organic and inorganic semiconductor materials. As a result, SWNTs are particularly suitable for certain applications with demanding mechanical requirements, e.g., flexible and/or conformal electronic systems. The main challenges in developing a technology based on devices that each incorporates an individual SWNT are to overcome (1) the electrical heterogeneity of

Address correspondence to jrogers@uiuc.edu

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as-synthesized SWNTs, in which the properties depend on the structure and diameter [5], (2) the high impedances and low current outputs associated with single SWNTs, and (3) difficulties in directed assembly of each SWNT, as required for deterministic integration into circuits. One means to solve these challenges involves the use of effective thin films consisting of large numbers of SWNTs in the form of random networks, aligned arrays or anything in between. In contrast to the more widely explored single tube strategies, here each device incorporates thousands or tens of thousands of SWNTs. Such an approach might represent a viable route to a technology due to (1) statistics that minimize the device-level effects of electronic heterogeneity in the SWNTs, (2) large active areas and high current outputs provided by the large numbers of SWNTs in each device, and (3) relaxed requirements of precise spatial position or orientation of any individual tube in the film [6, 7]. This article reviews our recent work in this area, starting with materials aspects of synthesizing the films, followed by the properties of individual devices formed with them and concluding with the types of circuits and systems that have been achieved.

1. Preparation of SWNT thin films

The preparation of SWNT thin films with controlled topologies, including nanotube alignment direction, length, and density (D, as measured by the number of tubes per unit area for random network films or tubes per length for aligned arrays) is critical for their successful application as electronic materials, as experimental and theoretical studies show that these parameters determine the collective electrical, optical, and mechanical properties [8, 9]. There are two approaches to assembling thin films of SWNTs. The first involves depositing SWNTs from their solution suspensions onto solid substrates utilizing, for example, specific interactions between SWNTs and functionalized surfaces [10, 11]. The second approach uses chemical vapor deposition (CVD) to grow SWNT thin films directly and, if necessary, dry transfer to another substrate. The solution deposition process has the potential for low cost and is compatible with a variety of substrates due to its open air, room temperature operation. A major disadvantage is that the solubilization procedures often require steps, such as high power ultrasonication and strong acid treatment, that can degrade the electrical properties and reduce the average tube length. The CVD method leads to SWNTs with fewer structural imperfections and longer average tube lengths than the solution process; both features lead to improved electrical properties of the associated films. More importantly, CVD enables extremely good control over various topological parameters, to an extent that is unlikely to be possible by solution deposition. This section discusses the controlled synthesis of SWNT films by CVD. Information on solution deposition processes can be found in a recent review [12].

With CVD, D can be controlled by the catalyst species, feed gas, catalyst concentration, duration of growth and so on. For example, random network SWNT films with D as high as several hundred tubes/μm^2 (Fig. 1(a)) can be synthesized by the combined use of ethanol feed gas [13], and Fe/Co/Mo tri-metallic catalyst loaded on silica nanoparticle supports [14, 15]. At high D, the metallic SWNTs (m-SWNTs), which typically represent 1/3 of the SWNTs produced in such a process, are fully interconnected as a percolating network. Such films serve as conducting layers, and are often referred to as metallic carbon nanotube networks (m-CNNs). These m-CNNs can, for example, serve as transparent conductors due to their high transmittance in the visible region and their low sheet resistance [16, 17]. By contrast, with Fe catalysts and methane as the feed gas, SWNT films with moderate to low D can be synthesized (Fig. 1(b)). Films of this type behave collectively as semiconducting networks (s-CNNs) because D is sufficiently high only to allow percolation transport through pathways that involve at least one semiconducting SWNT (s-SWNT). These s-CNNs can be used as semiconductors in active electronic devices, best positioned perhaps to compete with amorphous silicon for display applications or organic semiconductors for flexible electronics particularly for applications with demanding requirements on mechanical robustness and compatibility with harsh environmental conditions.

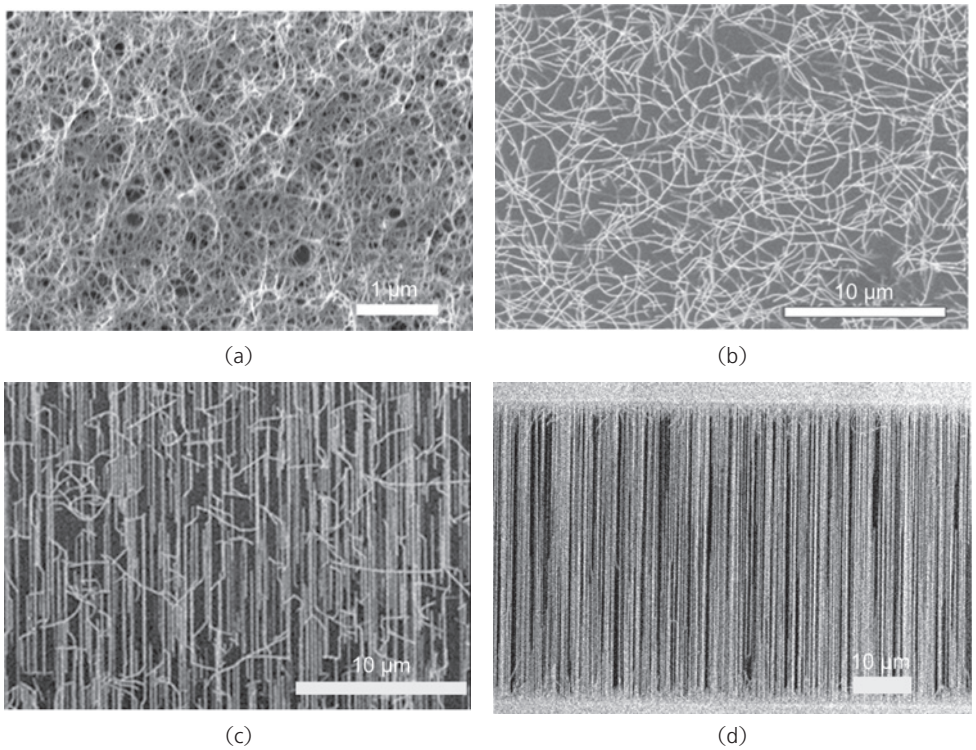


Figure 1 SEM images of SWNT thin films grown by CVD: (a) high *D* SWNT film grown with ethanol as the feed gas, and Fe/Co/Mo catalysts on silica supports; (b) moderate *D* SWNT film grown with methane as feed gas and Fe nanoparticle catalyst; (c) partially aligned SWNT film grown on single-crystalline ST-cut quartz substrate; (d) perfectly aligned SWNT arrays grown with Fe catalyst patterned into 10 μm wide strips (bright horizontal lines at top/bottom edges of the image) on a similar quartz substrate

In addition to *D*, control of alignment of the SWNTs is important because SWNT-SWNT junctions can limit effective electron transport in SWNT thin films. For example, at SWNT-SWNT junctions, a crossing m-SWNT can electrostatically shield, at least partly, the s-SWNT from the gate field, thereby frustrating switching. Also, experimental and theoretical studies suggest that contact barriers at these junctions can impede transport [18, 19]. Well-aligned SWNT arrays can take full advantage of the excellent intrinsic electrical properties of SWNTs, as demonstrated by measurements performed on individual nanotubes. We recently reported schemes for alignment that involve orientationally anisotropic interaction energies between SWNTs and certain single crystalline substrates such as quartz [20]. The degree of alignment depends on the surface quality, and can be controlled via growth parameters such as annealing time and catalyst density to obtain partially aligned arrays as shown in Fig. 1(c). The maximum degree of alignment and linearity in the shape of the SWNTs occur when the catalyst is patterned into small areas, such that the tubes grow primarily in regions of the substrate that are uncontaminated by catalyst (Fig. 1(d)) [21]. In these cases, SWNTs can be grown, in a wafer scale fashion, with linearity to within ~5 nm over lengths of many microns, and with deviations from parallelism of less than 0.1 degree. The *D* in such "perfectly" aligned arrays is typically 2–5 tubes/μm^2 but can reach peak values of 25–50 tubes/μm^2 in certain areas [22, 23]. These types of SWNT configurations are most suitable for applications that have demanding performance requirements (e.g., analog radio frequency (RF), where the competition is with compound inorganic semiconductors), where high *D*, linear configurations and a complete absence of SWNT–SWNT overlap junctions are paramount.

A major drawback of CVD, in its most widely reported form, is the requirement for high temperatures, generally above 600 °C [24]. These conditions preclude the use of substrates with low melting temperatures, e.g., plastic sheets for mechanically flexible electronics. Several methods exist for transferring SWNTs from their growth substrate to other surfaces, to avoid this limitation [25, 26]. In this approach, the transfer separates the high-temperature CVD synthesis from materials that would otherwise degrade under the growth conditions.

2. Transistors that use SWNT thin-film semiconductors

Transistors are the building blocks for all modern

electronic systems. Typical layouts for SWNT thin-film transistors (TFTs) are illustrated in Fig. 2. The current that flows between source/drain (S/D) electrodes is controlled by a voltage applied to a gate electrode that is separated from the SWNTs by a dielectric layer. The SWNT thin film can be grown or printed onto a substrate with a predefined gate electrode and dielectric to form a bottom gate device (Fig. 2(a)). This layout is easy to fabricate and is widely used for evaluating properties of SWNT TFTs, although it has certain disadvantages for circuit integration. Gate dielectrics and electrodes deposited on top of SWNT thin films yield top gate devices that are suitable for integrated circuits (ICs) with complex device-to-device interconnects (Fig. 2(b)). This layout is adopted for circuit/system demonstrations of integrated SWNT TFTs discussed in Section 4, and it is also used for devices built with aligned arrays on quartz substrates. In both top and bottom gate designs, the best performance, as measured by transconductance, operating voltage, and hysteresis,

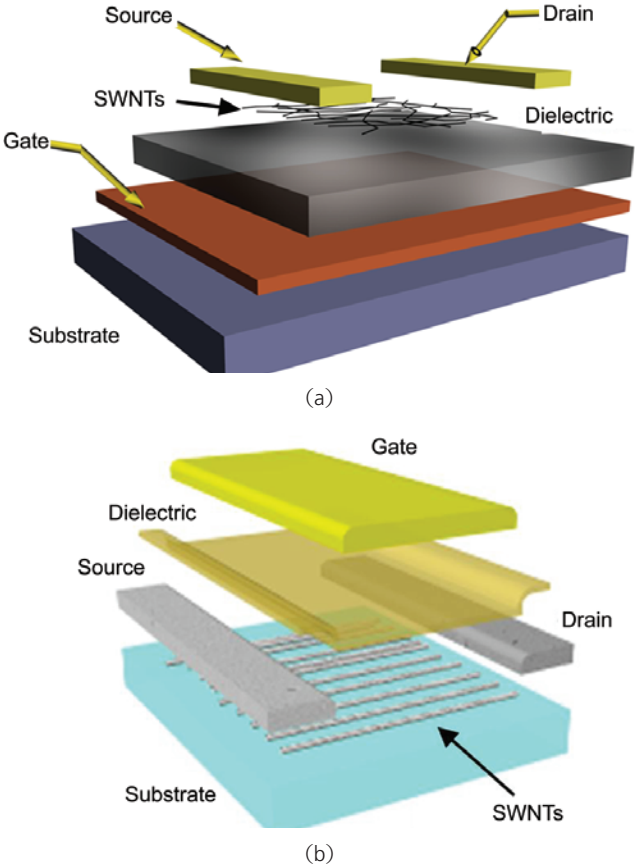


Figure 2 Schematic illustration of layouts for bottom-gate (a) and top-gate (b) SWNT TFT devices

is achieved with high capacitance gate dielectrics, such as a few nanometer-thick metal oxides [27] or self-assembled organic multilayers [28]. Compared with silicon, SWNT films are more compatible with these novel dielectrics, and unusual substrates, due to the absence of dangling bonds [29].

2.1 SWNT TFTs based on random networks

Figure 3(a) shows transfer curves of TFTs built on s-CNN grown by CVD, and processed using conventional thin film photolithographic, etching and deposition procedures. These particular devices use a dielectric of 100 nm SiO_2 and Ti (2 nm)/Au (50 nm) for the S/D electrodes. As for corresponding single tube transistors, the operation is largely unipolar p-channel. Polymer doping and other approaches can yield ambipolar or unipolar n-channel operation [30], similar to the case of single tube devices [31]. The effective field effect mobility is in the range 40–80 $cm^2/(V{\cdot}s)$, as extracted using standard analyses applied to the linear response regime (i.e., voltage between the source and drain, $V_{SD} << V_{GS}$, the voltage applied to the gate), with rigorous models for the capacitance coupling to the gate. These values are significantly better than the most widely explored competing materials (i.e., organic semiconductors or amorphous Si) for envisioned applications in flexible electronics. Furthermore, the data in the inset of Fig. 3(a) indicate that the effective device mobility is almost independent of channel length (L_C), consistent with a negligible role for contact resistance in this range. More detailed analysis using standard transmission-line models involves determining the resistance of semiconducting pathways (R_{sem}) from the overall device resistance, by assuming that R_{sem} and R_{met} (the resistance associated with the metallic pathways, as determined from I_{off}) are connected in parallel. The components of R_{sem} that are dependent and independent of L_C correspond to the resistances associated with the channel and the contacts, respectively. The results reveal that the gate voltage significantly modulates the conductance of the s-CNN, and that the contact resistance is negligible compared with the channel resistance for L_C larger than ~2 μm, for most cases of well designed devices [30]. This behavior is notably different from the

scaling behavior of devices based on aligned arrays, as discussed in the next section.

Due to the small and anisotropic optical absorption cross-sections of SWNTs and their relatively low surface coverages in the cases of interest here, SWNT films are transparent in the visible region, as mentioned previously [16]. Transparent electronic devices can therefore be constructed with this class of material [15, 32]. Figure 3(c) shows a schematic illustration of a flexible transparent TFT formed by sequentially transfer printing m-CNNs, as source/drain/gate electrodes, and s-CNNs, as semiconducting channels, onto a transparent plastic substrate [15]. Devices with this design have transparency as large as 75% even in the most opaque S/D electrode regions, as shown in Fig. 3(d). The degree of transparency compares well with technologies that use inorganic oxides as the electronic material. The transistor properties, with effective mobilities of ~30 $cm^2/(V{\cdot}s)$, are also similar to those of typical amorphous semiconducting oxides, <20 $cm^2/(V{\cdot}s)$ [33]. The solution processability of the CNNs and their improved mechanical robustness compared to the comparatively brittle oxides might provide important advantages for applications in flexible display and other areas.

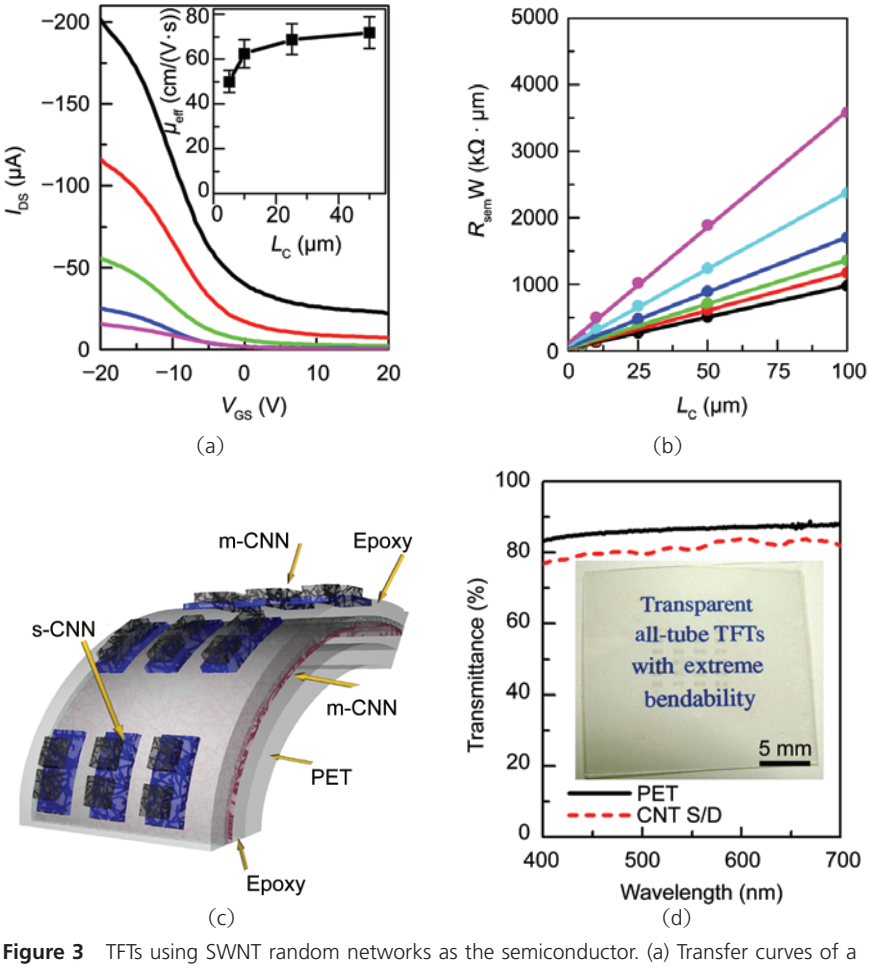


Figure 3 TFTs using SWNT random networks as the semiconductor. (a) Transfer curves of a series of devices (V_{GS}: gate-source voltage; I_{DS}: drain-source current; V_{DS}: drain-source voltage = −1 V). The L_Cs are 5 μm, 10 μm, 25 μm, 50 μm, and 100 μm, respectively, from the top to the bottom. Inset: effective device mobility (μ_{eff}) as a function of L_C. (b) Width-normalized resistance of the semiconducting responses of TFTs ($R_{sem}W$) based on SWNT random networks as a function of L_C at different V_{GS} (V_{GS} changes from −6 V to −16 V in steps of 2 V from top to bottom.). The solid lines represent linear fits. (c) Schematic illustration of the device layout and optical transmittance (d) of an "all-tube" transparent TFT in which metallic carbon nanotube networks (m-CNNs) serve as the electrodes and semiconducting carbon nanotube networks (s-CNNs) serve as the semiconductor. Inset: An array of transparent SWNT TFTs on a transparent plastic substrate (PET), resting on top of a piece of paper with printed text. The dashed red line corresponds to transmission through the source/drain (S/D) region of the device. Reproduced with permission from [15]. Copyright 2006 Wiley-VCH

The presence of m-SWNTs in an s-CNN can represent a challenge to their use as the semiconducting layer in a transistor. At high D, where the effective mobility tends to be highest, these m-SWNTs can form all-metallic conduction pathways from source to drain, thereby electrically shorting the device. Various purification schemes, such as electrical breakdown [34], ultracentrifugation [35], selective plasma etching [36], and selective chemical functionalization [37, 38] can yield s-CNNs with content of s-SWNTs enriched compared to the expected 2/3 population. As these methods continue to develop, they could become suitable for the types of applications contemplated here [39]. A completely different strategy to eliminate the purely metallic pathways through the s-CNN involves "engineering" the layout of the as-synthesized (or deposited) s-CNN via lithographic patterning and etching procedures.

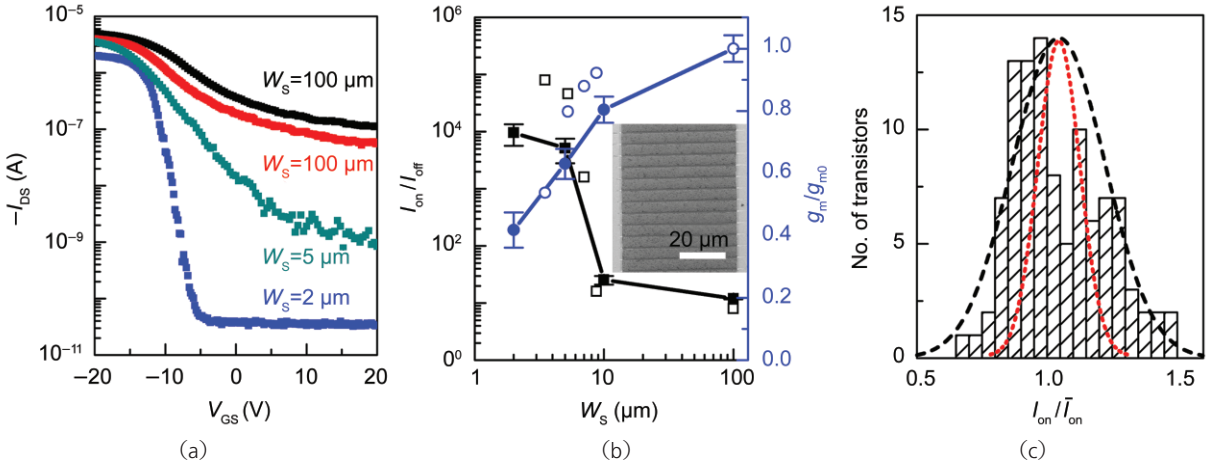


Figure 4 "Striping" scheme to enhance on/off ratio of TFTs based s-CNNs: (a) Transfer characteristics of TFTs with L_C of 100 μm, channel width (W) of 100 μm, and strip widths (W_S) of 100, 10, 5, 2 μm, from top to bottom, plotted on a semi-logarithmic scale (V_{DS}: −0.2 V). (b) Measured (filled) and simulated (open) on/off ratio (I_{on}/I_{off}) and normalized transconductance (g_m/g_{m0}, where "0" represents the state without strips) as a function of W_S for SWNT devices shown in (a). Inset: SEM image of the channel region of such a device. (c) Histogram of normalized $\bar{I}_{on}$ ($\bar{I}_{on}$: averaged on-state current) with superimposed Gaussian fitting of measured (dashed black) and simulated (dashed red) results. Reproduced with permission from [40]. Copyright 2008 Nature Publishing Group

For devices in which L_C is much larger than the average tube length, many SWNTs are involved in transport between S/D electrodes. Because there are more s-SWNTs than m-SWNTs and because only a single s-SWNT in a multitube transport pathway is needed to yield overall semiconducting behavior, it is possible to reduce significantly the possibility of metallic pathways by cutting narrow strips into the s-CNN oriented along the overall transport direction. These features can reduce drastically the probability of a purely metallic pathway, in a way that limits the lateral crosstalk between SWNTs but also maintains the conductance of most short semiconducting pathways (Fig. 4(b) inset) [40]. In this way, the ratio of the on to the off currents in the transistor (i.e., the on/off ratio) can be improved by orders of magnitude with only minor reductions in transconductance and slightly increased sensitivity of device parameters to D variations, when implemented in optimized geometries, as shown in Fig. 4(a). The effect of these strips on the electrical properties of the s-CNNs and associated devices can be quantified through first-principles percolative modeling, in which the network is represented as a collection of randomly positioned conductive wires with D and length corresponding to quantities measured by scanning electron microscopy (SEM) (Fig. 4(b)). This simple scheme provides "top down" control over the on/off ratio and effective mobility, even with unsorted, as-synthesized nanotube films, at a level that enables device yields and uniformities (Fig. 4(c)) suitable for ICs, as discussed subsequently. Theoretical modeling also provides a predictive framework for application in devices with various L_C, with selected combinations of strip widths (W_S), average tube lengths, and D [41].

2.2 SWNT TFTs based on aligned arrays

Compared with s-CNNs, aligned arrays provide dramatic improvements in device mobility, due to the long, straight geometries of the tubes and the absence of SWNT-SWNT junctions. In all cases with aligned array devices, L_C is much smaller than the average tube length such that each tube bridges the S/D electrodes directly [42, 43]. Figure 5(a) shows transfer curves of representative TFTs that use 1.5 μm thick epoxy dielectrics and Ti (1 nm)/Pd (20 nm) as S/D contacts. As with the s-CNN, p-channel operation is typically observed with high work function contact metals, with the possibility for ambipolar or n-channel behavior via the use of doping techniques. The effective device mobility, extracted at long L_C, is ~1000 $cm^2/(V \cdot s)$ when computed in the linear regime with a simple parallel-plate approximation for the capacitance coupling to the gate; this value is a ten-fold improvement over the mobility of similar

devices that use s-CNNs. The per tube mobilities, which we define as values that consider only the capacitance of the s-SWNTs [44], computed in a rigorous manner, can exceed 2000 $cm^2/(V{\cdot}s)$. This value is only somewhat lower than expectation based on measurements on devices that incorporate single SWNTs (~3000 $cm^2/(V{\cdot}s)$), for this range of diameters (Fig. 5(b)) [42]. Unlike s-CNN devices, the effective mobility decreases with L_C for aligned arrays, suggesting that the contact resistance can be a significant fraction of the overall resistance even for devices with L_C in the micron range, due mainly to the lowered channel resistances in this case compared to that of the random network devices. Scaling analysis, similar to that described for the network devices, shows that the gate voltage modulates mainly the channel and has comparably small influence on the contact resistance for devices with channel lengths in the micron range. Chemical doping techniques [45] or the use of certain metal carbides between the SWNT and S/D electrodes [46], as demonstrated in single tube devices, may help to reduce this contact resistance.

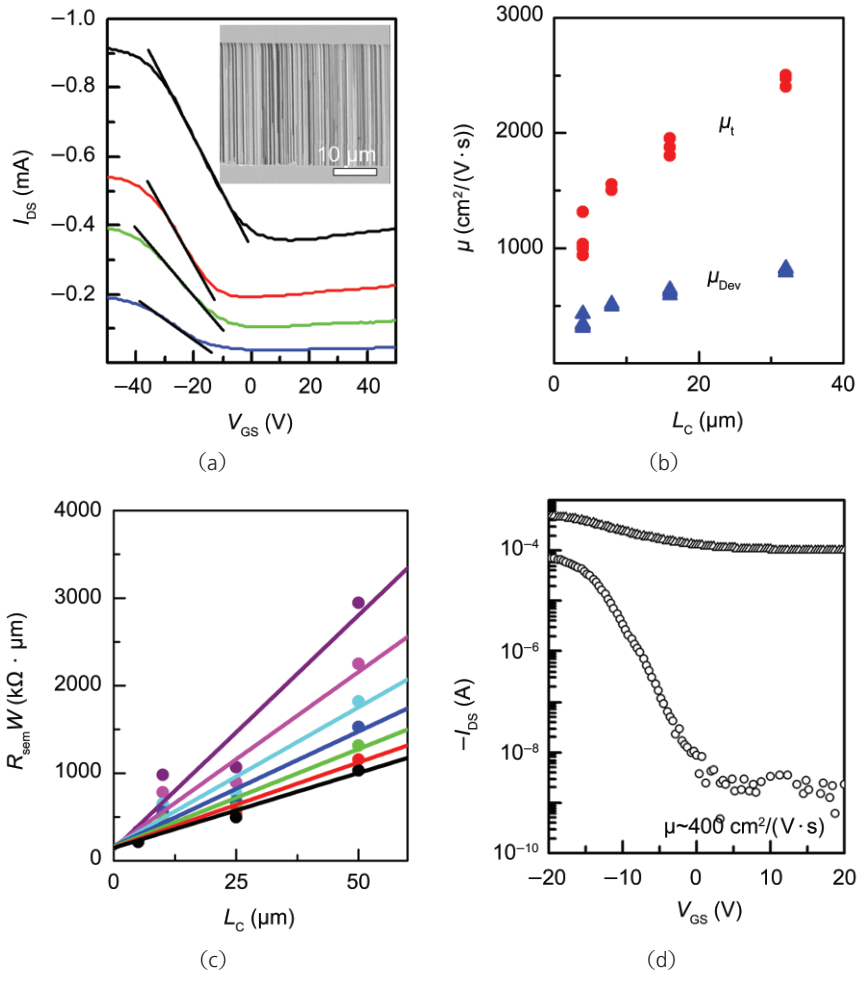


Figure 5 Characteristics of TFTs based on aligned arrays of SWNTs. (a) Transfer curves of a series of devices with W of 200 μm (V_{DS}: −0.5 V). L_Cs are 5, 10, 25, 50 μm, from top to bottom. The straight lines serve as visual guides to indicate the slopes used to extract the linear region g_m. Inset: SEM image of the channel region of such a device. (b) Mobilities (μ) calculated using a parallel plate model for capacitance (μ_{Dev}) and per-tube mobilities calculated using rigorous models for the capacitance coupling and only including the s-SWNTs (μ_t), both as a function of L_C. These calculations do not explicitly account for the effects of contacts. (c) Width-normalized resistance of the semiconducting responses of TFTs ($R_{sem}W$) based on aligned arrays of SWNTs as a function of L_C at different V_{GS} (V_{GS} changes from −20 V to −32 V in steps of 2 V from top to bottom.). The solid lines represent linear fits. Although all fitted lines show similar intercepts, this outcome is just a coincidence of the linear regression fitting process. The relative standard errors for the fitted intercepts are between 40% and 200%. (d) Transfer curves of similar devices with W of 200 μm and L_C of 12 μm before (triangles) and after (circles) electrical breakdown to improve the on/off ratio. Reproduced with permission from Ref. [42]. Copyright 2007 Nature Publishing Group

Compared to devices built on s-CNNs, especially with optimized strip structures, those based on aligned arrays have small on/off ratios (typically in a range between 2 and 5) even for long L_C and their on/off ratios cannot be increased with "striping" schemes because each SWNT directly bridges the S/D electrodes and 1/3 of them are m-SWNTs. Selective electrical breakdown can be used to increase the on/off ratio up to 10^5 (Fig. 5(d)) [42] In this process a large current is passed through the m-SWNTs while the p-channel s-SWNTs are adjusted to their off position by use of a positive applied gate voltage [34]. This precedule, which irreversibly eliminates transport pathways through metallic channels in the device, can also be applied to devices built on s-CNNs [6, 47], although the process tends to be more reproducible with the arrays, due perhaps to their relatively simple layouts.

3. High-frequency properties of SWNT TFTs

SWNTs exhibit room-temperature mobilities higher than those typical of single crystalline silicon, particularly when used in p-channel devices [5]. SWNTs also have low intrinsic capacitance and, unlike many other envisioned next-generation electronic materials and devices, they are compatible with standard metal oxide semiconductor field-effect transistor (MOSFET) structures [1]. Furthermore, recent work suggests the possibility of highly linear operation as high-frequency amplifiers [48]. These attributes suggest that SWNT arrays might eventually be competitive with silicon or III–V semiconductors in next-generation high-frequency devices, with the possibility for operation in the terahertz regime [49, 50]. Transistors that use aligned arrays have much lower device output impedance than single tube devices, thereby allowing evaluation of scattering parameters (*S*-parameters) directly with a network analyzer to determine their frequency response [51, 52]. Figure 6(a) shows current gain (H_{21}) and maximum available power gain (G_{max}), all derived from the S-parameters for an SWNT array device with L_C = 4 μm and a 50 nm thick high *k* gate dielectric [52]. The S/D electrode layouts match conventional signal-ground-signal microwave probes (Fig. 6(a), inset). These results indicate unity-current-gain frequency ft and unity-power gain frequency fmax of 2.5 GHz and 1.1 GHz, respectively. L_C scaling studies indicate that cutoff frequencies can be further increased following direct geometrical scaling routes (Fig. 6(b)). With further reduction of L_C to submicron regime, ca. L_C~700 nm, fmax can be as high as 10 GHz [53]. Such results, as obtained with devices that have relatively low *D*, ca. ~ 5 tubes/μm, and long L_C, ca. above 700 nm, suggest promise for achieving much higher speeds in optimized devices. In addition, the frequency behavior can be successfully reproduced by use of conventional small-signal models, with remarkably good agreement between measured and modeled results over two decades of frequency up to 50 GHz [53]. These outcomes suggest the suitability of established modeling tools to guide future device designs.

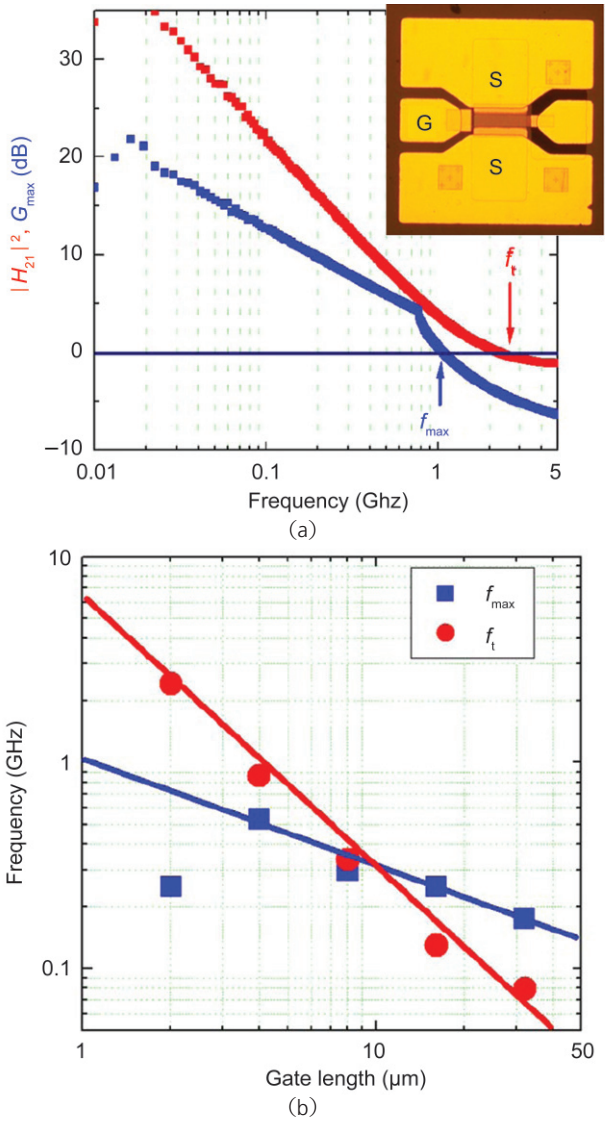


Figure 6 High-frequency properties of TFTs based on aligned arrays of SWNTs. (a) Current gain $|H_{21}|^2$ (squares) and maximum power gain (G_{max}) (triangles) determined from scattering parameter measurements as a function of frequency for a device with L_C of 4 μm. Inset: optical image of a device with signal-ground-signal layout for high frequency measurement. (b) Plot of cutoff frequency for current gain (f_t) and power gain (f_{max}) as function of L_C. Reproduced with permission from Ref. [52]. Copyright 2008 The National Academy of Sciences

4. Functional electronic systems composed of SWNT TFTs

Although substantial efforts have been made in recent years to understand the materials science and physics of SWNT TFTs and improve their performance, individual transistors are of little interest for applications. The next step is to interconnect these devices together to form functional systems [40, 54, 55]. In this section, we describe several demonstrations of digital and analog electronic circuits based on SWNT transistors.

4.1 Digital integrated circuits

Transistors based on s-CNNs engineered with optimized strips can provide on/off ratios and levels of uniformity sufficiently high to meet the requirements of functional digital ICs. Figure 7(a) shows a schematic layout of a p-MOS inverter, the fundamental building block for p-MOS digital circuits [40]. This inverter uses two TFTs built on an s-CNN transfer printed on a plastic substrate; the circuit diagram appears in Fig. 7(b). The top-gate structure of the devices allows separate access to each transistor and straightforward interconnection. This inverter exhibits a voltage gain of ~4, and its output transfer characteristics are consistent with simulation results obtained using empirical simulation program with integrated circuit emphasis (SPICE) models, proving the utility of this established computer aided design platform for the development of SWNT circuits. By the addition of another transistor to incorporate the OR function, a NOR circuit can be realized (Fig. 7(d)). The logic swing, defined as the voltage difference between logic "0" state and logic "1" state, is above 2.4 V, and agrees reasonably well with SPICE modeling results (Fig. 7(e)).

The ability to achieve IC building blocks composed of three TFTs opens the way to digital circuits of any size. Figure 8(a) shows an optical image of a chip featuring a four-bit decoder composed of 88 SWNT TFTs [40]. Input–output characteristics of this circuit show its ability to decipher a binary encoded input of four data bits into sixteen individual data output lines. A single output is enabled, depending on the correspondence of the encoded value to the data line number (Fig. 8(b)). This decoder can operate at frequencies of several kHz. Circuits with similar operating speeds based on organic transistors demand feature sizes more than 10 times smaller than those reported here (Fig. 8(b), inset) [56]. The ability of high mobility materials, such as s-CNN, to reduce the demands on feature size, and overlay registration, is important due to its implications for cost. Specifically, the demonstrator circuits described here were designed to use coarse critical dimensions in the transistors (e.g., ~100 μm), as a means to maintain compatibility

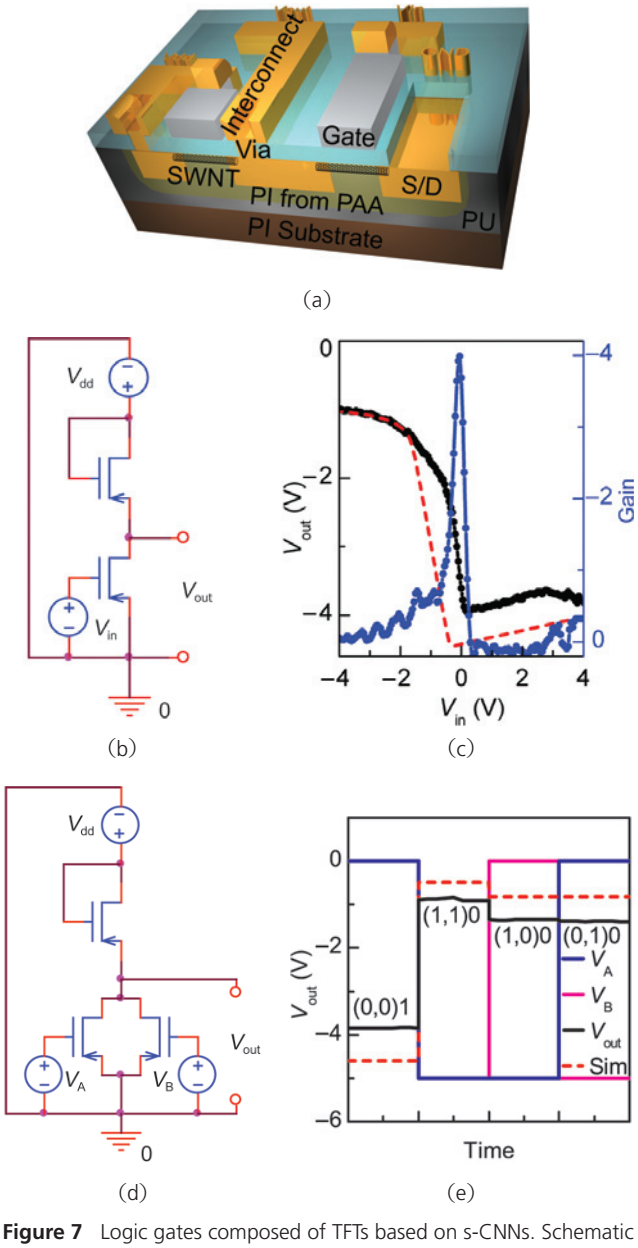
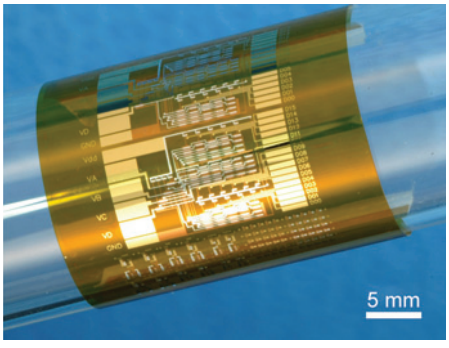
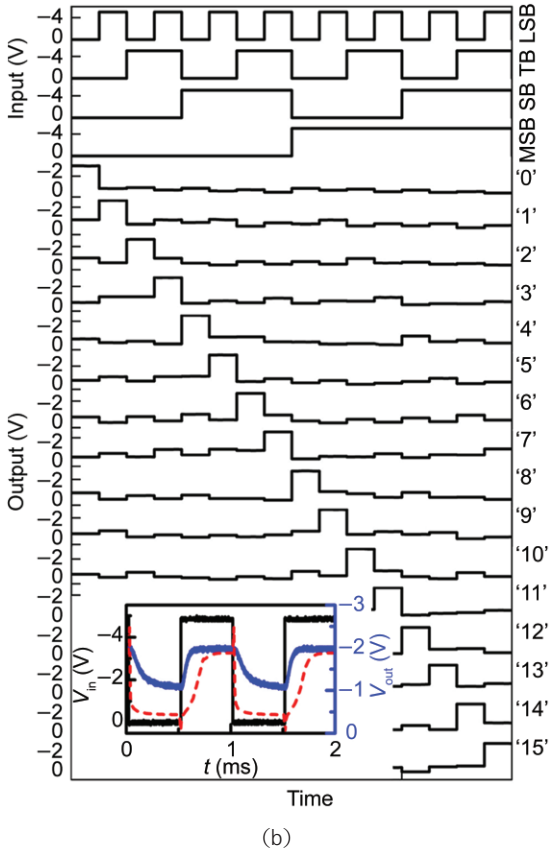


Figure 7 Logic gates composed of TFTs based on s-CNNs. Schematic view (a), circuit diagram (b), and static transfer characteristics (c) of an inverter composed of two p-channel TFTs on a polyimide (PI) substrate. PU: polyurethane; PAA: polyamic acid. Circuit diagram (d), and output–input characteristics (e) of a NOR gate composed of three TFTs. Logic "0" and "1" input signals of two terminals (V_A and V_B) of the NOR gate are driven by 0 V and 25 V, respectively. The logic "0" and "1" outputs are (0.88–1.39) V and –3.85 V, respectively. In (c) and (e), the dashed line represents circuit simulation results. Reproduced with permission from Ref. [40]. Copyright 2008 Nature Publishing Group

with commercial printing tools, e.g., screen printers, used in forming circuit boards [57, 58]. This attribute is important for the commercial success of this class of technology in flexible electronics, where low cost



(a)



(b)

Figure 8 Medium-scale IC based on TFTs that use s-CNNs, constructed on flexible polyimide (PI) substrate. (a) Optical image of a flexible circuit wrapped around a test tube. (b) Input-output characteristics of four-bit decoder composed of 88 TFTs. The first four traces are inputs and the remaining ones show the outputs of 16 terminals. Inset: Measured (blue) and simulated (red) dynamic response of one output terminal under a square-wave input pulse (black) at a clock frequency of 1 kHz. Reproduced with permission from Ref. [40]. Copyright 2008 Nature Publishing Group

manufacturing is generally believed to be critically important.

4.2 Analog radio frequency electronics

Analog circuits represent key components of communications and other systems in widespread, growing commercial use. High-speed transistors are central to the operation of such circuits. The modest levels of integration (e.g., hundreds of devices), and the relaxed requirements on on/off ratio and other aspects make this application area potentially well matched to the capabilities of SWNT array transistors. As mentioned in Section 3, RF transistors have been demonstrated at frequencies up to 10 GHz, with relatively coarse device dimensions. Connection to other components, e.g., inductors and resistors, yields radio frequency power amplifiers [52] and oscillators [59], two of the most important building blocks of analog electronic systems. As an example, these devices can be then connected and impedance matched to yield functional radio receiving systems, where the SWNT TFTs provide all of the active components including even the audio output amplifier stage, as shown in Fig. 9(a) [53]. An optical image of a completed SWNT radio is shown in the inset of Fig. 9(b). This relatively simple system, and others like it, is fully functional and capable of receiving, demodulating, and amplifying signals broadcasted by commercial radio stations. Figure 9(b) presents the power spectrum recorded during a weather/traffic report that is directly audible through headphones connected to the system.

5. Conclusions

Individual SWNTs provide an ideal platform to study the physics of 1-D quantum confined systems. Thin films of SWNTs represent a higher level of integration that provide equally interesting opportunities for research, but also a materials strategy that might yield realistic device applications. The exceptional electrical, mechanical, optical, chemical, and thermal properties of SWNT thin films make them especially attractive for novel multipurpose/multifunctional systems, where several of these unique properties combine to enable functionality that is difficult or impossible to achieve with established materials. Examples include transparent devices [17] and printable, flexible and/or large area electronics [60]. In the form of aligned arrays, such SWNT films may possibly be able to compete with conventional

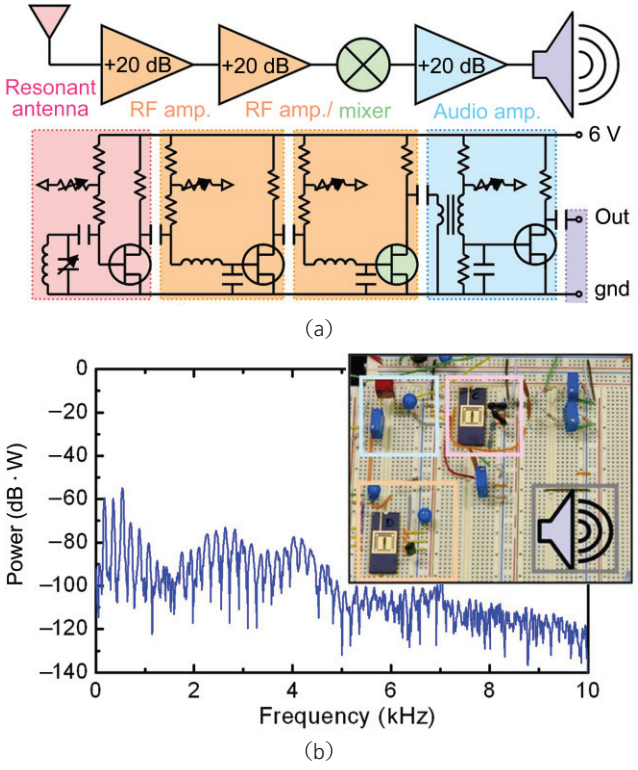


Figure 9 Analog radio system based on high frequency TFTs that use aligned arrays of SWNTs. (a) Block and circuit diagram of the radio system in which SWNT-based devices (6 in total) provide all of the active components. (b) Power spectrum of the radio output measured across an external speaker, for a commercial broadcast of a traffic report, showing a response characteristic of the human voice. Inset: Optical image of the completed radio system. Reproduced with permission from Ref. [52]. Copyright 2008 The National Academy of Sciences

materials in high-frequency electronics, or as high-frequency components of heterogeneously integrated systems [61]. The demonstrations reviewed here provide some examples in these two very different areas of potential application. In spite of recent progress, significant chemistry and materials science challenges remain. Prominent among these are methods to eliminate the m-SWNTs, controlled schemes to dope the s-SWNTs and strategies to improve various aspects of the growth and deposition. The success of this materials technology will depend on how quickly and effectively these challenges can be overcome, as well as on developments with competing classes of materials such as inorganic nanoparticles / wire / membranes [62] and films of graphene flakes [63, 64]. These considerations aside, we believe that the possibilities for real applications, together with the rich range of associated fundamental aspects, create a bright future for research and development of thin film SWNT electronic materials.

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