Complementary Logic Gates and Ring Oscillators on Plastic Substrates by Use of Printed Ribbons of Single-Crystalline Silicon

Dae-Hyeong Kim, Jong-Hyun Ahn, Hoon-Sik Kim, Keon Jae Lee, Tae-Ho Kim, Chang-Jae Yu, Ralph G. Nuzzo, and John A. Rogers

***Abstract*—CMOS inverters and three-stage ring oscillators were formed on flexible plastic substrates by transfer printing of p-type and n-type single crystalline ribbons of silicon. The gain and the sum of high and low noise margins of the inverters were as high as ∼150 and 4.5 V at supply voltages of 5 V, respectively. The frequencies of the ring oscillators reached 2.6 MHz at supply voltages of 10 V. These results, as obtained with devices that have relatively large critical dimensions (i.e., channel lengths in the several micrometer range), taken together with good mechanical bendability, suggest promise for the use of this type of technology for flexible electronic systems.**

***Index Terms*—CMOS inverter, flexible circuits, thin-film transistor (TFT).**

I. Introduction

LARGE AREA electronics is an increasingly important class of technology [1], with many new device possibilities that could be enabled by use of mechanically flexible substrates. In applications that demand sophisticated electronic functionalities, it is useful to combine n- and p-channel devices to yield CMOS logic. The power efficiency of such circuits [2] provides a significant advantage, especially for systems on plastic substrates where significant power dissipation by the circuits can, conceivably, degrade the plastic. Recent past work demonstrated nMOS transistors and nMOS circuits formed using printing-like techniques [3]–[7]. Such systems have limited practical utility due to the inefficiency of nMOS circuit designs. In this letter, we extend these previously reported methods to p-channel transistors, and introduce approaches for integration that yield full CMOS capabilities on plastic substrates. The performance characteristics of representative circuit elements exceed previous reports of other types of CMOS devices on flexible substrates (i.e. laser annealed silicon, organic semiconductors and others) as well as nanowire devices on rigid substrates [8]–[11]. Like any new technology, the cost of the process described here is difficult to estimate. We believe, however, that the cost can be low, based on its use of simple, printing-like techniques and its ability to be implemented with silicon derived from bulk wafers [12]. Circuits of this type have the potential to be useful for electronic systems that demand both high performance and power-efficient operation in lightweight, mechanically bendable designs.

Manuscript received August 14, 2007; revised October 5, 2007. This work was supported by the Department of Energy (DEFG02-91ER45439) and used the Center for Microanalysis of Materials of the Frederick Seitz Materials Research Laboratory supported by the Department of Energy (DEFG02-91ER45439). The review of this letter was arranged by Editor J. Sin.

D.-H. Kim, J.-H. Ahn, H.-S. Kim, K. J. Lee, T.-H. Kim, R. G. Nuzzo, and J. A. Rogers are with the Department of Materials Science and Engineering, Frederick Seitz Materials Research Laboratory and Beckman Institute for Advanced Science and Technology, Department of Chemistry, University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA (e-mail: jrogers@uiuc.edu).

C.-J. Yu is with the Department of Materials Science and Engineering, Frederick Seitz Materials Research Laboratory and Beckman Institute for Advanced Science and Technology, University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA, and also with the Department of Electronics and Computer Engineering, Hanyang University, Seoul 133-791, Korea.

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Digital Object Identifier 10.1109/LED.2007.910770

II. Device Fabrication

The procedures involve the sequential transfer printing of doped Si ribbons derived from silicon-on-insulator (SOI) wafers onto plastic substrates followed by processing to yield devices and circuits. This process begins with p- and n-type SOI wafers (Soitec, Unibond; p-type: Si (290 nm)/SiO_2 (400 nm), 6.0–9.4 $\times 10^{14}$ cm^{-3} doping; n-type: Si (260 nm)/SiO_2 (1000 nm), 2.7–5.2 $\times 10^{15}$ cm^{-3} doping). Phosphorous and boron spin-on-dopants (Filmtronics, P509 and B219) were used to accomplish the n and p doping for source and drain [13]. Defining patterns of resist by photolithography, etching the top Si with SF_6, and then removing the buried oxide with HF released Si ribbons with integrated, doped contacts. Contacting an elastomeric stamp of poly(dimethysiloxane) (PDMS) against these ribbons caused them to adhere to the PDMS surface, and peeling the stamp away removed the ribbons from the SOI wafer. This stamp was used to deliver ribbons to an adherent plastic substrate, thereby completing the transfer printing process. For CMOS applications reported here, this printing procedure [4]–[6] was performed twice, in a sequential fashion, with n and p doped ribbons. A polyimide (PI; DuPont, Kapton) sheet coated with bisbenzocyclobutene (∼1 μm; Dow Chemical, Cyclotene) provided the adherent substrate. Lithography, deposition, etch and liftoff defined gate dielectrics of SiO_2 [50 nm; formed by plasma-enhanced chemical vapor deposition (PECVD)] and source, drain, gate and interconnect metallization of Cr (5 nm)/Au (100 nm).

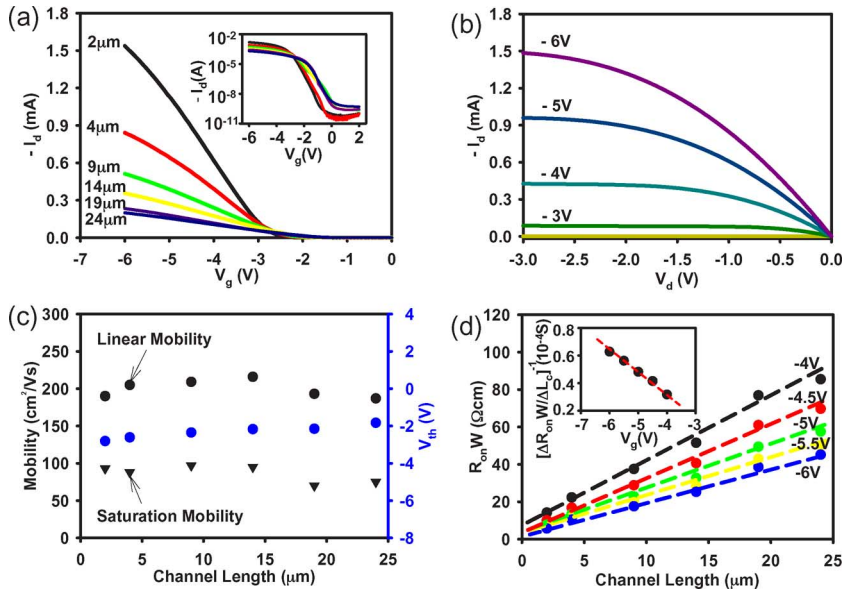

Fig. 1. (a) Source/drain current (I_d) as a function of gate voltage (V_g) evaluated at a source/drain bias (V_d) of -0.5 V, for pMOS TFTs with different channel lengths (L_c) between 2 and 24 μm (channel widths, W, of 180 μm) on a PI substrate. The inset shows a semilog plot of these data, illustrating on/off ratios of $\sim 10^6$. (b) Current–voltage characteristics of a pMOS TFT with $L_c = 9$ μm and $W = 180$ μm. (c) Linear and saturation mobility and threshold voltage $(V_{\rm th})$ as a function of channel length. (d) Width-normalized ON $(R_{\rm on})$ resistance as a function of channel length at different gate voltages. The dashed lines correspond to linear fits of the data. The inset shows the sheet conductance, determined from the reciprocal of the slopes of the linear fits in (d), as a function of gate voltage.

III. Results and Discussion

Fig. 1(a) shows transfer curves for Si-ribbon based pMOS thin-film transistors (TFTs) with channel lengths (L_c) between 2 and 24 μm, and contact overlaps (L_o; defined by the distance that the gate electrode extends over the doped source/drain regions) between 1.5 and 5.5 μm, all with channel widths (W) of 180 μm. Fig. 1(b) presents current–voltage characteristics for a representative device with $L_c = 9$ μm. The on/off ratios were $\sim 10^6$ and threshold voltages were -2.5 ± 0.5 V. The threshold voltage is larger with shorter channel length, perhaps due to effects of interface defect states [14]. The effective mobilities, calculated using standard field-effect transistor models [15], are 200 ± 20 cm^2/V $\cdot$ s and 85 ± 10 cm^2/V $\cdot$ s, in the linear and saturation regimes, respectively, independent of channel length, as shown in Fig. 1(c). Although lower than our nMOS results [6], as expected, they are higher than other types of pMOS devices on plastic, including laser annealed polycrystalline silicon [9], [10]. The gate leakage current was within tens of picoamperes. Also, the maximum gate-swing hysteresis was less than $\sim$0.5 V at a sweep rate of $\sim$25 V/s, reducing to approximately half of this value at faster rates ($\sim$125 V/s). We speculate that this hysteresis results from defects associated with trapped charges at the interface between Si and SiO_2, which is often observed with PECVD SiO_2 gate dielectrics in silicon devices [16]. Similar top gate devices fabricated on SOI substrates with thick buried oxide showed performance nearly identical to those on PI. This result suggests that the interface between the PECVD oxide and the silicon limits the performance. Fig. 1(d) shows the width-normalized resistance in ON-state $(R_{\rm on})$ evaluated at gate voltages between -4 and -6 V as a function of the channel length, indicating that the contact resistance is small compared to the channel resistances for most device geometries. The inset shows the variation of sheet conductance at different gate voltages [17]. The linear fit yields intrinsic device threshold voltage and mobility of -2.0 ± 0.5 V and 225 ± 15 cm^2/V $\cdot$ s.

Electrically interconnecting these devices with similar nMOS transistors can yield CMOS functionality on plastic. Fig. 2 shows optical images of CMOS inverters (top), a schematic diagram (left bottom) and log scale transfer curves (right bottom). The L_c and L_o are 12 and 10 μm, respectively; the channel widths of the pMOS and nMOS devices are 300 and 100 μm, respectively. The nMOS transistors showed properties consistent with previous reports [6]: effective linear and saturation mobilities of 550 ± 50 and 460 ± 50 cm^2/V $\cdot$ s, respectively, the threshold voltages of 0.2 ± 0.2 V and on/off ratios of $\sim 10^6$. The improved mobilities of nMOS and pMOS devices compared to previous reports of flexible devices in CMOS inverters based on organic or low temperature polysilicon (LTPS) materials [9]–[11] lead to better electrical performance. With a supply voltage of 5 V, these CMOS inverters exhibit good transfer characteristics with gains of $\sim$150 with high and low noise margins (NM_H and NM_L, respectively) around 3.9 and 0.6 V, respectively as shown in Fig. 2(b) and (c) [2]. The operation of this circuit is reasonably consistent with circuit simulations using PSPICE.

Good mechanical bendability is important for applications in flexible electronics. We performed systematic tests by mechanically bending the PI substrate to achieve approximate surface strain values between 0.051% and 0.29%, corresponding to bending radii of 25.5 and 4.5 mm, respectively, with a 25-μm-thick substrate [see the insets of Fig. 2(b) and (c)]. The strain values were computed by using the bend radii and the substrate thickness. The results indicate only small deviations of input voltage at maximum gain (V_M) and noise margins, which is smaller than wafer-level strained Si experiments [18], perhaps

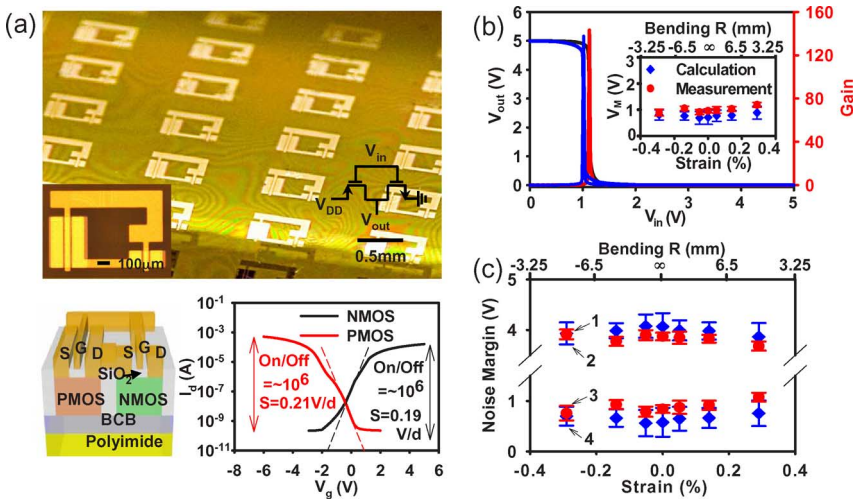

Fig. 2. (a) Optical image of an array of CMOS inverters on a PI substrate; the insets on the left and right bottom give a magnified image and circuit diagram, respectively (top). Schematic illustration of an inverter and log scale transfer curves for nMOS and pMOS devices (left and right bottom, respectively). (b) Transfer characteristics and gain for a typical device; the inset shows the change of voltage (V_M) at maximum gain as a function of bending-induced strain and bending radii. The error range corresponds to a standard deviation of the data. (c) Noise margin value at different strain values. [1: high noise margin (NM_H) calculation, 2: high noise margin (NM_H) measurement, 3: low noise margin (NM_L) calculation, 4: low noise margin (NM_L) measurement].

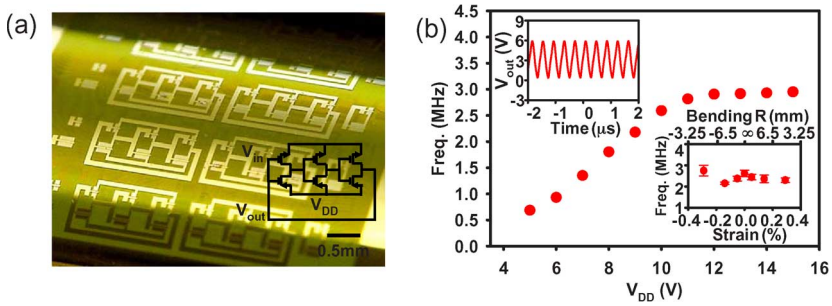

Fig. 3. (a) Image of an array of ring oscillators; the inset on the right bottom gives a circuit diagram. (b) Dependence of the oscillation frequency on the supply voltage (V_{DD}); the upper left inset shows output characteristics of an oscillator evaluated with a 10-V supply (V_{DD}); the lower right inset shows the variation in frequency as a function of bending radius and corresponding bending strain.

due to limitations in our simple estimates of the strains. The calculations using CMOS inverter models [19] and separately measured individual nMOS and pMOS device data at each bending radius agree well with the experiments as shown in Fig. 2(b) and (c).

More advanced circuits, such as ring oscillators, can be built by integrating a multiple of such CMOS inverters. Fig. 3(a) and its inset present optical images of three-stage ring oscillators on PI and their circuit diagram, respectively. The L_c, L_o and W for the transistors in the inverters are the same as those devices described above. The circuits exhibit an oscillation frequency of 2.6 MHz, corresponding to a stage delay of 64 ns. Even though this frequency is lower than that of recently reported LTPS devices (100 MHz at $V_{\mathrm{DD}} = 15$ V and $L_c = 2$ μm, self-aligned) [10], the performance is good considering our larger L_c and L_o and lower V_{DD} values ($\sim$10 V). As shown in Fig. 3(b), the oscillation frequency varies approximately linearly with the supply voltage up to $\sim$10 V above which the frequency remains unchanged. Thermal degradation, similar to that reported previously [20], [21], represents one possible explanation for this behavior. The inset of Fig. 3(b) shows bending test results that indicate slight but nonsystematic variations. Strains, either tensile or compressive, are known to affect the output performance both at the device and the circuit levels. Studies of parallel channel ring oscillators on silicon wafers under uniaxial strain with mechanical bowing showed insignificant speed changes due to simultaneous strain effect on both nMOS and pMOS [22]. Thus, it is believed that these strain-induced effects on our ring oscillators with parallel channel layout compensate each other, resulting in an insignificant variation in output performance.

IV. Conclusion

This letter describes procedures for implementing single crystal silicon CMOS inverters and ring oscillators on flexible plastic substrates. Electrical and mechanical measurements show performance that could be valuable for emerging classes of flexible electronics whose requirements lie beyond those achievable with organic semiconductors, polysilicon and other approaches. The same methods presented here should be applicable to more complex circuits; this possibility represents a useful direction for future research.

ACKNOWLEDGMENT

D.-H. Kim and J.-H. Ahn contributed equally to this paper.

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