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p-Channel, n-Channel Thin Film Transistors and p–n Diodes Based on Single Wall Carbon Nanotube Networks

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ABSTRACT

This paper demonstrates the use of arrays of networks of single wall carbon nanotubes (SWNTs) and electrical breakdown procedures for building thin film transistors (TFTs) that have good, reproducible performance and high current output. Channel length scaling analysis of these TFTs indicates that the resistance at the source/drain contacts is a small fraction of the device resistance, in the linear regime. When measured with the channel exposed to air or coated by poly(methyl methacrylate) (PMMA), these transistors operate in the unipolar p mode. By spin-coating the polymer polyethylenimine (PEI) on the channel region, these transistors can be switched to operate in the unipolar n mode. Patterning the exposure of a single channel to PMMA and PEI yields p–n diodes. These results indicate that SWNT-TFTs can provide the building blocks of complex complementary circuits for a range of applications in macroelectronics, sensors, and other systems.

Semiconducting single wall carbon nanotubes (SWNTs) with diameters between 1 and 4 nm represent one-dimensional electronic materials that have exceptionally good properties: their mobilities can be as high as 100 000 cm^2/Vs,[1] their current carrying capacity can exceed 10^9 A/cm^2 (refs 2,3), and the ON/OFF current ratios can be larger than 10^5.[4] A variety of devices, based on the integration of individual SWNTs with lithographically defined metal electrodes have been demonstrated, including field effect transistors (FETs),[5] diodes,[6−8] logic circuit elements,[9] optical emission devices,[10] and chemical sensors.[11] In an ambient environment, semiconducting SWNTs generally show unipolar p-type behavior.[3,4] By doping with potassium, the unipolar p-type behavior can be switched to unipolar n-type behavior. This approach has been used to build single tube p−n diodes[8] and complementary logic gates.[9] n-Type doping can also be realized by simply spin casting polyethylenimine (PEI) on top of a SWNT.[12,13] These favorable intrinsic electrical characteristics and the easy ability to tune them make these single SWNT devices potentially attractive for a range of applications. Realistic circuits and devices, however, require solutions to significant challenges associated with precisely controlling the electronic properties (e.g. mobility, ON current, OFF current, etc.) of the tubes, defining their spatial positions and orientation, and forming reliable low barrier contacts to them.

Recent reports describe thin film p-type FETs that use oriented arrays[14] of SWNTs or two-dimensional (2D) percolation networks[15] to avoid some of these challenges. The reported thin film transistors (TFTs) based on arrays achieve high ON/OFF ratios (10 000) by electrical breakdown of the individual metallic tubes, but they exhibit relatively low mobilities (0.1 cm^2/Vs).[14] Devices that use networks[15] exhibit mobilities of 7−270 cm^2/Vs. Although ON/OFF ratios of 10 000 can be achieved for low-density networks (1 μm^{-2}; slightly above the percolation threshold 0.1−0.3 μm^{-2} for tube lengths 1−3 μm), for high-density networks (> 3 μm^{-2}), ON/OFF ratios are typically less than 10. Also, for channel lengths comparable to or shorter than the average length of the SWNTs in the network, the device properties can depend strongly on channel geometry and they can vary from device to device.

Here we present p and n channel TFTs that use arrays of isolated stripes of SWNT networks in which metallic pathways are eliminated by electrical breakdown. The network density is about 2−10 μm^{-2}, well above an approximate estimate of the percolation threshold density of 0.01−0.04 μm^{-2} (tube length 5−10 μm). When operating in ambient conditions, such devices show unipolar p-type

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performance with uniform mobilities (up to 40 cm^2/Vs) and ON/OFF ratios of 100−1000, even with networks of nanotubes that have diameters ranging from 1 to 3 nm and which contain metal tube content of ∼30%. Studies of channel length scaling suggest that the contacts do not limit the device performance. When coated with PEI, these same devices show unipolar n-type behavior. Patterning the SWNT network stripes within the channel into adjacent p and n type regions yields devices that behave like p−n diodes. Collectively, these results demonstrate that TFTs based on SWNT network stripes can form the basic building blocks for complementary logic circuits.

Degenerately doped Si substrates with 100 nm dry thermal silicon dioxide provide the gate electrode and gate dielectric, respectively, for all of the devices presented here. Chemical vapor deposition (CVD) forms submonolayer networks of SWNTs on these substrates. The growth recipe is similar to that described in ref 16 using commercial ferritin (Sigma) diluted 100 times with distilled water as catalyst. The randomly aligned tubes have diameters about 1−3 nm and lengths $l \sim 5-10\ \mu m$. Tube density of $2 \sim 10\ \mu m^{-2}$ can be achieved uniformly over substrates with dimensions of 1 × 6 cm; this density is well above the threshold density $\rho_{th} \sim 1/\langle l \rangle^2 \sim 0.01-0.04\ \mu m^{-2}$ as estimated based on a simple description of the network as a system of infinite extent with percolation theory.[17−19] These networks electrically conduct like a two-dimensional electronic material due to the good tube−tube contact.[15,20]

Patterning Pd source/drain contacts on top of these substrates by electron beam lithography,[3,7] or by Si_3N_4 membrane based shadow mask evaporation (SME)[21] forms arrays of devices. SME allows quick deposition of contacts by a single evaporation without exposing the tubes to any chemical processing. This technique may also have some promise for low-cost, large-area fabrication of flexible circuits.[22] Devices made by SME typically showed slightly higher or comparable performance compared to those made by electron beam lithography. Figure 1a shows a scanning electron microscope (SEM) image of part of a typical shadow mask. The black areas are open holes through which the Pd passes during evaporation. Part 1 labels the Si_3N_4 stripes that define the separation distances between the source and drain electrodes. Part 2 labels the Si_3N_4 membranes that isolate neighboring channels in the same row. Part 3 is the supporting silicon substrate. Figure 1b shows an image of an array of devices with the channel length ranging from 2 to 50 μm. The widths of channels in Figure 1b are all 200 μm. The inset shows an SEM of one channel.

Cutting stripes in the SWNT network film completes the device fabrication. The cutting is accomplished by exposure of selected regions of the film to an oxygen reactive ion etch (PlasmaTherm 760) through a resist of poly(methyl methacrylate) (PMMA) patterned by deep ultraviolet (UV) photolithography. Figure 1c illustrates the geometry of the stripes. The PMMA is removed by acetone and the sample substrate is rinsed by 2-propanol after etching. Figure 1d shows an atomic force microscope (AFM) image of a device with a channel length of 2 μm. Carbon nanotubes exist only

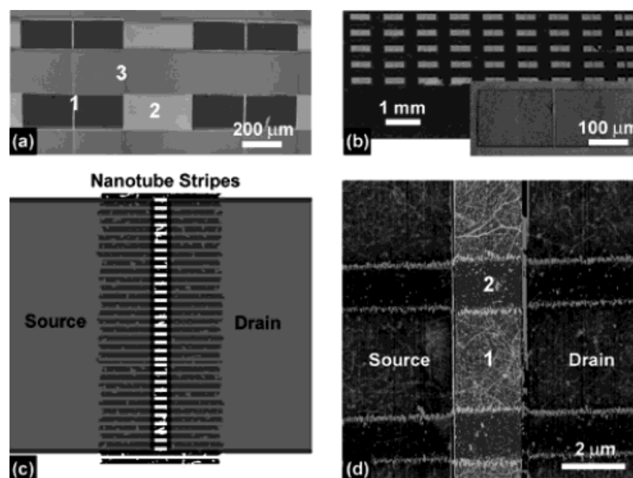

Figure 1. (a) Scanning electron microscope (SEM) image of a Si_3N_4 membrane based shadow mask. Region 1 is the suspended membrane stripe for channel lengths between 2 μm to 50 μm. Region 2 is the suspended membrane blocks which isolate channels in the same row. Region 3 is the support silicon substrate which isolates channels in the same column. (b) Optical image of arrays of channels made by shadow mask evaporation. Channel lengths vary from 2 to 50 μm from left to right. Inset shows an SEM image of one channel. (c) Schematic illustration of a thin film transistor based on patterned arrays of nanotube networks. The structures are formed by selectively removing (by oxygen reactive ion etching) regions of a uniform nanotube network formed by chemical vapor deposition. In the case illustrated here, the widths of the patterned stripes are 3−4 μm with a spacing of 1−2 μm. (d) Atomic force microscope (AFM) image of a thin film transistor based on carbon nanotube strip arrays with channel length of 2 μm. Nanotubes in region 1 remain intact while nanotubes in region 2 are removed by etching.

in the array of stripes, each of which has a width of 3−4 μm. The stripes isolate channels of multiple devices from each other. We also observed that in many cases they also enhance the final step in processing the devices: electrical breakdown of metallic pathways from source to drain. In this procedure, a voltage of between +20 and +30 V is applied to the gate and then a negative voltage is applied between the source and drain. These large positive gate voltages turn off the p-type semiconducting SWNT. At a well defined source/drain bias voltage, most of the current irreversibly disappears after multiple sweeps. Figure 2a shows the breakdown voltages for devices with different channel lengths. The voltages were selected carefully to minimize degradation of the device mobility. It is reasonable to expect that longer channels require larger voltages for breakdown, although the exact relationship depends on many factors, including degree of heat sinking to electrodes, etc.[23]

All measurements are carried out in the ambient environment. Figure 2b shows the transfer characteristics of a device (device 1; $L = 2\ \mu m$ $W = 200\ \mu m$) before and after breakdown when the gate voltage is swept from −20 V to +20 V at a source/drain bias voltage of 0.5 V. This device and all others that we built operated in the unipolar p mode, consistent with observations of single tube devices. Before the electrical breakdown, the ON/OFF ratio can be as small as 3−4 for channels with L = 2 μm. Roughly 1/3 of the SWNT in CVD grown tubes are metallic.[24] The large OFF

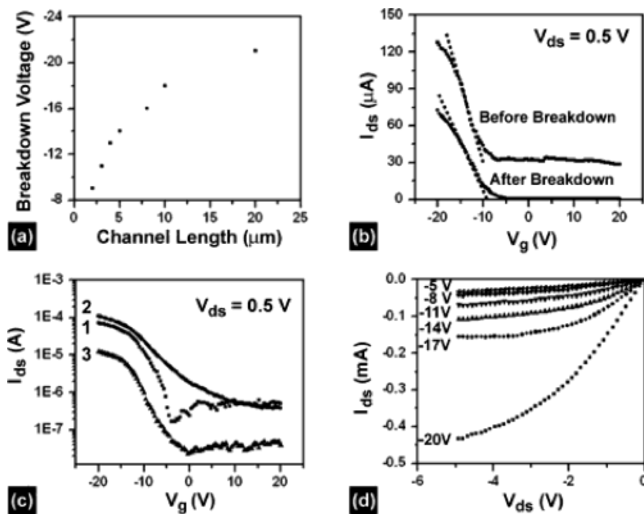

Figure 2. (a) Breakdown voltages used for channels with different length. Electrical breakdown of metallic conducting path is realized by sweeping the source/drain bias voltage with a maximum voltage 1−2 V below the breakdown voltage while applying a positive gate voltage of 20−30 V. (b) Transfer characteristics of Device 1 (L = 2 μm, W = 200 μm) before and after the electrical breakdown. ON and OFF current difference and the mobility are typically only 10−30% lower after the electrical breakdown. (c) Transfer characteristics in a log format for three different channels. Device 2 (L = 7 μm, W = 100 μm) has a device mobility of 40 cm^2/Vs which is the highest among nearly 400 channels measured. In Device 3 (L = 20 μm, W = 200 μm), the stripes have a length of 20 μm with a width of 3 μm. (d) Output characteristics when the gate voltage is increased from −20 V to −5 V with a step size of 3 V for Device 1. Typical saturation behavior for transistors is clearly observed.

current in the case of devices with L comparable to or substantially less than $\langle l \rangle$ includes substantial contributions from single metallic tubes spanning the channel. For all devices, multitube metallic pathways from source to drain also give rise to the OFF current. Electrical breakdown can remove both of these contributions to the OFF current. The first several sweeps of the electrical breakdown process usually show abrupt current drops of about 25 μA.[2] Current drops of 1 μA or smaller occur in subsequent sweeps. ON/OFF ratios of 100−1000 can be reached with only 10−30% loss of the mobility value. This moderate decrease may be due to loss of semiconducting multitube pathways that include metallic tubes which are also part of metallic pathways that are destroyed during the breakdown process. The loss of large diameter semiconducting tubes with small band-gap,[25] which cannot be turned off completely even at a gate voltage of between +20 and +30 V, may also contribute to the loss. Further improvement of the ON/OFF ratio above this level by breakdown at higher voltages usually causes degradation of devices with dramatic decreases (∼10×) in mobility. It is likely that improved ON/OFF ratios will be possible by reducing the content of metallic tubes in the network, especially when multitube metallic pathways dominate the OFF current. We observed that the stripe geometry typically improved the efficiency of the breakdown procedure. Without the stripes, we often observed large decreases (10×) in the device mobility after similar breakdown process, especially for channels longer than 4 μm. Cutting the film into stripes avoids single long metallic tubes that span the channel at steep angles and effectively long multitube metallic pathways.

To calculate the device mobilities, we treat the channels similar to those made with conventional uniform semiconducting thin films. For simplicity, we only calculate the linear mobility which can be obtained from the slope in the transfer characteristics by the formula $\mu = (L/W)\ (t/\epsilon_r\epsilon_0)\ (dI_{ds}/V_{ds}\text{-}dV_g)$ where the gate dielectric thickness t is 100 nm and the dielectric constant for silicon oxide ϵ_r is 3.9. From Figure 2b, we obtain the device mobility of 6 cm^2/Vs after breakdown for Device 1. Figure 2c shows transfer characteristics of devices from different substrates after breakdown. Device 1 has an ON/OFF ratio of 120. Although variations in mobility from device to device on a given substrate are small, significant differences can be observed from substrate to substrate. Device 2 (L = 7 μm, W = 100 μm) has a device mobility of 40 cm^2/Vs and ON/OFF ratio of 250. This device, and others made on the same substrate, exhibit the highest mobilities that we observed. The density of the tubes is likely to be an important factor in determining the mobility. In Device 3 (L = 20 μm, W = 200 μm), the stripes have a large aspect ratio with a length of 20 μm with a width of 3 μm. These data clearly demonstrate that the percolation network conducts effectively like a uniform two-dimensional film. Among nearly 400 channels tested, the device mobility value ranges from 3 to 40 cm^2/Vs. Our fabrication process may also apply to networks with much higher density, which may allow further improvement of the mobility.

The output characteristics for Device 1 under various gate voltages V_g in steps of 3 V are shown in Figure 2d. The shapes of source/drain current versus source/drain bias voltage ($I_{ds}-V_{ds}$) curves closely resemble the output characteristics of conventional p-type TFT, exhibiting linear regions at low V_{ds} and saturation regions at higher V_{ds}. The current levels are in the mA range, which is much higher than typical output from single tube based transistors. We note that we observed a reduction of the ON/OFF ratio with increasing V_{ds} in almost all devices. This effect is the subject of current study.

With our tube density (2−10 μm^{-2}), which is nearly 2 orders of magnitude higher than the percolation threshold density (0.01−0.04 μm^{-2}), we find that nearly all samples built from the same CVD substrate of the size 1 cm × 6 cm have similar mobilities. Figure 3a shows the mobility of 60 devices built from five separately processed pieces of a single CVD substrate. Although the channel lengths range from 2 to 50 μm, the average mobility value is 5.7 cm^2/Vs with a standard deviation of 1.8 cm^2/Vs. This level of uniformity in performance indicates some promise for the use of these types of devices in realistic applications.

The uniformity also enables study of the scaling of ON currents with channel dimensions to reveal the role of contacts in these devices. Figure 3b shows that for channel lengths between 2 and 20 μm, the ON current depends, to a good approximation, inversely on the channel length. These results suggest that the device behavior is consistent with a

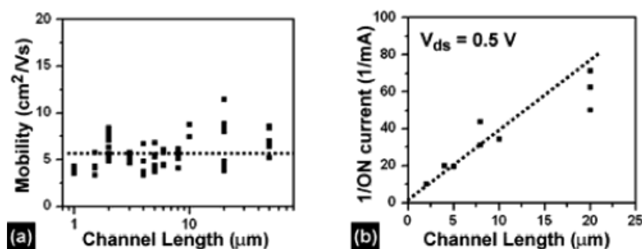

Figure 3. (a) SWNT TFT device mobility, measured in the linear regime, as a function of channel length. The apparent mobility does not depend strongly on channel length for this range of dimensions. (b) Channel length scaling of the ON current. All channels have the same width of 200 μm.

conventional thin film transistor whose contact resistances are small compared to the total device resistance. The current also scales linearly with the channel width, which can be easily understood since the channel width only changes the number of the stripes in the channel.

Obtaining both p and n-channel devices is crucial to achieving efficient operation of complex logic circuits. Single wall carbon nanotubes can be functionalized by amine-rich polymers such as PEI to switch their operation from p-type to n-type irreversibly.[13,14] This same approach works for the types of SWNT TFTs introduced here. To build n channel devices, we first dissolve low molecular weight PEI (~800, Aldrich Chemicals) in methanol with a volume concentration of 1:5. Then the solution is coated onto the exposed channel of a device at a spin speed of 2000 rpm and the sample is baked at 45 °C for 10 min to dry out the solvent. Without any further processing, this procedure converts an originally unipolar p-type device into a unipolar n-type one. Figure 4a shows the transfer characteristics before and after PEI coating of a device ($L = 2$ μm, $W = 200$ μm) at a source/drain bias voltage $V_{ds} = 0.5$ V. Originally the device is p-type with ON current of 67 μA, mobility value of 6 cm^2/Vs, and ON/OFF ratio of 150. After the doping, the channel becomes n-type with ON current of 12 μA, mobility value of 0.6 cm^2/Vs, and ON/OFF ratio of 12. Reliable n-type behavior was observed for low source/drain voltages for all ~10 devices that were tested, although full doping as displayed in single tube devices[12,13] was not observed. The reduced performance for n-type behavior may be ascribed to incomplete doping for some tubes in the stripes. Some tubes may still remain p-type, which gives higher OFF current. Further improvement of this doping process will require additional work.

This same coating procedure can be applied selectively to different parts of the channel of a single device to build complex devices. As a simple example, it is possible to build p−n diodes, which are widely used in rectification, switching, photonic devices, and other operations in modern electronic applications. To fabricate such a device, we start with a p-type TFT channel as discussed above. By using deep UV lithography of PMMA followed by uniform coating of PEI, we pattern the channel so that half of it is coated by PMMA and the other half by PEI, as illustrated in Figure 4b. The area coated by PEI becomes n-type while the other part remains p-type. Figure 4c shows the transfer characteristics of a p−n diode made from originally p-type device ($L = 8$

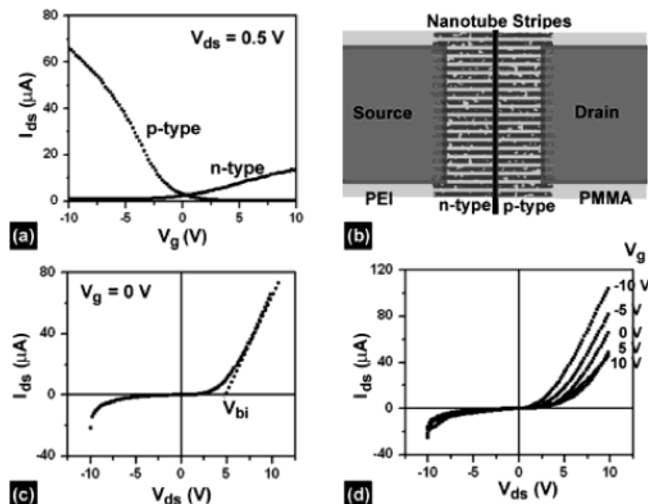

Figure 4. (a) Transfer characteristics of a SWNT-TFT measured before and after coating with PEI. This polymer converts the initial unipolar p type operation to unipolar n type. (b) Schematic illustration of a p−n diode formed by patterning PEI onto one-half of the channel region, by using PMMA resist formed by deep UV lithography. In this case, one-half of the channel is p-type and the other half is n-type. (c) Transfer characteristics of a gated p−n diode ($L = 8$ μm, $W = 200$ μm) measured at zero gate voltage. It behaves like a diode with series resistance. (d) Output characteristics of the p−n at different gate voltages. The built-in potential is modulated by the gate voltage.

μm, $W = 200$ μm) when there is no gate voltage applied. When a forward bias, or positive bias voltage on the p-side, is applied, the current increases rapidly as the voltage increases. However, for a reverse bias, virtually no current (~1 μA) flows until a breakdown voltage of 9 V is reached. The current−voltage charactertistics can be qualitatively explained by a p−n junction with series resistance effect.[26] From the slope at high forward bias voltage, we can define a series resistance $R_s = 36$ kΩ. The s-intercept gives a built-in potential $V_{bi} = 4.6$ V.

Since the diode is based on a thin film, both the p-side and n-side can be modulated by the back gate voltage V_g. Figure 4d shows the output characteristics of the p−n diode in Figure 4c. Negative gate voltages decrease the built-in potential with larger decrease for higher gate voltage. At $V_g = -5$ V, V_{bi} is reduced to 3.2 V, while at $V_g = -10$ V, $V_{bi} = 2$ V is even smaller. When the gate voltage ispositive, $V_g = +5$ V, V_{bi} is increased to 4.9 V. But when we increase the positve gate voltage further to $V_g = +10$ V, the current−voltage characteristics remains similar to that at $V_g = +5$ V. The ability to tune the built-in potential by the gate modulation may enhance the performance the diodes for a range of applications. Further investigation will reveal the basic mechanisms for operation of this type of p−n diode.

In conclusion, we present a type of TFT based on arrays of stripes of percolation networks of SWNTs with the metallic conduction reduced through electrical breakdown. These devices show relatively high device mobility of 3−40 cm^2/Vs and ON/OFF ratios (at small V_{sd}) of 100−1000. Although one-third of tubes are metallic and tubes have different diameters, characteristic of standard CVD growth conditions, channels made from the same CVD substrate of

the size 1 cm × 6 cm have uniform performance with both good length scaling and width scaling. These devices can be switched from unipolar p-type behavior to unipolar n-type behavior by simply spin coating a layer of PEI on the channel region. Coating one-half of a single channel with this polymer yields gate-modulated p−n rectifying diodes. These results represent essential elements for complex complementary circuits. The level of performance that we present here makes these devices potentially attractive alternatives to amorphous silicon and organic semiconductors for niche applications in flexible displays, sensors, and other areas of macroelectronics.[27,28] Their mobility may be improved by increasing of the tube density while the ON/OFF ratio may be enhanced dramatically by decreasing the metallic tube content. Realistic application of these type of devices may also require supression of the hysteresis.[13] Such improvements could make these devices important for a range of systems, including those that demand high performance.

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References

(1) Durkop, T.; Getty, S. A.; Cobas, E.; Fuhrer, M. S. *Nano Lett.* **2004**, *4*, 35.
(2) Yao, Z.; Kane, C. L.; Dekker, C. *Phys. Rev. Lett*. **2000**, *84*, 2941.
(3) Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. J. *Nature* **2003**, *424*, 654.
(4) Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P.; Lundstrom, M.; Dai, H. J. *Nature Mater.* **2002**, *1*, 241.
(5) Tans, S. J.; Verschueren, A. R. M.; Dekker, C. *Nature* **1998**, *393*, 49.
(6) Antonov, R. D.; Johnson, A. T. *Phys. Rev. Lett.* **1999**, *83*, 3274.
(7) Freitag, M.; Radosavljevic, M.; Zhou, Y. X.; Johnson, A. T.; Smith, W. F. *Appl. Phys. Lett.* **2001**, *79*, 3326.
(8) Zhou, C. W.; Kong, J.; Yenilmez, E.; Dai, H. J. *Science* **2000**, *290*, 1552.
(9) Backtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. *Science* **2001**, *294*, 1317.
(10) Misewich, J. A.; Martel, R.; Avouris, Ph.; Tsang, J. C.; Heinze, S.; Tersoff, J. *Science* **2003**, *300*, 783.
(11) Kong, J.; Franklin, N. R.; Zhou, C. W.; Chapline, M. G.; Peng, S.; Cho, K. J.; Dai, H. J. *Science* **2000**, *287*, 622.
(12) Shim, M.; Javey, A.; Kam, N. W. S.; Dai, H. J. *J. Am. Chem. Soc.* **2001**, *123*, 11512.
(13) Siddons, G. P.; Merchin, D.; Back, J. H.; Jeong, J. K.; Shim, M. *Nano Lett.* **2004**, *4*, 927.
(14) Seidel, R.; Graham, A. P.; Unger, E.; Duesberg, G. S.; Liebau, M.; Steinhoegl, W.; Kreupl, F.; Hoenlein, W. *Nano Lett.* **2004**, *4*, 831.
(15) Snow, E. S.; Novak, J. P.; Campbell, P. M.; Park, D. *Appl. Phys. Lett.* **2003**, *82*, 2145.
(16) Shim, M.; Siddons, G. P. *Appl. Phys. Lett.* **2003**, *83*, 3564.
(17) Kirkpatrick, S. *Rev. Mod. Phys.* **1973**, *45*, 574.
(18) Dobson, M. A.; Garland, J. C. *Phys. Rev. B* **1985**, *32*, 7621.
(19) Frank, D. J.; Lobb, C. J. *Phys. Rev. B* **1988**, *37*, 302.
(20) Fuhrer, M. S.; Nygard, J.; Shih, L.; Forero, M.; Yoon, Y. G.; Mazzoni, M. S. C.; Choi, H. J.; Ihm, J.; Louie, S. G.; Zettl, A.; McEuen, P. L. *Science* **2000**, *288*, 494.
(21) Zhou, Y. X.; Johnson, A. T.; Hone, J.; Smith, W. F. *Nano Lett.* **2003**, *3*, 1371.
(22) Baude, P. F.; Ender, D. A.; Haase, M. A.; Kelley, T. W.; Muyres, D. V.; Theiss, S. D. *Appl. Phys. Lett.* **2003**, *82*, 3964.
(23) Collins, P. G.; Arnold, M. S.; Avouris, Ph. *Science* **2001**, *292*, 706.
(24) Li, Y. M.; Mann, D.; Rolandi, M.; Kim, W.; Ural, A.; Hung, S.; Javey, A.; Cao, J.; Wang, D. W.; Yenilmez, E.; Wang, Q.; Gibbons, J. F.; Nishi, Y.; Dai, H. J. *Nano Lett.* **2004**, *4*, 317.
(25) Dresselhaus, M.; Dresselhaus, G.; Avouris, Ph. *Carbon Nanotubes: Synthesis, Structure, Properties and Applications*; Spring: Berlin, 2001.
(26) Sze, S. M. *Semiconductor Devices: Physics and Technology*; John Wiley & Sons: New York, 2001.
(27) Rogers, J. A.; Bao, Z. N.; Baldwin, K.; Dodabalapur, A.; Crone, B.; Raju, V. N.; Kuck, V.; Katz, H. E.; Amundson, K.; Ewing, J.; Drzaic, P. *Proc. Natl. Acad. Sci. U.S.A.* **2001**, *98*, 4835.
(28) For reviews and references, see Kagan, C. R., Andry, P., Eds.; *Thin Film Transistors*; Marcel Dekker: New York, 2003.
(29) Radosavljevic, M.; Freitag, M.; Thadani, K. V.; Johnson, A. T. *Nano Lett.* **2002**, *2*, 761.

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