A printable form of silicon for high performance thin film transistors on plastic substrates

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Free-standing micro- and nanoscale objects of single crystal silicon can be fabricated from silicon-on-insulator wafers by lithographic patterning of resist, etching of the exposed top silicon, and removing the underlying SiO_2 to lift-off the remaining silicon. A large collection of such objects constitutes a type of material that can be deposited and patterned, by dry transfer printing or solution casting, onto plastic substrates to yield mechanically flexible thin film transistors that have excellent electrical properties. Effective mobilities of devices built with this material, which we refer to as microstructured silicon (μs-Si), are demonstrated to be as high as 180 cm^2/V s on plastic substrates. This form of "top down" microtechnology might represent an attractive route to high performance flexible electronic systems. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1767591]

Solution processable conductors, dielectrics, and semiconductors together with flexible plastic substrates represent enabling materials for electronic circuits that can be fabricated by continuous, high speed printing techniques.[1–6] It is generally believed that these types of systems, which can cover large areas, will be important for new applications in consumer electronics.[7–10] This letter describes a semiconducting micro/nanomaterial which we refer to as microstructured silicon (μs-Si), that can be printed, using dry transfer or solution based techniques, onto plastic substrates to produce high performance TFTs. Effective mobilities, as determined by standard analysis of current–voltage characteristics, are as large as $\sim$180 cm^2/V s.

Figure 1 schematically illustrates representative steps for producing μs-Si. The process begins by stripping the native oxide layer from a conventional SOI substrate by using dilute (1%) HF. Immediately loading the wafer into an electron beam evaporator (Temescal BJD1800) followed by sequential deposition of Al (20 nm; 0.1 nm/s) and then Au (100 nm; 1 nm/s) forms a metallization layer on the top silicon. Microcontact printing or photolithography and etching (TFA for Au; AL-11 premixed Cyantec etchant for Al) patterns the Al/Au into desired geometries. Anisotropic wet etching of the exposed silicon (TMAH; 3.5 min for 100-nm-thick Si) defines smooth sidewalls on Al/Au coated elements of single crystal silicon that lift-off of the wafer when the underlying SiO_2 is etched away with concentrated (49%) HF. The Al/Au can be removed or it can be integrated directly into a final device structure as, for example, source and drain electrodes in a thin film transistor. Certain aspects of these processing steps are similar to those used for fabricating beams and wires of silicon designed for other applications.[11–13]

Figure 2 presents optical and scanning electron micrographs of a range of μs-Si microstrips. It shows them in ethanol suspensions and as cast onto substrates of various types. Wires, platelets, disks, etc., could also be formed in this manner. Note the smooth etched sidewalls of these objects. By use of large area soft lithographic techniques, it is possible, in a single low cost processing sequence, to produce large numbers (i.e., billions) of such objects with lateral dimensions down to 50 nm (and possibly smaller) and with nearly any geometry. For the TFTs in typical flexible electronic systems, long ($\sim$10 μm) and narrow ($\sim$1 μm) strips of silicon are useful. We used two approaches to transferring the μs-Si to substrates for integration into TFTs. The first takes advantage of the known orientation and position of the μs-Si objects just prior to their lift-off from the SOI substrate. In this case, procedures similar to those of soft lithographic transfer printing techniques[14–19] are used to move the μs-Si from the SOI (after etching away the SiO_2 but before lifting off the silicon) to desired locations on the device substrate. In particular, a conformable elastomeric transfer element [i.e., flat piece of poly(dimethylsiloxane)] picks up the objects from the SOI surface and transfers them to a desired substrate. Similarly, μs-Si objects can be directly transferred onto thin plastic substrates by Au cold welding using receptacle pads defined on the surface of the target substrate. Figure 3(a) present an image of transferred μs-Si onto a PDMS coated polyimide sheet: the microstrips are well aligned and transferred with controlled orientation. We did not observe any cracking of the μs-Si (by careful examination with a scanning electron microscope) even when the substrate was bent significantly. Similar results were obtained (without the need of an elastomeric layer) using a Au coated thin Mylar sheet as illustrated by the bottom inset micrograph picture. Note that a coverage density close to 100% can be achieved in this manner. In the other approach, the μs-Si objects are lifted off of the SOI substrate and dispersed into solvent to form a suspension that can be cast onto the device substrate using solution based printing approaches. This strategy has the advantage that it can be performed with many of the techniques that have already been explored for plastic electronics (i.e., ink jet printing, thermal transfer printing, screen printing, etc.).[20–22] Both methods can be carried out at room temperature in an ambient environment. They are, therefore,

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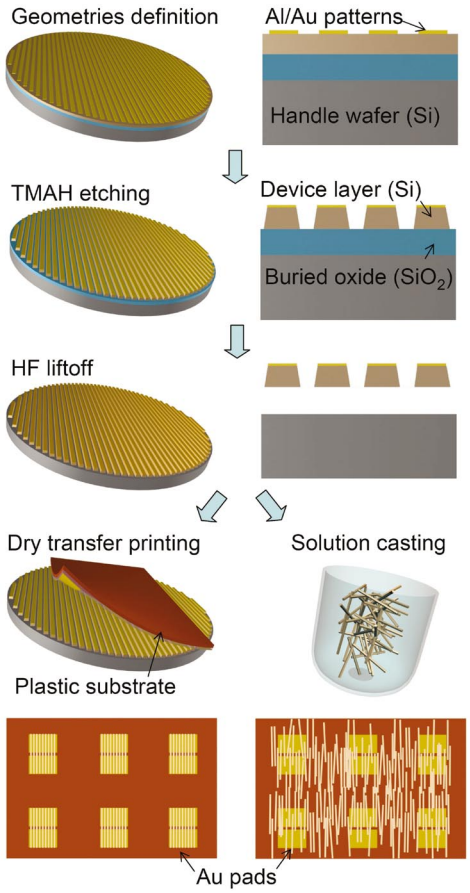

FIG. 1. (Color) Schematic illustration of representative processing steps for producing microstructured silicon (μs-Si). Conventional or soft lithographic procedures define patterns of Al(20 nm)/Au(100 nm) on the top surface of a silicon-on-insulator substrate. Anisotropic wet etching (50:75 TMAH/H_2O at 90 °C for ~3 min) of the exposed regions of the silicon, followed by removal of the underlying SiO_2 (etching with HF) lifts off micro/nanoscale objects of single crystal silicon. These objects, which we refer to collectively as μs-Si, can be dry transfer printed or solution cast at ambient conditions onto a wide variety of device substrates, including low cost plastic sheets, for building devices such as high performance thin film transistors.

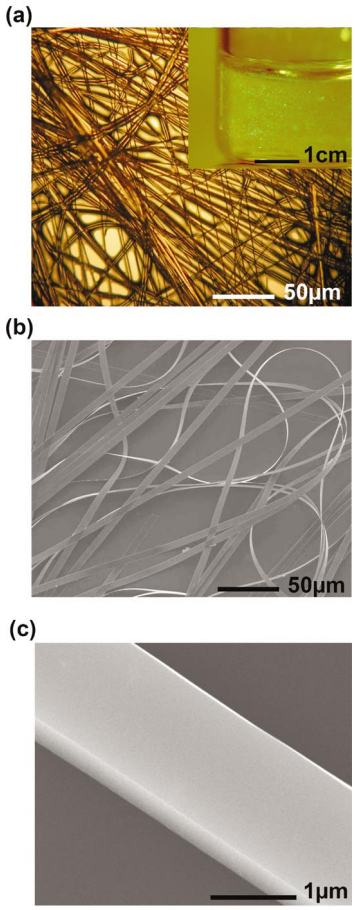

FIG. 2. (Color) Images of micro- and nanoscale elements of single crystal silicon. (a) An optical micrograph of a solution cast tangled mat of silicon rods (widths 2 μm; thickness 2 μm; lengths ~15 mm). The inset image shows μs-Si strips (roughly 10 million of them) dispersed in a solution of ethanol. The low resolution SEM image in (b) illustrates the mechanical flexibility range of some flat microstrips (thickness 340 nm; widths 5 μm; lengths ~15 mm) solution casted onto a bare silicon wafer. (c) A high resolution SEM image of one of these objects. Note the extremely smooth sidewalls generated by the anisotropic wet etching procedures.

compatible with a wide range of substrates, including low cost plastics.

Figure 3(b) shows an optical micrograph (inset) and electrical characteristics of a μs-Si device built on the SOI wafer (Si thickness of 100 nm, etched in an array of 25-μm-wide strips, with an underlying oxide with 200-nm thickness). Lifting these ribbons off of the substrate and transferring them to plastic yield devices with similar cases. Figure 3(c) presents an optical micrograph of such a μs-Si TFT. The substrate consists of a Mylar sheet coated with indium tin oxide (ITO, ~100-nm thick) as a gate and a photocured epoxy as a gate dielectric (SU8-5; Microchem Corp). The capacitance of the dielectric (2.85 nF/cm^2) was evaluated using capacitor test structures formed near the device. This device uses solution cast μs-Si that consists of a 20-μm-wide and 340-nm-thick strip obtained from a *p*-doped SOI wafer. A 25-nm-thick layer of SiO_2 was grown on top of the silicon by dry oxidation in a horizontal quartz tube furnace prior to transfer. Source and drain electrodes of Al(20 nm)/Au(180 nm) were defined by liftoff. The channel length is 50 μm and the width is 20 μm. Figure 3(c) shows electrical measurements collected from this device. The Al/Au metallization provides reasonably low resistance Schottky barrier contacts to the silicon, as expected for an Al (work function of 4.2 eV) metallization on *p*-doped silicon.[23] Aluminum is well known to diffuse rapidly into silicon, but no special care was taken to avoid localized aluminum–silicon interactions as no postmetallization high temperature annealing step was carried out. The on/off ratio of this device is slightly lower than ~10^3. Analysis of the transfer characteristic of Fig. 3(c) indicates linear regime mobility of 180 cm^2/V s using a parallel plate model for the dielectric capacitance.[24] For simplicity, this analysis ignores the effects of contacts and processing induced changes in the threshold voltage.

Even with perfect contacts, there are theoretical arguments to suggest that transistors which incorporate very high aspect ratio (i.e., ultralarge length to width ratios) semiconducting elements in the channel region (i.e., nanotubes or nanowires) will have responses that are different than those of conventional devices.[25] To avoid these effects, we chose μs-Si made of microstrips that have widths in the same order with the transistor channel length. The properties (mobilities, normalized transconductance, on/off ratio) observed here are ~3/4 to those of TFTs made on the SOI

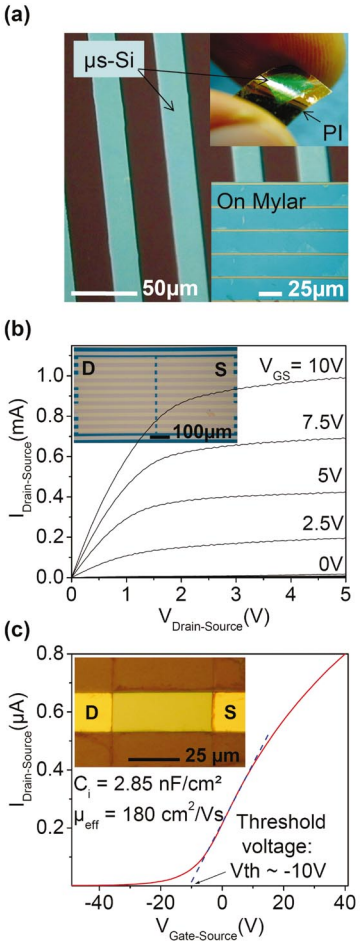

FIG. 3. (Color) High performance thin film transistor formed with μs-Si as the semiconductor. (a) A top view micrograph of μs-Si transferred onto a PDMS coated Kapton sheet (25-μm thick). The top inset pictures illustrate the flexibility of this system. The bottom inset shows a top view micrograph of μs-Si dense microstrips (25-μm wide; ~2 μm spaced apart) cold welded on a thin Ti/Au coated Mylar sheet. (b) Current–voltage (I–V) characteristics of a device made with ribbons (25-μm wide) that remain on the surface of the SOI wafer (L=10 μm, W=390 μm). The inset shows an optical micrograph; several ribbons operate in parallel in this device. (c) A device made on a Mylar sheet coated with ITO gate and polymer dielectric. The semiconductor uses a 20-μm wide microstrip of single crystal silicon in a channel whose length is L=50 μm. The μs-Si in this case was patterned by solution cast. The transfer characteristics were measured at V_{DS}=0.1 V. The slope of this curve defines an effective device mobility (using the physical width of the source and drain electrodes, which is equal to the width of the μs-Si strip in this case) of 180 cm^2/V s. The inset shows an optical micrograph of the device.

substrate after etching of the Si but before lift-off. (Here the buried SiO_2 oxide acts as the dielectric and the silicon handle substrate acts as the gate electrode.) This result suggests that the processing steps used to produce the μs-Si and to transfer it to the device substrate do not alter significantly the properties of the silicon or its surfaces that result from the initial patterning and silicon etching steps. It also indicates that the van der Waals interface with the SU8 dielectric is capable of supporting good device properties.

This letter demonstrates a single crystal silicon-based approach to flexible electronic circuits on plastic substrates. Its main advantage is that it separates the crystal growth and processing of the silicon from the plastic substrate and other components of the devices. In that sense, it shares certain conceptual features with methods that use fluidic self-assembly (FSA) of fully formed silicon microchips onto plastic sheets.[26] The μs-Si method, however, is much more flexible in the processing sequences and in the materials choices that are possible. In that sense, it has strong similarities with conventional approaches (i.e., layer-by-layer) to flexible electronics. The wide range of geometries and material structures for the elements that make up the μs-Si make it possible to incorporate features that lie between the FSA and the layer-by-layer strategies. For example, an SiO_2 layer can be formed on one side of the silicon to yield an integrated dielectric, in a strategy similar to that for the integrated source/drain metallization demonstrated here. A current disadvantage of the technique is that although the SOI wafers are not specialty items, they are also not low in cost. We are currently exploring strategies for generating silicon micro/nanoelements without the use of SOI and we are seeking to apply these methods to other inorganic semiconductor materials.

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