Nanoscale organic transistors that use source/drain electrodes supported by high resolution rubber stamps

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Soft contact lamination and metal-coated elastomeric stamps provide the basis for a convenient and noninvasive approach to establishing high resolution electrical contacts to electroactive organic materials. The features of relief on the stamps define, with nanometer resolution, the geometry and separation of electrically independent electrodes that are formed by uniform, blanket evaporation of a thin metal film onto the stamp. Placing this coated stamp on a flat substrate leads to ''wetting'' and atomic scale contact that establishes efficient electrical connections. When the substrate supports an organic semiconductor, a gate dielectric and a gate, this soft lamination process yields high performance top contact transistors with source/drain electrodes on the stamp. We use this approach to investigate charge transport through pentacene in transistor structures with channel lengths that span more than three decades: from 250 μm to ~150 nm. We also report some preliminary measurements on charge transport through organic monolayers using the same laminated transistor structures. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1541941]

Recent interest in the science and the emerging applications of electroactive organic and bio-organic materials[1] motivates research into noninvasive methods for forming high resolution electrical contacts on these classes of ''soft,'' molecular materials. Many of the lithographic techniques that were developed for traditional microelectronic systems cannot be used because these organics are often incompatible with the required resists, developers, solvents, and exposure conditions. It was recently demonstrated that some of these problems can be avoided with the use of soft, conformable electrical contacts and lamination procedures.[2] Here we describe a related, but greatly simplified, approach that retains some of the important attractive features, eliminates the need for direct high resolution patterning of the electrodes, and enables transistor channels with lengths deep into the nanometer regime. This method exploits the surface relief on elastomeric stamps to define, with nanometer resolution, the geometry and separation of electrodes that are formed by directional deposition of thin metal films onto the stamps. Soft contact of these metal-coated stamps with the organic noninvasively establishes multiple independent electrical connections. The contact is reversible and it can be performed at room temperature and without applying pressure, adhesives, etc., that are generally used with traditional lamination or wafer bonding methods. This procedure provides a powerful tool for studying the physics of charge transport down to nanoscale dimensions in chemically fragile or ultrathin soft materials. Here we describe the method and demonstrate its use for investigating the electrical properties of thin film organic semiconductors in transistor structures with channel lengths that span more than three decades: from 250 μm to ~150 nm. We also present some results in transistors with self-assembled monolayers formed on the stamp-supported contacts.

Figure 1 presents a schematic illustration of this stamp-based lamination approach. It begins with the fabrication of high resolution rubber stamps (bilayers of two different types of the elastomer polydimethylsiloxane)[3,4] by casting and curing against photolithographically defined ''masters'' that consist of patterned resist (SU-8, Microchem Corp.; thickness between 5 and 15 μm) with vertical or reentrant sidewalls on silicon substrates. For the nanoscale transistors, we used patterns of resist (STR 1805, Shipley Corp.; thickness between 300 and 400 nm) produced with a near field photolithographic technique.[5] Exposing the stamps briefly (1–2 s) to an oxygen plasma forms surface hydroxyl groups. Electron beam deposition of Ti (1 nm; 0.3 nm/s) followed by Au (15 nm; 1 nm/s) with a flux of metal perpendicular to the surface of the stamp leads to deposition predominantly on the raised and recessed regions and not on the sidewalls. In this way, blanket uniform deposition yields patterned and

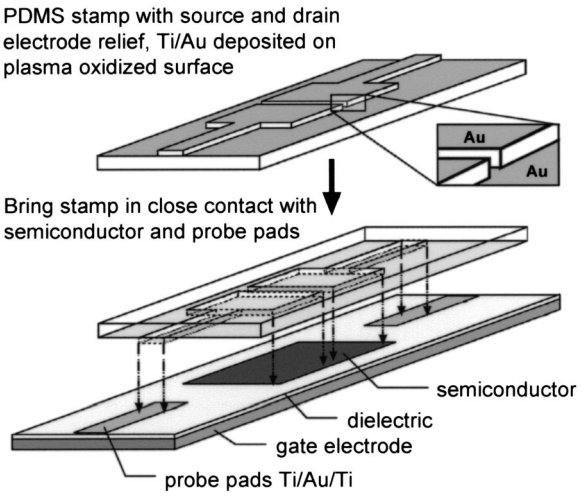

FIG. 1. Schematic illustration of steps for building thin film transistors by soft contact lamination with metal-coated rubber stamps.

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electrically isolated thin metal electrodes with the geometry and resolution of the relief structure. Films formed according to these procedures have good adhesion to the stamp and do not show the macroscopic cracking or rippling that can be observed in similar systems.[6]

Placing this type of metal-coated stamp onto a flat, smooth substrate leads to ''wetting'' that provides intimate contact between the two surfaces without the need to apply pressure, heat, etc. This phenomenon was recently exploited with stamps that had relatively thick and electrically continuous metal coatings to produce patterned electrets in thin polymer substrates.[7] To form top contact organic transistors with our discontinuous metal-coated stamps, we used a doped silicon substrate with a uniform 300-nm-thick layer of thermally grown SiO_2 (Process Specialties Inc.) and a thermally evaporated thin film of pentacene (25 nm thick, evaporated at 0.06 nm/s through a shadow mask with 2.5 mm $\times$3.0 mm rectangular openings). The silicon wafer serves as the gate electrode, the SiO_2 provides the gate dielectric, and the metal films on the raised regions of the stamp form the source and drain electrodes. Electron beam evaporated contact pads [trilayers of Ti (1 nm)/Au (40 nm)/Ti (30 nm)] on the SiO_2 connect to raised lines on the stamp. The transistors are probed by making source/drain contacts to these pads and a gate contact to a region of the silicon substrate where the SiO_2 is scratched away. For the nanoscale devices, we used a thin (26 nm) layer of chemical vapor deposited SiN_x as the gate dielectric and a doped silicon wafer as the substrate and gate. The stamps could be placed into contact with and removed from either type of substrate many times without any visible change or damage, or alteration in the electrical properties of the stamp, the pentacene or the resulting transistors. The stamps wetted the transistor substrates with very little or no applied pressure. Once in contact, the stamps remained in contact without applied pressure, until they were actively peeled away.

To establish the good performance of stamp-based laminated transistors, we compared their characteristics to control devices fabricated using the standard technique of evaporating gold top contact electrodes directly onto the semiconductor through a shadow mask. The channel widths and lengths and other geometrical features of the source and drain electrodes were exactly the same in the two types of devices: channel length $(L)=250\ \mu$m, channel width $(W)=5$ mm. The transistors were built on two adjacent areas (10 mm $\times$20 mm rectangular regions separated by 10 mm) of pentacene on a single substrate. Figure 2(a) shows some representative results. The stamp-based devices typically exhibited 20%–50% higher saturation currents (and, therefore, effective mobilities, μ_{eff}) than the shadow mask evaporated devices (Au, 50 nm thick deposited at 0.5 nm/s). There were no such systematic differences in the on/off ratios, which were (relative to a gate voltage of 0 V) in the range of 10^3–10^5. We also note that the electrical properties of the evaporated devices depend on the evaporation rate: the currents decrease by as much as a factor of 5 with decreasing evaporation rate between 1 and 0.1 nm/s. These observations suggest that deposition of metal can alter the organic semiconductor in a manner that affects the electrical properties of the transistor.

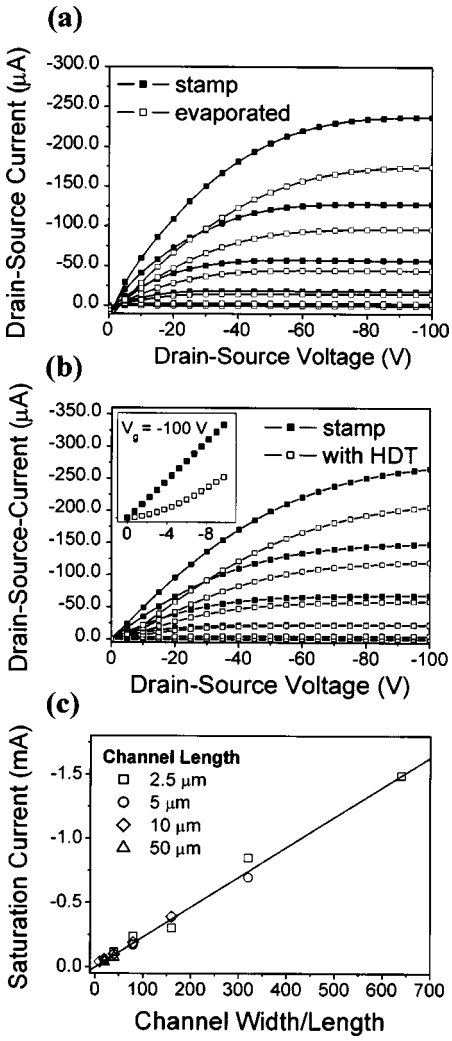

FIG. 2. Part (a) shows current–voltage characteristics of two top contact organic transistors: one of these uses soft contact of a metal-coated rubber stamp to define the source/drain electrodes (stamp) and the other uses contacts evaporated directly on the semiconductor through a shadow mask (evaporated). Part (b) shows current–voltage characteristics of transistors formed with stamps that have bare gold coatings and those with gold coatings and a self-assembled monolayer (SAM) of hexadecanthiolate (HDT). Part (c) shows saturation currents measured at a gate voltage of 80 V in 17 different devices characterized by a wide range of channel widths and lengths.

This result highlights the comparatively noninvasive nature of the laminated contacts.

To demonstrate the suitability of this same laminated test structure for investigating the properties of charge transport through organic monolayers, we built stamp-based devices with a bare gold coating and one with a self-assembled monolayer on the gold formed by contacting the stamp against a flat piece of polydimethysiloxane (PDMS) that was ''inked'' with a 2 mM solution of hexadecanethiol (HDT) in ethanol. Figure 2(b) shows the current–voltage characteristics; the inset shows the behavior in the linear regime at a gate voltage of -100 V. The stamp treated with the HDT layer shows strongly nonohmic behavior, due to the tunneling barrier formed by the self-assembled monolayer (SAM). The device formed with the bare gold, on the other hand, shows purely ohmic behavior and higher saturation currents. The difference between the behavior of these two devices reveals the electrical influence of the monolayer. Quantifying

these differences and relating them to molecular structure is the focus of current work.

The relatively tow parasitic resistances in the bare gold stamp devices can also be observed by measuring transistor properties as a function of channel length. Since the stamps can easily be contacted and then removed from the substrate without affecting the stamp, the substrate, or the semiconductor, it is possible to build multiple devices (consecutively, one after another) on a single region of pentacene. This capability makes it possible to test accurately the electrical properties of transistors as a function of channel length and width, with a precision that is not limited by spatial variations in the properties of the semiconductor (or other components of the devices). Figure 2(c) shows the measured saturation currents from stamp-based transistors with a wide range of *W*'s and *L*'s formed on a single small region of pentacene (1 mm$\times$2 mm). The data illustrate a remarkably good linear scaling of the current with the ratio *W/L* for channel lengths ranging from 50 to 2.5 μm and channel widths from 2 mm to 100 μm. They suggest that the stamp-based approach yields devices that are free of measurable artifacts in this range of geometries. (It is difficult to fabricate devices that are free of contact related artifacts over this wide range of geometries using other approaches for depositing and patterning the contacts.) They also indicate that the effective mobilities of these transistors are independent of *W* or *L* over this wide range. For the devices shown here, which use unpurified pentacene deposited onto substrates at room temperature, the mobilities computed in the saturation regime are 0.06 ± 0.01 cm^2/V s.

The results of Fig. 2(c) represent a broad and systematic set of measurements on top contact organic transistors with channel lengths in the micron range. These data indicate that all of the devices display the expected physics and current scaling with *W* and *L*. At channel lengths and widths that are comparable to or smaller than the grain size ($\sim$300 nm) in the pentacene films, different behavior might be expected. Bottom contact organic transistors with $\sim$100 nm channel lengths[8] and top contact devices with channels shorter than $\sim$200 nm[9] both showed reduced effective mobilities and on/off ratios compared to micron-scale devices. Interpretation of those results was complicated, however, by the differences between semiconductor film growth at the edges of the electrodes and at the center of the channel[10,11] in the case of the bottom contact devices and exposure of the semiconductor to electron beam patterning processes for the top contact systems. Laminated top contact devices are of interest partly because they avoid these issues entirely. Figure 3 shows results from a stamp-based transistor with a channel length of $\sim$150 nm, which represents a dimension that cannot be achieved with our other related lamination method.[2] Here relief on the stamp defines the channel length, and microcontact printing defines the channel width (20 μm). The etching step in the printing process eliminates gold from the recessed region of the stamp at the channel location. The results indicate lower mobilities ($\sim$5 times lower, as approximated by the dependence of currents measured at source/drain voltages

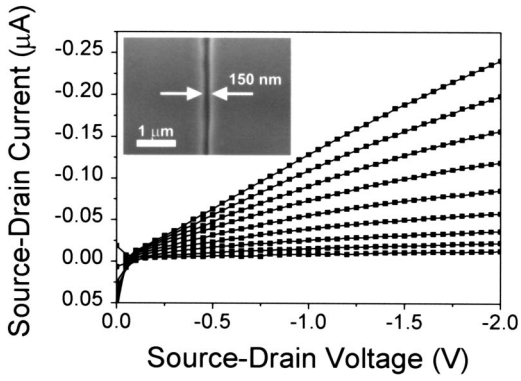

FIG. 3. Current–voltage characteristics from a nanoscale organic transistor formed by soft contact of a metal coated stamp with a thin semiconducting film of pentacene on a dielectric layer of SiN_x (26 nm) on a doped silicon substrate. The gate voltage varies between $+1.0$ and -2.2 V in steps of 0.4 V. The channel length of this device is $\sim$150 nm. The inset shows a scanning electron micrograph of the separation between the source and drain electrodes on the stamp.

of -2.0 V for different gate voltages) and on/off ratios ($\sim$10 times lower) in these nanoscale devices compared to stamp-based devices with 2.5 μm channel length and 100 μm channel width formed on the same region of pentacene and with the same substrate. These differences may be due partly to intrinsic parasitic resistances in these top contact geometries. They may also be due to some mild short channel effects, which might be present at some small but non-negligible level in these nanoscale devices (i.e., ratio of channel length to dielectric thickness is $\sim$6). Our current efforts are directed toward a systematic investigation of electrical characteristics of organic transistors with a range of submicron channel lengths. The results presented in this letter demonstrate that the soft contact stamp based approach for building the necessary devices will be useful for these studies. More generally, the simplicity of this approach, its capability for nanometer resolution, and its compatibility with a wide range of fragile soft materials and even with organic self-assembled monolayers suggest a strong potential for its use in measuring charge transport through unconventional materials that are difficult to process with standard methods.

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