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Deterministic assembly of CMOS microchips is demonstrated as a promising route to 3D, heterogeneously integrated microsystems, in which biodegradable components sourced from commercial semiconductor foundries are employed as building blocks, to enable functional transformations by controlled transience based on coupled physical and electrical processes. Demonstration examples range from logic gates and analog circuits to multilayer systems that undergo multistage transformation, as discussed in article number 1704955 by John A. Rogers and co-workers. Image designed by Jan-Kai Chang.

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Biodegradable Electronic Systems in 3D, Heterogeneously Integrated Formats

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Biodegradable electronic systems represent an emerging class of technology with unique application possibilities, from temporary biomedical implants to "green" consumer gadgets. This paper introduces materials and processing methods for 3D, heterogeneously integrated devices of this type, with various functional examples in sophisticated forms of silicon-based electronics. Specifically, techniques for performing multilayer assembly by transfer printing and for fabricating layer-to-layer vias and interconnects by lithographic procedures serve as routes to biodegradable, 3D integrated circuits composed of functional building blocks formed using specialized approaches or sourced from commercial semiconductor foundries. Demonstration examples range from logic gates and analog circuits that undergo functional transformation by transience to systems that integrate multilayer resistive sensors for in situ, continuous electrical monitoring of the processes of transience. The results significantly expand the scope of engineering options for biodegradable electronics and other types of transient microsystem technologies.

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Transient electronic systems represent an unusual class of semiconductor technology, defined by a capacity to disintegrate, physically transform or vanish at predictable rates upon activation of trigger stimuli or exposure to certain environmental queues.[1–3] Interest in this emerging field follows from possibilities for broad types of applications that cannot be addressed with traditional, i.e., nontransient, forms of electronics. Examples range from environmentally/biologically degradable platforms for "green" consumer devices and temporary biomedical implants, to digital data storage systems with hardware-based security features, to remote environmental monitors that avoid the need for recovery and disposal.[4–8] Demonstrated material options for transient electronics include specially formulated organics (e.g., hygroscopic polymers, cellulose-based biomaterials), certain classes of metals (e.g., Mo, W, Mg, Zn) and high-performance inorganic semiconductors (e.g., Si, Ge, ZnO), a variety of thin film dielectrics and encapsulation materials (e.g., SiO_2, Si_3N_4, MgO, polyanhydrides), and biodegradable substrates (e.g., silk proteins, organic polymers).[9–17] Recent reports describe system level examples that span implantable sensors for physiological monitoring and vehicles for programmed drug release, harvesters for converting mechanical into electrical power, and photodetector arrays for capturing digital images.[14,18–21] Here, all of the constituent materials dissolve entirely, at controlled rates and times, in body fluids or ground water, with benign end products.[16–22] In some of these cases, such as intracranial/intrathoracic sensors, advanced schemes in integration allow deployment of prefabricated device components onto separately processed, flexible bioorganic substrates where they can be subsequently interconnected to provide desired function at the system level.[8,18,21]

An important recent finding in this context is that certain materials and processing methods for these technologies can be aligned with those in modern integrated circuits, thereby affording opportunities to leverage existing silicon complementary metal-oxide-semiconductor (CMOS) foundries for cost-effective production of high-performance devices with sophisticated modes of operation.[5,23,24] In all previous works, a single active layer supports a planar, 2D configuration of constituent transient microcomponents and dissolvable interconnects. The layouts and/or encapsulation layers define the functions and lifetimes.[9–11,23] 3D multilayer designs offer opportunities to

bypass engineering constraints and performance limitations associated with such 2D geometries. In fact, 3D heterogeneous integration for system-on-chip technologies represents one of the most promising routes to enhanced functionality in conventional electronics, where the third dimension provides the ability to accommodate growing demands in integration density, at given lithographic design rules.[25–28]

Traditional routes to 3D integration rely on epitaxial growth or wafer/wire bonding.[29,30] Alternative methods based on transfer printing exploit additive assembly of micro/nanomaterials or devices into heterogeneous material layouts enabled by the soft, nondestructive mechanics of the transfer process and its room temperature operation.[26,31–34] Compatibility with organic materials and substrates, and with certain levels of nonplanar topography, follows naturally. These features are critically important for transient electronics, where diverse materials with disparate properties and processing thermal budgets (PTBs) must be combined together.[18,23,24] Specifically, 3D integration via transfer printing involves vertical stacking of thin, functional elements prefabricated in whole or in part on separate substrates, thereby avoiding constraints associated with PTBs in bottom-up, growth-based strategies.[25–30,35] Materials and device components with lateral feature sizes and thicknesses as small as a few nanometers and with dimensions as large as several millimeters can be manipulated in this manner, with throughputs, at scales and over areas that cannot be reproduced with even the most sophisticated, robotic pick-and-place tools.[25–27,34–36] Compared with conventional through-silicon via technologies that exploit silicon interposers, solder balls, and high aspect ratio vertical interconnects, the overall thicknesses of 3D stacks formed by transfer printing can be as small as a few microns or less, thereby allowing use of lithographically processed thin films as interconnects and dielectrics.[37,38]

Early research in this direction involved nanomaterials, such as carbon nanotubes and inorganic semiconductor nanowires, as the basis for 3D nanoelectronic systems.[26,27,35] The most recent results exploit carbon nanotubes integrated with silicon CMOS, where computing, data storage, and signal transfer occurs in a single 3D chip, thereby suggesting a path toward future power efficient, high-speed, data-intensive devices.[39,40]

The work presented here introduces adaptations of these basic approaches for use in transient platforms in which multilayer stacks of biodegradable high-performance metal-oxide-semiconductor field-effect transistors (MOSFETs) integrate into thin, 3D interconnected layouts on polymeric substrates. Demonstrations include systems that undergo multistage physical transformation in function as a result of physical and electrical layouts that lead to consecutive or interlaced dissolution. 3D analog devices capable of varied levels of amplification and digital circuits that transform from AND to NAND gates are possible, in flexible, biodegradable formats. Additional illustrations include stacks in which water-soluble interlayers and sensors define timescales for physical disintegration, in a way that allows for continuous, in situ electrical monitoring of the processes of transience. These and other capabilities qualitatively extend design options in transient electronics, with implications for broad classes of related microsystems, from optoelectronics, to photonics, chem/biosensors, and microelectromechanical devices.

The results described in the following exploit transient microelectronic components derived from silicon on insulator (SOI) wafers processed in a nontraditional way in a commercial foundry (**Figure 1**a).[24] Key constituent materials include Si, SiO_2, and Si_3N_4, each of which reacts in a biocompatible manner with water to form benign end products ($Si(OH)_4$ and NH_3), and tungsten, which undergoes hydrolysis according to $2W + 2H_2O + 3O_2 \rightarrow 2H_2WO_4$.[16,17,41–44] Here, anisotropic etching of the underlying wafer with the buried oxide layer as a backside etch stop, followed by transfer printing allows delivery of ultrathin, high performance, functional microcomponents as transient building blocks for systems constructed on foreign substrates. When implemented in a step and repeat fashion, this scheme allows distributed functionality over large 2D areas and/or in stacked configurations, with spatial layouts that are decoupled from the original distributions of the microcomponents on the source wafer (Figure 1c).

The sequences for integration and assembly appear in **Figure 2**, starting with on-wafer processing to yield releasable microcomponents (Figure 2b) and ending with post-transfer interconnection and encapsulation Figure 2c). A film of SiN_x (≈700 nm) coated conformally on the source wafer by plasma-enhanced chemical-vapor deposition (PECVD) serves as a passivation layer. Inductively coupled plasma (ICP) reactive ion etching (RIE) of the underlying interlayer dielectric in regions between the microcomponents defines trenches that delineate the areas targeted for release. These trenches leave small regions at the corners as physical tethers, or anchors, to retain the positions and orientations of the microcomponents during anisotropic etching of the underlying silicon by immersion in tetramethylammonium hydroxide (TMAH, 8.3 wt% at 85 °C). Transfer printing using stamps of poly(dimethylsiloxane) (PDMS) enables removal and delivery of selected collections of these microcomponents (total thickness of ≈3 μm) onto target substrates, in this case a Si wafer coated with poly(lactic-*co*-glycolic acid) (PLGA) (>50 μm). A set of scanning electron microscope (SEM) images collected at key stages of this process appears in Figure 2b.

Spin casting a planarizing overcoat of PLGA yields a biodegradable interlayer dielectric. Photolithographically defined openings created by RIE expose contact pads on the underlying microcomponents. The thin geometry of the PLGA coating allows formation of interconnects and vias by use of conventional thin film processing techniques. Applying another overcoat of PLGA and performing a similar sequence of steps yields an additional functional layer of interconnected microcomponents, with a collection of electrical contacts to the underlying layer. Printing at temperatures slightly above the glass transition of the PLGA yields sufficient tackiness to receive printed microcomponents at high yields.

Continuing this sequence can extend the layered structure to stacks of eight layers (and potentially more), with registration accuracy at the micron scale, limited mainly by mechanical aspects associated with the transfer printing tool (Figure S1, Supporting Information, ≈1 μm for the system reported here) and deformations of the softened PLGA, as opposed to distortions associated with the elastomeric stamp. Examples of integrated microsystems in 3D configurations appear in Figure 2c. Extending this stacking process beyond the results shown here

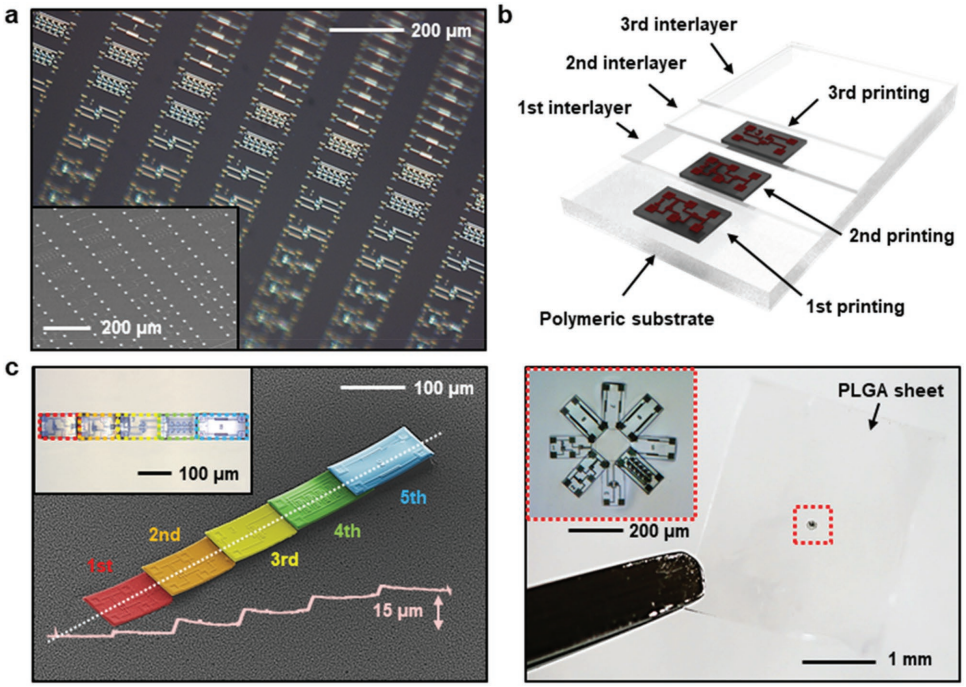

Figure 1. 3D deterministic assembly of transient electronic microcomponents into heterogeneously integrated systems with stacked layouts. a) Optical micrograph of arrays of CMOS microcomponents on a 6 in. source wafer and magnified SEM image (inset) of representative devices. b) Schematic illustration of a 3D stacked assembly on a polymeric substrate. c) SEM image (left; inset: optical micrograph) and optical images (right; inset: magnified view) of 3D stacked microchips on thin sheets of PLGA. Surface profilometry indicates a height of ≈15 μm for these five layer stacks. Each layer is offset/tilted and colorized to facilitate viewing.

will require improved control over the transfer mechanics to minimize lateral motions and variations in contact force, both of which can lead to unwanted displacements and/or fracture of fragile components, especially in the presence of nonplanar features on the receiving substrate.

The versatility of this approach provides access to diverse classes of 3D biodegradable systems. **Figure 3** presents an example designed for functional transformation from logical AND to logical NAND upon dissolution of certain upper layers in the stack by immersion in phosphate buffer solution (PBS, pH 7.4) at 70 °C for 24 h. These logic circuits (Figure 3a) consist of n-channel MOSFET (NMOS) and p-channel MOSFET (PMOS) pairs for the lower layer NAND gate (left), a CMOS inverter as the upper layer for logical negation (middle), and two layers of tungsten traces (300 nm thick) for interconnection. Corresponding electrical characteristics of each constituent device appear in Figure 3b. The performance is consistent with that obtained from unprocessed devices on the source wafer (on/off ratio of $> 10^7$ and threshold voltage V_{th} of ≈ -1.1 V for PMOS; on/off ratio of $> 10^8$ and V_{th} of ≈1 V for NMOS; DC gain of ≈25 at supply bias of 3 V for CMOS). Figure 3c presents circuit diagrams and switching waveforms, where V_A and V_B correspond to the input voltages, V_{DD} is the supply voltage (3 V) and Out_2 and Out_1 indicate output voltages before and after transience, respectively.

During dissolution in PBS, the upper functional layers (i.e., CMOS inverter, W interconnects, and PLGA interlayer) dissolve/disintegrate gradually, beginning with W interconnects over a period of ≈1 h, and concluding with delamination of the CMOS inverter after ≈24 h. During this period, the NAND circuits on the lower layer remain unchanged. The result transforms the function from AND (Figure 3c, middle) to NAND logic (Figure 3c, right).

3D transient analog devices that undergo functional transformation are also possible. **Figure 4** shows a transient cascode amplifier (Figure 4a, left) with a microcapacitor (Figure 4b, left) on an overlying layer (Figure 4a, right) connected through aligned vias (Figure 4b, right). Figure 4c presents the frequency response of this circuit in its initial state, showing gains of up to 4.1 at low frequencies and attenuated signals over the corner frequency of 6 kHz. Dissolution of the upper layer leads to disintegration of the filter microcapacitor in a way that alters the characteristics of the amplifier. A circuit schematic (Figure 4d, left) and set of switching waveforms Figure 4d, right) highlight the system architecture and corresponding changes in the electrical function, respectively. Specifically, the operation transforms from that of a low-pass resistor–capacitor (RC) filter to a cascode amplifier. Dissolution changes the output voltages at 1 MHz from attenuation by >30 dB (Out_2) to amplification by a gain of ≈4 (Out_1) under supply voltage (V_{dd}) and bias (V_{bias}) levels of = 3 V. A large load resistance R_L of 56 kΩ enables outputs with high voltage gains (A_v) according to $A_v = -g_m R_L$, where g_m is the transconductance of the constituent transistors. The transfer characteristics (left) and output voltage response (right) of the cascode amplifier that results from transformation appear in Figure 4e; the voltage gain is ≈4 when the input AC signals have a DC bias of 1.8 V and a peak-to-peak amplitude of 100 mV.

In these systems, the PLGA serves as the interlayer dielectric; its transience, through hydrolytic degradation and mechanical disintegration, determines the timescale for functional

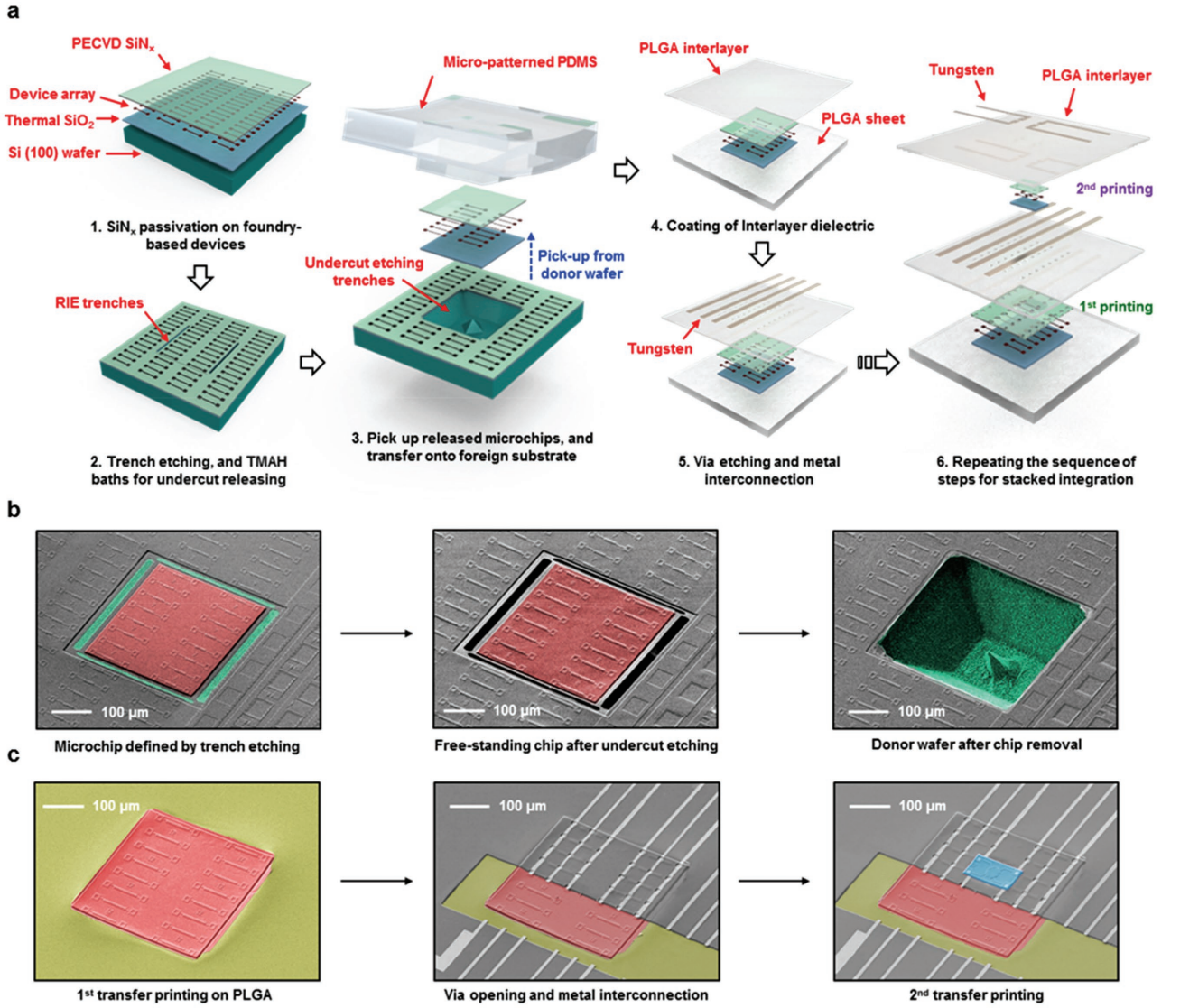

Figure 2. Release and assembly of fully formed transient electronic microcomponents via several cycles of transfer printing. a) Schematic illustration of the processing steps and structural configuration of a 3D interconnected platform. Planarizing layers of PLGA serve as adhesives and interlayer dielectrics to facilitate 3D heterogeneous integration. b) SEM images of the steps for releasing an array of diodes, shown in sequence from left to right. c) SEM images of this same array after printing onto a PLGA substrate (left), after forming interlayer coats and metal interconnects (mid), and after printing a second (top) layer Hall plate (right). Etching openings in the PLGA interlayers enables imaging of the underlying devices. The colorized regions correspond to the released microcomponents (red), the Si handle wafer (cyan), the PLGA receiving substrate (yellow), and the secondary printed microchip (blue).

transformation. The ratio of lactic acid to glycolic acid used to form the polymer, together with the molecular weight, block structure, and crystallinity, are the most critical determinants of the relevant properties.[45–47] The dielectric characteristics and hydrolysis kinetics for PLGA with various composition ratios appear in **Figure 5**a–c. Here, alternating current (AC) measurements on a metal–insulator–metal (MIM) capacitor ($A \approx 50 \times 100\ \mu m^2$) yield the relative permittivity as a function of frequency $\varepsilon_r(\omega)$, according to $C_{MIM} = \varepsilon_0 \varepsilon_r(\omega) A/t$ where ε_0 is the vacuum permittivity and t is the film thickness. Figure 5a shows that $\varepsilon_r(\omega)$ of PLGA (M_w of 50 000–75 000; Sigma-Aldrich) with different lactide:glycolide compositions lies between 2.9 and 2.6. The variations with content of glycolide units can be attributed to asymmetric polarity associated with the polar carbonyl constituent (i.e., ester groups).[48–50] These values are consistent with the amphiphilic nature of PLGA and are comparable to those of common spin-on polymeric dielectrics such as benzocyclobutene ($\varepsilon_r \approx 2.7$), slightly larger than that of polynorbornene ($\varepsilon_r \approx 2.2$ to 2.4) but smaller than polyimide ($\varepsilon_r \approx 3.1$ to 3.5).[51,52] By comparison to SiO_2 at similar thicknesses, PLGA offers reduced RC delays and AC power dissipation ($\propto CV^2 f$, where C is the interconnect capacitance, V is the applied voltage, and f is the frequency of the applied voltage).[53]

The effects of hydrolysis of PLGA (85:15) interlayers at several stages of immersion in PBS (pH 7.4) at physiological temperatures (37 °C) appear in Figure 5b. Gradual hydrolysis

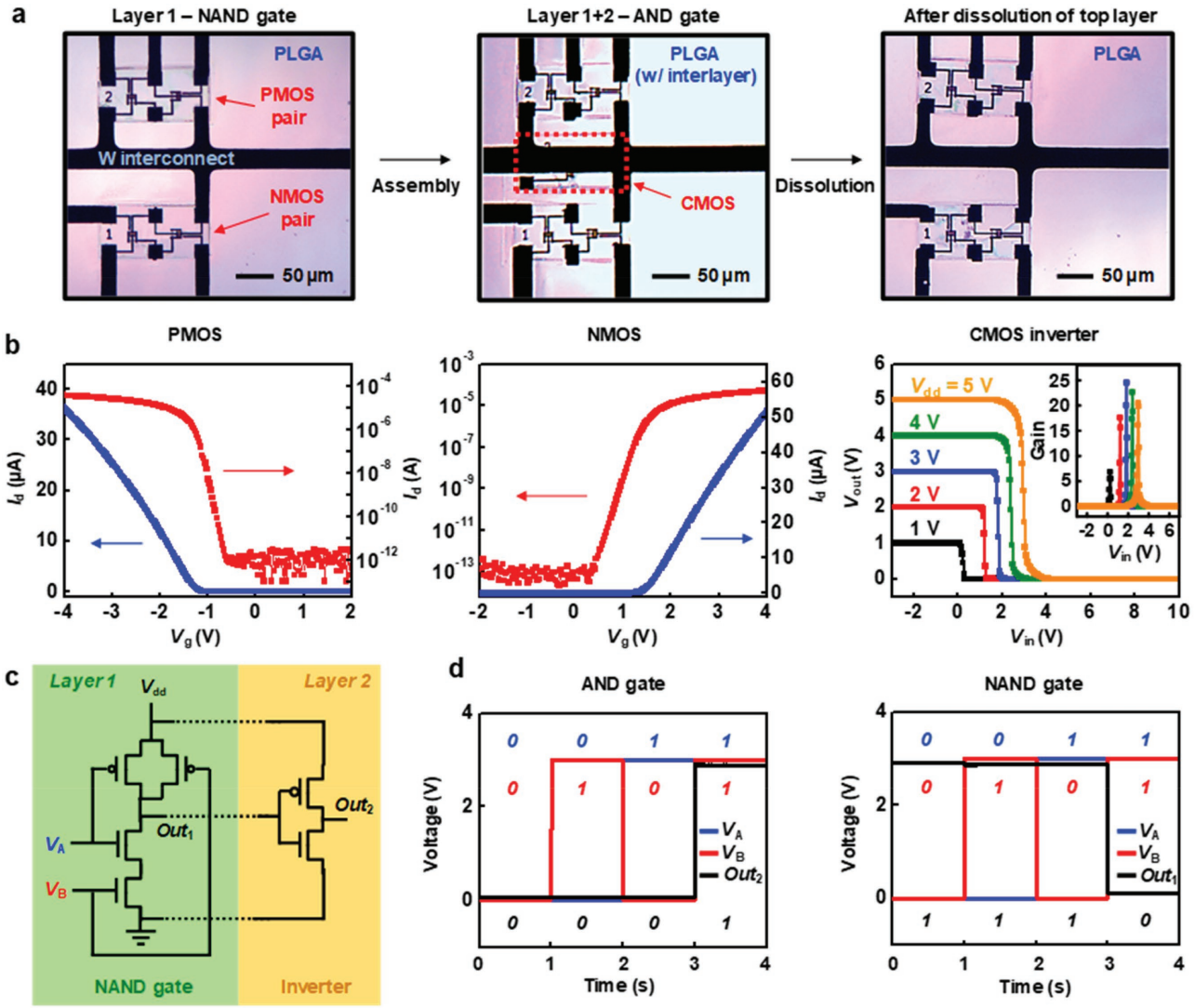

Figure 3. Functional transformation in 3D transient CMOS logic gates. a) Optical images of the layered structure of 3D transient logic gates, before stacking (left) and after transformation from an AND gate (mid) to a NAND gate (right) by dissolution of the inverter on the second (top) layer. b) Linear and log scale plots of the transfer curves of a representative PMOS (left) and NMOS (mid) pair that forms the NAND gate on the first (bottom) layer. The right panel shows voltage transfer curves and gain characteristics of the CMOS inverter on the second layer. c) Circuit schematic of the 3D transient AND gate. The NAND gate implemented on the lower layer follows from combining the NMOS and PMOS pairs with layer-to-layer interconnects (dash line) to an overlying CMOS inverter for the AND logic function. d) Switching waveforms for the 3D transient logic gate before (AND, left) and after (NAND, right) transformation by dissolution. V_A, V_B are the input voltages, and V_{dd} is the supply voltage (3 V).

of underlying serpentine traces of Mg (Figure 5b, left) suggests that water penetrates through the upper PLGA interlayer within the first 45 min. Simultaneous hydrolysis and swelling by water uptake give the initially transparent film an opaque, white appearance.[54,55] Losses in weight are >20% after 10 d of immersion (Figure 5b, right). These results indicate collective processes of diffusion with bulk and surface erosion, in which the effective diffusivity of PLGA interlayers obtained from experiments ($\approx 1.2 \times 10^{-4}$ μm^2 s^{-1} by assuming an approximate reaction constant of 5×10^{-4} s^{-1} inferred from published data and analytical model reported by Li et al.) is consistent with literature reports (10^{-6}–10^{-4} μm^2 s^{-1}, corresponding to diffusion through PLGA in its solid phase).[56–61] Atomic force microscope (AFM) characterization for a representative patterned plateau of PLGA (Figure 5c) highlights associated volumetric details through changes in topography before and after immersion; swelling by water uptake leads to 13.5%–21% increases in volume. The primary effect of these processes on transience in electronic function follows from loss of mechanical integrity and associated fracture of interconnects and vias.

Figure 5d presents a sequence of SEM images collected during dissolution of bilayer stacks of microcomponents with PLGA (85:15) interlayers due to immersion in PBS. Physical changes are consistent with nonuniform hydrolysis and dissolution, resulting in overall disintegration. First, the microcomponents on the top-layer dissolve and disintegrate themselves, in a manner consistent with previous reports.[16,24] Specifically, the layered inorganic constituent materials decompose

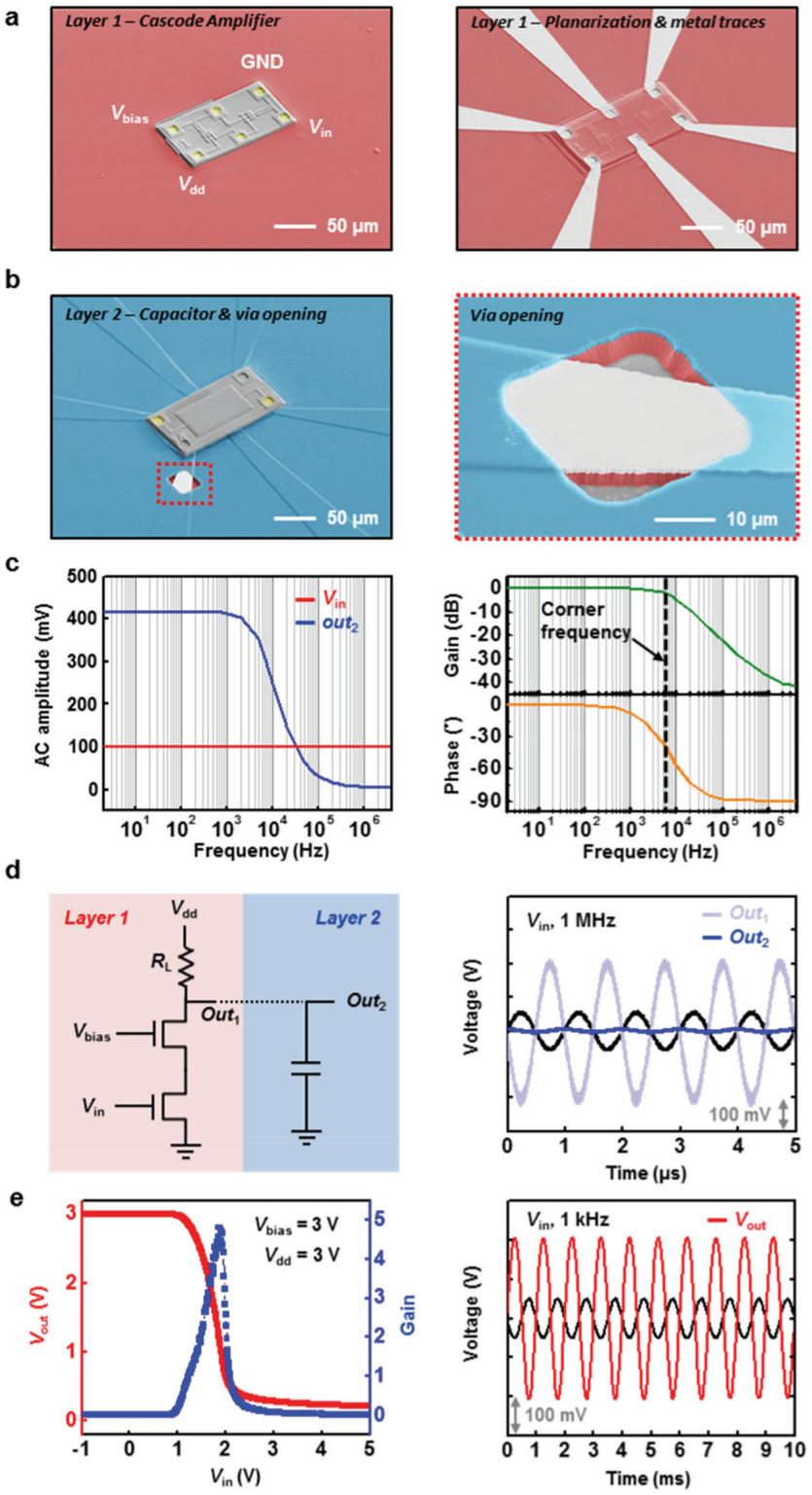

Figure 4. 3D transient analog circuits designed for controlled transformation in function. a) SEM images of a cascode amplifier (left) printed on a sheet of PLGA, planarized with an additional coating of PLGA and interconnected to yield the first functional layer (right). The cascode amplifier consists of two interconnected body-tied H-type MOSFETs, preferred for analog applications. b) SEM images of a representative capacitor (left) printed over the first layer, with a via through the PLGA interlayer (right) for vertical interconnection. SEM images are colorized for ease of viewing (yellow: metal pads; red: first-tier structure; blue: second-tier structure). c) Frequency response (left) of 3D amplifier circuits that drive function for the low-pass filter before transformation. A corner frequency of 6 kHz for the first-order filter can be derived from the gain and phase response (right). d) Circuit schematic of 3D amplifier circuits (left) and corresponding input and output waveforms (right) with R_L = 56 kΩ at 1 MHz input for different stages of functional transformation by dissolution (out_2: initial state; out_1: after disintegration of upper layer capacitor). The input voltage has a DC bias of 1.8 V with an AC peak-to-peak amplitude of 100 mV. e) Voltage transfer characteristics (left) of cascode amplifiers after transformation and corresponding switching waveforms (right) at 1 kHz input. The DC bias and AC amplitude are similar to that in (d) to enable high gain outputs.

uniformly and gradually at a molecular level, starting from structural edges and propagating to other regions on a layer-by-layer basis. Complete disintegration follows from delamination of device residues, as determined by fast swelling and associated fracture of the PLGA interlayer rather than by slow dissolution of the buried oxide (BOX) (i.e., thermal SiO_2).[5,24] The bottom active layer dissolves in a similar but more random manner, depending on the spatial distribution of overlying PLGA residues. By consequence, immersion in PBS eliminates everything across the entire 3D system by successive dissolution through the thickness. Engineering control over the interlayer is critically important in determining the timescales for system-level transience and any associated staged transformation in function.

3D configurations in transient devices also offer capabilities for continuous electrical monitoring of the system disintegration. **Figure 6** shows an example in which transient sensing elements at different interlayers provide in situ indications of the progress of disintegration and dissolution. In this simple example, stacked transient resistors interconnected in parallel give a total resistance of $R_{network}$, as in Figure 6a. Here, polysilicon microresistors with resistances of 1.25 and 2.5 kΩ (Figure 6b) appear on alternating layers (i.e., 1.25 kΩ for the 1st layer, 2.5 kΩ for the 2nd layer, 1.25 kΩ for the 3rd layer, and 2.5 kΩ for the 4th layer) to form a four-stage resistive tracking system ($R_{network}$ = 416.67 Ω) with a total thickness of ≈15 μm. The thickness of a single interlayer (PLGA 85:15 in this case) can be as small as 100 nm and that of a single active layer (i.e., including PLGA interlayers, 300-nm-thick metal interconnects, and 3-μm-thick microcomponents) is ≈3.5 μm for the examples described here

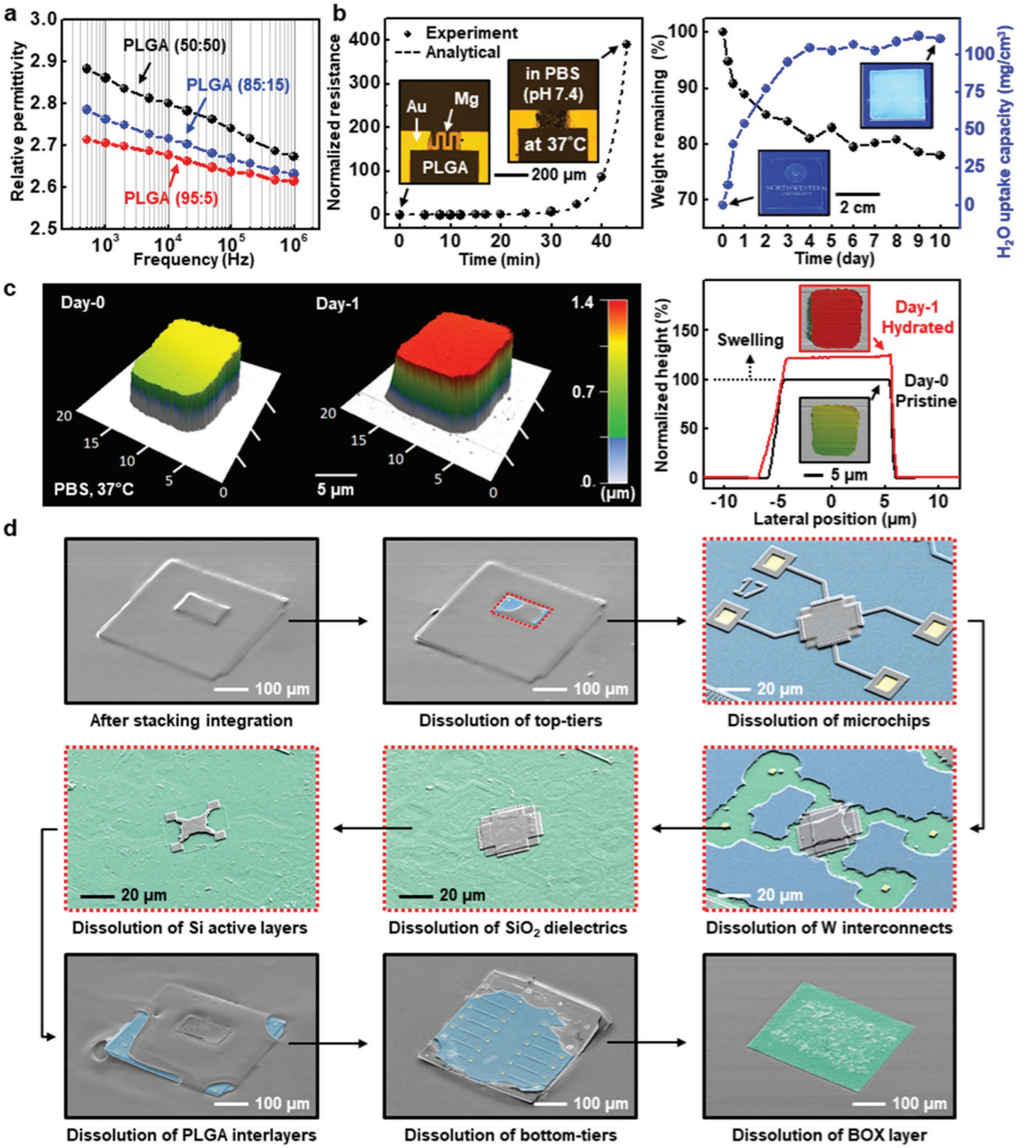

Figure 5. Dissolution characteristics of films of PLGA and kinetics for transience of 3D transient electronics immersed in PBS (pH 7.4) at 37 °C. a) Experimental results for relative permittivity of PLGA with different monomer ratios (lactic acid: glycolic acid). b) Water permeation (left) and hydrolysis kinetics (right) of PLGA (85:15) interlayers, as determined by the time evolution of the resistance of an underlying thin film trace of Mg and of the overall weight, respectively. Insets show optical images before and after soaking. c) AFM topographical images and corresponding profiles (inset: top view) of a patterned plateau of PLGA (85:15) before (black, day 0) and after soaking (red, day 1). d) Time sequence of SEM images for 3D transient electronics at various stages of disintegration (colorized according to different sections; blue: printed microchips, yellow: metal pads, cyan: BOX layer).

(Figure 6c). The tracking system disintegrates in PBS (pH 7.4) at 37 °C, leading to a step-wise set of increments in $R_{network}$ over the course of dissolution. Figure 6d shows the time evolution of $R_{network}$ and corresponding changes in the 3D resistive tracking system as a result of progressive disconnection of the resistive components. Four, separately staged changes in electrical

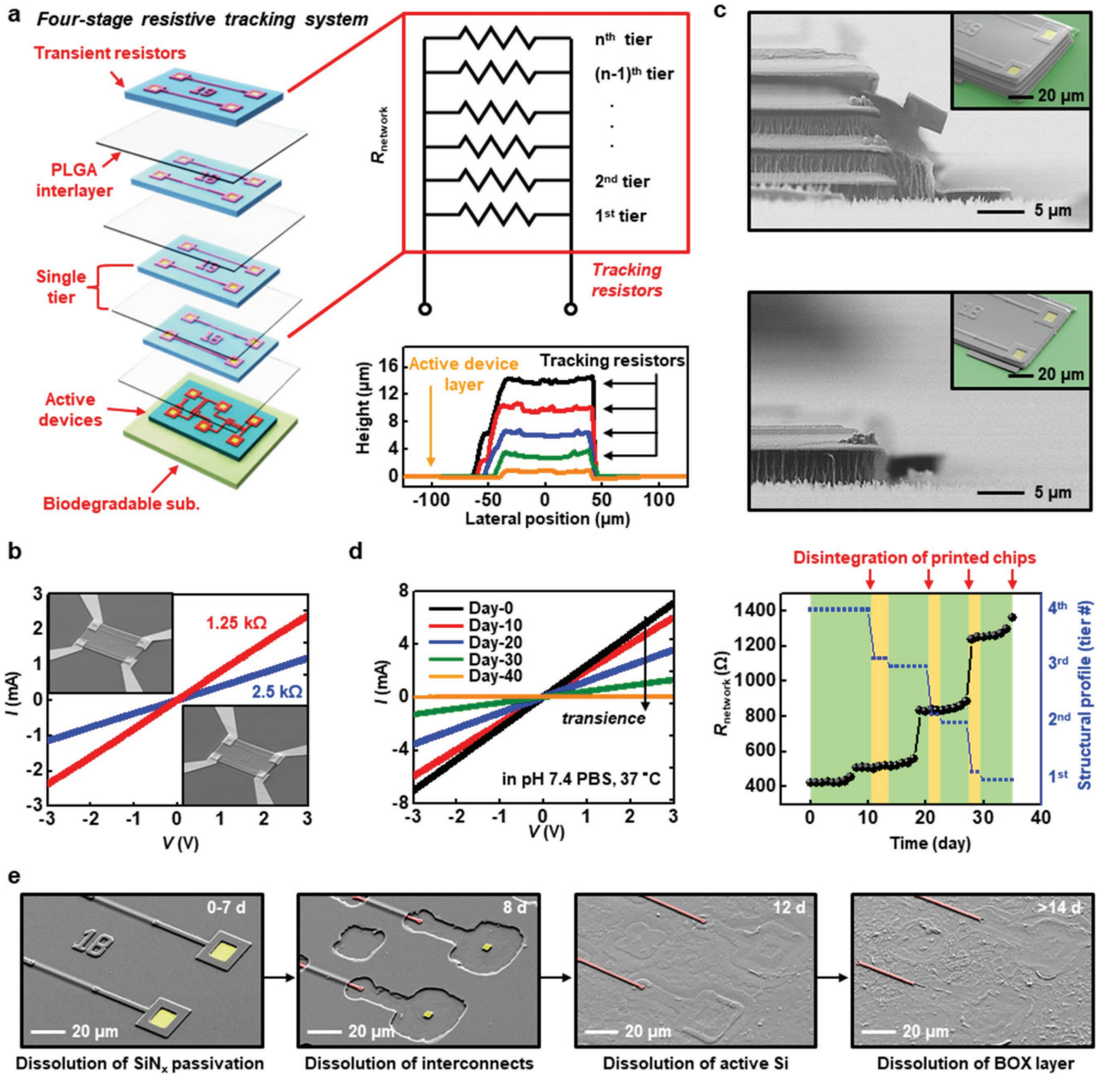

Figure 6. Resistive sensors for temporal monitoring of processes of transience in a stacked 3D electronic system. a) Schematic illustration (left) and circuit schematic (top right) of a four-stage resistive tracking system integrated with active transient circuits. Corresponding profiles of the stacked resistive microcomponents showing a height of ≈15 μm for the entire system (bottom right). b) Electrical characteristics of transient microresistors that serve as sensors. c) SEM cross-sectional images of these same stacked microchips (top: four-layer stack; bottom: single-layer stack). Embedded microcomponents exposed by oxygen plasma etching for ease of viewing, showing thicknesses of ≈100 nm for the interlayers. d) Functional transience (left) and corresponding time evolution (right) of a four-stage resistive tracking system in PBS at 37 °C. Colored domains represent dissolution of different components (green: printed microresistors; yellow: PLGA interlayers). Red arrows indicate the times at which a microresistor delaminates. e) SEM images at various stages of dissolution of transient microresistors under the same conditions. SEM images are colorized for ease of viewing (yellow: metal pads; red: polycrystalline Si).

properties at different timescales and subsequent chip delamination suggest unique kinetics for disintegration of each layer. The implication is that dissolution of constituent materials or loss of printed microcomponents leads to functional transformation. Dissolution of the uppermost microresistor defines the first stage, in which rapid changes in $R_{network}$ occur by consequence of dissolution of the top resistive component (i.e., sequential dissolution of SiN_x passivation, SiO_2 interlayer dielectric, and W interconnects of the microresistor). The timescale for stable operation of an exposed microresistor under these conditions is ≈7 d (Figure 6e). Similar kinetics define the second stage, in which degradation of the overlying PLGA

interlayer slightly delays the functional transience. The third stage involves fracture of the printed microresistor due to swelling of the PLGA interlayers; hence, the functional time period at this stage is governed by swelling strains and associated fracture, rather than by dissolution. Finally, delamination of the microresistor on the lowest layer terminates resistive operation of the tracking system, followed by performance degradation of the underlying active circuits within 2 d. Decreased operational timescales for the lower layers suggest that dissolution of the 3D system occurs in a nonuniform fashion, with leakage/diffusion of water through the supporting PLGA interlayers and complete loss of mechanical integrity in the 3D layered system. Improved lifetimes and/or control in transience might be possible through combined use of impermeable materials (e.g., Si) and/or biofluid barriers (e.g., thermal SiO_2, Si_3N_4, HfO_2).

In conclusion, the concepts introduced here allow biodegradable 3D integrated electronics by transfer printing, with demonstrations using foundry-based microcomponents. The resulting strategy in stacked microscale deterministic assembly enable high packing density, condensed footprint, and enhanced functionality compared to traditional 2D layouts. The thicknesses and compositions of the interlayer dielectrics, along with the overall system geometries, lead to controlled transience due to coupled physical and electrical processes. Examples, from digital logic gates to analog amplifiers, illustrate some of the possibilities in multistaged transformation and high-performance operation. The core ideas can be extended to other types of advanced electronic circuits, and to additional classes of microsystems, from sensors to optoelectronics and microelectromechanical devices.

Experimental Section

Release and Transfer Printing of Foundry-Based Transient Electronic Microcomponents: The source wafers with transient microcomponents exploited a commercial process with a 1 µm design node in a partially depleted SOI CMOS platform (XI10 series; X-FAB) on 6 in. SOI (100) wafers. Constituent materials included active layers of Si (≈250 nm), gate oxide (≈25 nm), interlayer dielectric (ILD, ≈750 nm), and intermetal dielectric (IMD, ≈650 nm) layers of SiO_2 on a 1-µm-thick BOX layer, with up to three layers of W (≈300 nm) for interconnects (with 100-nm-thick Ti/TiN adhesion layers). Photolithography and ICP-RIE with SF_6 gas (STS Mesc Multiplex) eliminated ILD and IMD around the perimeters of each microcomponent to define targeted areas for release. A coating of PECVD SiN_x (≈600 nm) deposited at a mixed radio frequency power of 20 W (STS Mesc Multiplex) and patterned by photolithography and etching encapsulated the active regions of the microcomponents and defined narrow anchor regions at strategic locations near the edges. An additional ICP-RIE step established trenches through the nitride and BOX layers and into a small depth at the surface of the underlying silicon wafer. Anisotropic undercut etching followed immersion in a bath of diluted TMAH (8.3 wt% in H_2O; Sigma-Aldrich) at 85 °C. These steps resulted in arrays of microcomponents fully released from the underlying silicon wafer in a freely suspended configuration (≈3 µm), tethered by SiN_x anchors across the trenches. Transfer printing with a PDMS (10:1 mixture of base to curing agent) stamp removed and delivered selected collections of these microcomponents from the source wafer to foreign substrates.

Fabrication of Vertically Integrated Transient Circuits: Thin films of PLGA (95:5) heated to temperatures slightly over their glass transition temperatures (100 °C; molecular weight of 50 000–75 000) served as the receiving surfaces for transfer printing. Spin-coating of PLGA (85:15; Sigma-Aldrich) in an anisole solution minimized dissolution of underlying glassy PLGA, to yield planarizing interlayers on top of the printed microcomponents. RIE (O_2 gas, March RIE) through a hard mask of Mg deposited by sputtering and patterned by photolithography and etching, defined vias through the PLGA interlayers. Removal of the Mg mask completed this part of the processing. Patterning of layers of W (300 nm) deposited by sputtering over and into the vias by photolithography and etching provided layer-to-layer electrical connections. Additional microcomponents aligned and printed onto the resulting platform via a precision 4-axis transfer printer followed by repetitive application of the steps described above served as the route to stacked, 3D transient systems.

Characterization of Processes of Transience: After immersion in PBS (pH 7.4; Sigma-Aldrich) at 37 °C for certain periods of time, samples were removed from the solutions, rinsed and dried, and characterized at each stage of transience. Insoluble traces of Cr/Au served as connections for electrical probing with a function generator (3390; Keithley), an oscilloscope (TDS 2012C; Tektronix), a LCR meter (4980A; Agilent), and a semiconductor parameter analyzer (4155C; Agilent) with a probe station in a dark box. Changes in structure and morphology were monitored by field emission SEM (S4800; Hitachi), profilometry (3030; Dektak), and AFM (Cypher; Asylum Research) tools. Separate studies of PLGA involved immersion followed by drying under vacuum with desiccant for 3 d. Weighing the PLGA-coated samples before and after immersion in PBS define the mass loss of PLGA, and measurements of this type after drying of hydrated films yield the water uptake.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

3D integration, biodegradable electronics, flexible devices, heterogeneous integration, transfer printing

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[1] S. Hwang, H. Tao, D. Kim, H. Cheng, J. Song, E. Rill, M. Brenckle, B. Panilaitis, S. Won, Y. Kim, Y. Song, K. Yu, A. Ameen, R. Li, Y. Su, M. Yang, D. Kaplan, M. Zakin, M. Slepian, Y. Huang, F. Omenetto, J. A. Rogers, *Science* **2012**, *337*, 1640.

[2] K. Fu, Z. Wang, J. Dai, M. Carter, L. Hu, *Chem. Mater.* **2016**, *28*, 3527.
[3] H. Cheng, V. Vepachedu, *Theor. Appl. Mech. Lett.* **2016**, *6*, 21.
[4] C. Bettinger, Z. Bao, *Adv. Mater.* **2010**, *22*, 651.
[5] S. Hwang, J. Song, X. Huang, H. Cheng, S. Kang, B. Kim, J. Kim, S. Yu, Y. Huang, J. A. Rogers, *Adv. Mater.* **2014**, *26*, 3905.
[6] C. Park, S. Kang, H. Hernandez, J. Kaitz, D. Wie, J. Shin, O. Lee, N. Sottos, J. Moore, J. A. Rogers, S. White, *Adv. Mater.* **2015**, *27*, 3783.
[7] Y. Jung, T. Chang, H. Zhang, C. Yao, Q. Zheng, V. Yang, H. Mi, M. Kim, S. Cho, D. Park, H. Jiang, J. Lee, Y. Qiu, W. Zhou, Z. Cai, S. Gong, Z. Ma, *Nat. Commun.* **2015**, *6*, 7170.
[8] K. Yu, D. Kuzum, S. Hwang, B. Kim, H. Juul, N. Kim, S. Won, K. Chiang, M. Trumpis, A. Richardson, H. Cheng, H. Fang, M. Thompson, H. Bink, D. Talos, K. Seo, H. Lee, S. Kang, J. Kim, J. Lee, Y. Huang, F. Jensen, M. Dichter, T. Lucas, J. Viventi, B. Litt, J. A. Rogers, *Nat. Mater.* **2016**, *15*, 782.
[9] B. Kim, J. Kim, L. Persano, S. Hwang, S. Lee, J. Lee, Y. Yu, Y. Kang, S. Won, J. Koo, Y. Cho, G. Hur, A. Banks, J. Song, P. Won, Y. Song, K. Jang, D. Kang, C. Lee, D. Pisignano, J. A. Rogers, *Adv. Funct. Mater.* **2017**, *27*, 1606008.
[10] X. Zhang, L. Bellan, *ACS Appl. Mater. Interfaces* **2017**, *9*, 21991.
[11] T. Lei, M. Guan, J. Liu, H. Lin, R. Pfattner, L. Shaw, A. McGuire, T. Huang, L. Shao, K. Cheng, J. Tok, Z. Bao, *Proc. Natl. Acad. Sci. USA* **2017**, *114*, 5107.
[12] L. Yin, H. Cheng, S. Mao, R. Haasch, Y. Liu, X. Xie, S. Hwang, H. Jain, S. Kang, Y. Su, R. Li, Y. Huang, J. A. Rogers, *Adv. Funct. Mater.* **2013**, *24*, 645.
[13] Z. Wang, K. Fu, Z. Liu, Y. Yao, J. Dai, Y. Wang, B. Liu, L. Hu, *Adv. Funct. Mater.* **2017**, *27*, 1605724.
[14] C. Dagdeviren, S. Hwang, Y. Su, S. Kim, H. Cheng, O. Gur, R. Haney, F. Omenetto, Y. Huang, J. A. Rogers, *Small* **2013**, *9*, 3398.
[15] S. Hwang, G. Park, C. Edwards, E. Corbin, S. Kang, H. Cheng, J. Song, J. Kim, S. Yu, J. Ng, J. Lee, J. Kim, C. Yee, B. Bhaduri, Y. Su, F. Omennetto, Y. Huang, R. Bashir, L. Goddard, G. Popescu, K. Lee, J. A. Rogers, *ACS Nano* **2014**, *8*, 5843.
[16] S. Kang, S. Hwang, H. Cheng, S. Yu, B. Kim, J. Kim, Y. Huang, J. A. Rogers, *Adv. Funct. Mater.* **2014**, *24*, 4427.
[17] L. Yin, A. Farimani, K. Min, N. Vishal, J. Lam, Y. Lee, N. Aluru, J. A. Rogers, *Adv. Mater.* **2015**, *27*, 1857.
[18] S. Kang, R. Murphy, S. Hwang, S. Lee, D. Harburg, N. Krueger, J. Shin, P. Gamble, H. Cheng, S. Yu, Z. Liu, J. McCall, M. Stephen, H. Ying, J. Kim, G. Park, R. Webb, C. Lee, S. Chung, D. Wie, A. Gujar, B. Vemulapalli, A. Kim, K. Lee, J. Cheng, Y. Huang, S. Lee, P. Braun, W. Ray, J. A. Rogers, *Nature* **2016**, *530*, 71.
[19] Q. Liang, Q. Zhang, X. Yan, X. Liao, L. Han, F. Yi, M. Ma, Y. Zhang, *Adv. Mater.* **2016**, *29*, 1604961.
[20] G. Salvatore, J. Sülzle, F. Dalla Valle, G. Cantarella, F. Robotti, P. Jokic, S. Knobelspies, A. Daus, L. Büthe, L. Petti, N. Kirchgessner, R. Hopf, M. Magno, G. Tröster, *Adv. Funct. Mater.* **2017**, *27*, 1702390.
[21] C. Lee, H. Kim, D. Harburg, G. Park, Y. Ma, T. Pan, J. Kim, N. Lee, B. Kim, K. Jang, S. Kang, Y. Huang, J. Kim, K. Lee, C. Leal, J. A. Rogers, *NPG Asia Mater.* **2015**, *7*, e227.
[22] X. Huang, Y. Liu, S. Hwang, S. Kang, D. Patnaik, J. Cortes, J. A. Rogers, *Adv. Mater.* **2014**, *26*, 7371.
[23] S. Hwang, D. Kim, H. Tao, T. Kim, S. Kim, K. Yu, B. Panilaitis, J. Jeong, J. Song, F. Omenetto, J. A. Rogers, *Adv. Funct. Mater.* **2013**, *23*, 4087.
[24] J.-K. Chang, H. Fang, C. Bower, E. Song, X. Yu, J. A. Rogers, *Proc. Natl. Acad. Sci. USA* **2017**, *114*, E5522.
[25] A. Carlson, A. Bowen, Y. Huang, R. Nuzzo, J. A. Rogers, *Adv. Mater.* **2012**, *24*, 5284.
[26] J. Ahn, H. Kim, K. Lee, S. Jeon, S. Kang, Y. Sun, R. Nuzzo, J. A. Rogers, *Science* **2006**, *314*, 1754.
[27] S. Nam, X. Jiang, Q. Xiong, D. Ham, C. Lieber, *Proc. Natl. Acad. Sci. USA* **2009**, *106*, 21035.
[28] A. Sachid, M. Tosun, S. Desai, C. Hsu, D. Lien, S. Madhvapathy, Y. Chen, M. Hettick, J. Kang, Y. Zeng, J. He, E. Chang, Y. Chueh, A. Javey, C. Hu, *Adv. Mater.* **2016**, *28*, 2547.
[29] P. Garrou, C. Bower, P. Ramm, *Handbook of 3D Integration*, Wiley-VCH, Weinheim, Germany **2012**.
[30] K. Banerjee, S. Souri, P. Kapur, K. Saraswat, *Proc. IEEE* **2001**, *89*, 602.
[31] H. Kim, E. Brueckner, J. Song, Y. Li, S. Kim, C. Lu, J. Sulkin, K. Choquette, Y. Huang, R. Nuzzo, J. A. Rogers, *Proc. Natl. Acad. Sci. USA* **2011**, *108*, 10072.
[32] Z. Fan, J. Ho, Z. Jacobson, R. Yerushalmi, R. Alley, H. Razavi, A. Javey, *Nano Lett.* **2008**, *8*, 20.
[33] M. McAlpine, H. Ahmad, D. Wang, J. Heath, *Nat. Mater.* **2007**, *6*, 397.
[34] B. Corbett, R. Loi, W. Zhou, D. Liu, Z. Ma, *Prog. Quantum Electron.* **2017**, *52*, 1.
[35] A. Javey, S. Nam, R. Friedman, H. Yan, C. Lieber, *Nano Lett.* **2007**, *7*, 773.
[36] M. Meitl, Z. Zhu, V. Kumar, K. Lee, X. Feng, Y. Huang, I. Adesida, R. Nuzzo, J. A. Rogers, *Nat. Mater.* **2005**, *5*, 33.
[37] G. Katti, M. Stucchi, K. De Meyer, W. Dehaene, *IEEE Trans. Electron Devices* **2010**, *57*, 256.
[38] M. Motoyoshi, *Proc. IEEE* **2009**, *97*, 43.
[39] M. Shulaker, G. Hills, N. Patil, H. Wei, H. Chen, H. Wong, S. Mitra, *Nature* **2013**, *501*, 526.
[40] M. Shulaker, G. Hills, R. Park, R. Howe, K. Saraswat, H. Wong, S. Mitra, *Nature* **2017**, *547*, 74.
[41] H. Cheng, R. Barnett, U. Landman, *J. Chem. Phys.* **2002**, *116*, 9300.
[42] E. Baeuerlein, *Biomineralization*, Wiley-VCH, Weinheim, Germany **2004**.
[43] Q. Chen, G. Thouas, *Mater. Sci. Eng. R* **2015**, *87*, 1.
[44] D. Lison, J. Bucket, P. Hoet, *Lancet* **1997**, *349*, 58.
[45] V. Thakur, M. Thakur, *Handbook of Polymers For Pharmaceutical Technologies, Biodegradable Polymers*, Wiley-Scrivener, Hoboken **2015**.
[46] A. Domb, *Handbook of Biodegradable Polymers*, Harwood Academic, Amsterdam **1997**.
[47] I. Dékány, *Adsorption And Nanostructures*, Springer, Berlin, Germany **2002**.
[48] Z. Cao, Q. Yu, H. Xue, G. Cheng, S. Jiang, *Angew. Chem., Int. Ed.* **2010**, *122*, 3859.
[49] V. Babak, F. Baros, O. Boulanouar, F. Boury, M. Fromm, N. Kildeeva, N. Ubrich, P. Maincent, *Colloids Surf., B* **2007**, *59*, 194.
[50] Y. Wan, X. Qu, J. Lu, C. Zhu, L. Wan, J. Yang, J. Bei, S. Wang, *Biomaterials* **2004**, *25*, 4777.
[51] V. Karagkiozaki, E. Vavoulidis, P. G. Karagiannidis, M. Gioti, D. G. Fatouros, I. S. Vizirianakis, S. Logothetidis, *Int. J. Nanomed.* **2012**, *7*, 5327.
[52] A. Kondyurin, I. Kondyurina, M. Bilek, *arXiv:1101.0659 [physics. chem-ph]*.
[53] J. Hattori, K. Fukuda, T. Irisawa, H. Ota, T. Maeda, *Jpn. J. Appl. Phys.* **2017**, *56*, 04CC02.
[54] Z. He, Y. Sun, J. Cao, Y. Duan, *Phys. Chem. Chem. Phys.* **2016**, *18*, 11986.
[55] A. Shibata, S. Yada, M. Terakawa, *Sci. Rep.* **2016**, *6*, 27884.
[56] R. Li, H. Cheng, Y. Su, S. Hwang, L. Yin, H. Tao, M. Brenckle, D. Kim, F. Omenetto, J. A. Rogers, Y. Huang, *Adv. Funct. Mater.* **2013**, *23*, 3106.
[57] J. Kang, S. Schwendeman, *Macromolecules* **2003**, *36*, 1324.
[58] X. Zhu, R. Braatz, *J. Biomed. Mater. Res. A* **2014**, *103*, 2269.
[59] X. Wu, N. Wang, *J. Biomater. Sci., Polym. Ed.* **2001**, *12*, 21.
[60] P. Ritger, N. Peppas, *J. Controlled Release* **1987**, *5*, 37.
[61] Y. You, S. Lee, J. Youk, B. Min, S. Lee, W. Park, *Polym. Degrad. Stab.* **2005**, *90*, 441.

