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FULL PAPER

Dry Transient Electronic Systems by Use of Materials that Sublime

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The recent emergence of materials for electronic systems that are capable of programmable self-destruction and/or bio/eco-resorption creates the potential for important classes of devices that cannot be easily addressed using conventional technologies, ranging from temporary biomedical implants to enviromentally benign environmental monitors to hardware secure data systems. Although most previous demonstrations rely on wet chemistry to initiate transient processes of degradation/decomposition, options in "dry transient electronic systems" could expand the range of possible uses. The work presented here introduces materials and composite systems in which sublimation under ambient conditions leads to mechanical fragmentation and disintegration of active devices upon disappearance of a supporting substrate, encapsulation layer, interlayer dielectric and/or gate dielectric. Examples span arrays of transistors based on silicon nanomembranes with specialized device designs to solar cells adapted from commercial components.

1. Introduction

The emerging field of transient electronics relies on the development of materials and device architectures that undergo controlled, physical self-elimination by processes ranging from water dissolution to enzymatic degradation to depolymerization to mechanical fragmentation.[1–5] Such features are of interest for applications not well served by conventional technologies, such as temporary biomedical implants,[6–11] resorbable environmental monitors,[12] physically secure data storage systems,[13–15] and nonrecoverable sensitive electronics.[16–20] Most work in transient electronics involves the development of systems that dissolve or are physically altered by the action of wet chemistries. Examples include biodegradable electronics, where

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dissolution in biofluids eliminates device load on the body and self-destructing devices with cointegrated triggerable microfluidic systems that contain etchants.[16,18,21] Certain applications could, however, benefit from transient operation in environments where there is little or no ambient water or moisture, such as in the desert, at high altitudes, or in space, using device designs that avoid the need for microfluidics.

This paper presents materials and device designs for forms of transient electronics that undergo timed self-destruction induced by ambient sublimation of a supporting substrate, encapsulation layer, interlayer dielectric, and/or gate dielectric followed by resulting fragmentation of the remaining, ultrathin components of the circuit.[22] Such "dry" operation provides capabilities that complement those of more widely explored "wet" systems. Examples of these approaches include transistors and solar cells formed by transfer printing ultrathin, preformed silicon devices onto sublimating substrates, including demonstrations where the same material also serves as the dielectric layers. Sublimation leads to disintegration of the remaining materials into microscopic fragments due to loss of mechanical support and/or adjoining films. Cyclododecane (CDD), sometimes utilized as a temporary layer to protect fragile and sensitive surfaces during archeological recovery,[23,24] provides an excellent material for such purposes due to its low melting point (90 °C), high vapor pressure (0.1 hPa) at room temperature, and low viscosity at elevated temperatures (2.2 mPaS@95 °C). Other examples of materials include menthol, camphor, perfluorododecane, and hexamethylcyclotrisiloxane. Composites based on embedded nanoparticles provide a means to control the rate of sublimation by modulating the exposed interfacial area.

The dry mode of transience in the technology presented here has several advantages compared to wet alternatives: it avoids (1) the need for external or internal sources of liquid reactants whose availability might be limited either by the nature of the surrounding environment or the difficulty in forming hermetically sealed, integrated microfluidic reservoirs, (2) challenges in semiconductor processing of materials that are susceptible to liquid exposure, and (3) variability in dissolution/reaction rates due to uncontrolled flows of dissolving liquids. The combination of wet and dry approaches could create additional possibilities, where sublimating materials—many of which have extremely low water solubility and permeability rates—serve as an encapsulating layer for wet transient devices.

2. Results and Discussion

Applying mechanical forces to crystal grains (sample mass in the decigram range) can yield free-standing films of waxy sublimating solids. Specifically, forces of 50–60 kN applied for 10–30 min through a two-column precision manual press at room temperature activate material transport and grain melting to facilitate film formation. Depending on the force, processing time ,and amount of starting material, films with 500–700 μm thickness and 3–4 cm diameter can be achieved in this manner.
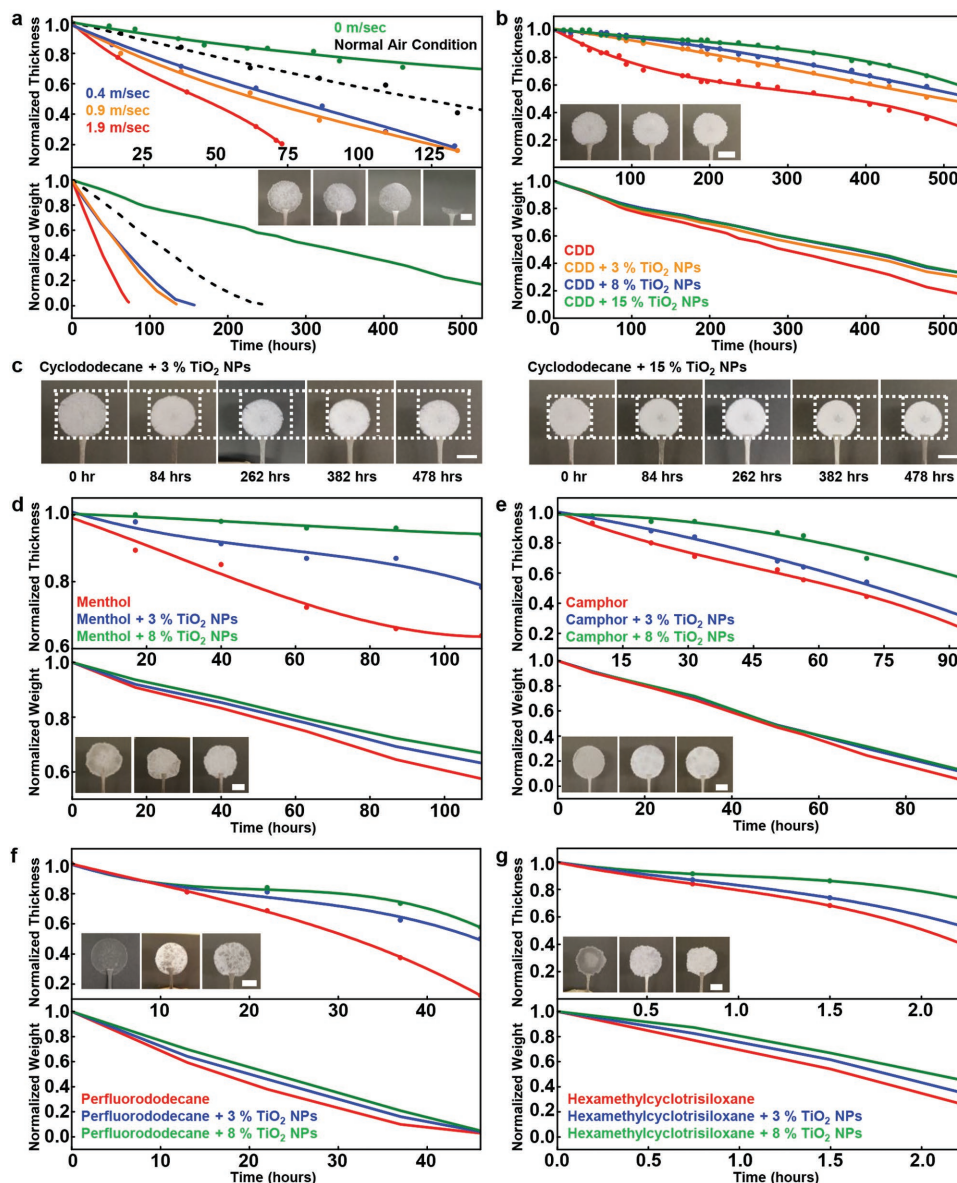
Many factors, including thickness, shape, exposed surface area, and ambient conditions such as temperature and air ventilation, affect the rate of sublimation in a material such as CDD.

The role of ventilation can be assessed by placing samples with identical shapes and masses under a fume hood under stable ambient conditions (temperature: 21 °C; humidity: 30%–40%), varying the face velocity of the hood through the position of the front sash, and measuring the sample thickness (at the center) and mass at several times (**Figure 1**a). Data collected under ambient laboratory conditions serve as points of comparison (black dots in Figure 1a). In the absence of ventilation, the sublimation rate is about 1.3 μm h^{-1}. This rate increases to 4.6 μm h^{-1} under ventilation with an air velocity of 1.9 m s^{-1}. The corresponding mass losses are of 0.7 and 4 mg h^{-1}, respectively (data linear fitting for $0 \leq t \leq 70$ h). Photographs in the inset of Figure 1a display the morphological and dimensional changes of CDD samples, stored at the highest ventilation rate tested here.

An effective strategy to reduce the sublimation rate involves addition of titanium dioxide nanoparticles (TiO$_2$ NPs, average diameter: 10 nm) with concentrations in the range 3%–15% w/w in the CDD. The result reduces the sublimation rate by a factor of 3 for the 15% w/w case during the first 100 h for samples that have a total surface area of ≈20 cm^2 and a mass of ≈0.3 g (Figure 1b). Sublimation proceeds rapidly at the edges, and NPs deposit on the supporting substrate as the CDD disappears. For times beyond ≈100 h, the sublimation rate further decreases, particularly for formulations that involve high NP loading. After 500 h, the thicknesses of CDD samples doped with NPs at 8% are roughly twice as large as those of pure CDD. Photographs that capture the time dependence of the morphologies of samples with different NPs content appear in Figure 1c. The inclusion of NPs might reduce the mesoscale extension of more volatile, superficial molecular layers, and compete with sublimation by hydrophobic–hydrophobic interactions with the wax molecules, thus leading to sublimation enthalpy increase and to a reduced rate of mass loss.

A range of other materials can also be considered, as summarized in Figure 1d–g and Figures S1–3 (Supporting Information). For instance, menthol exhibits sublimation rates comparable to CDD (1.6 μm h^{-1}), with values that are also strongly reduced by the addition of NPs (up to five times for 8% w/w doped samples). The inclusion of NPs appears to be a generally applicable strategy to reduce the sublimation rate.
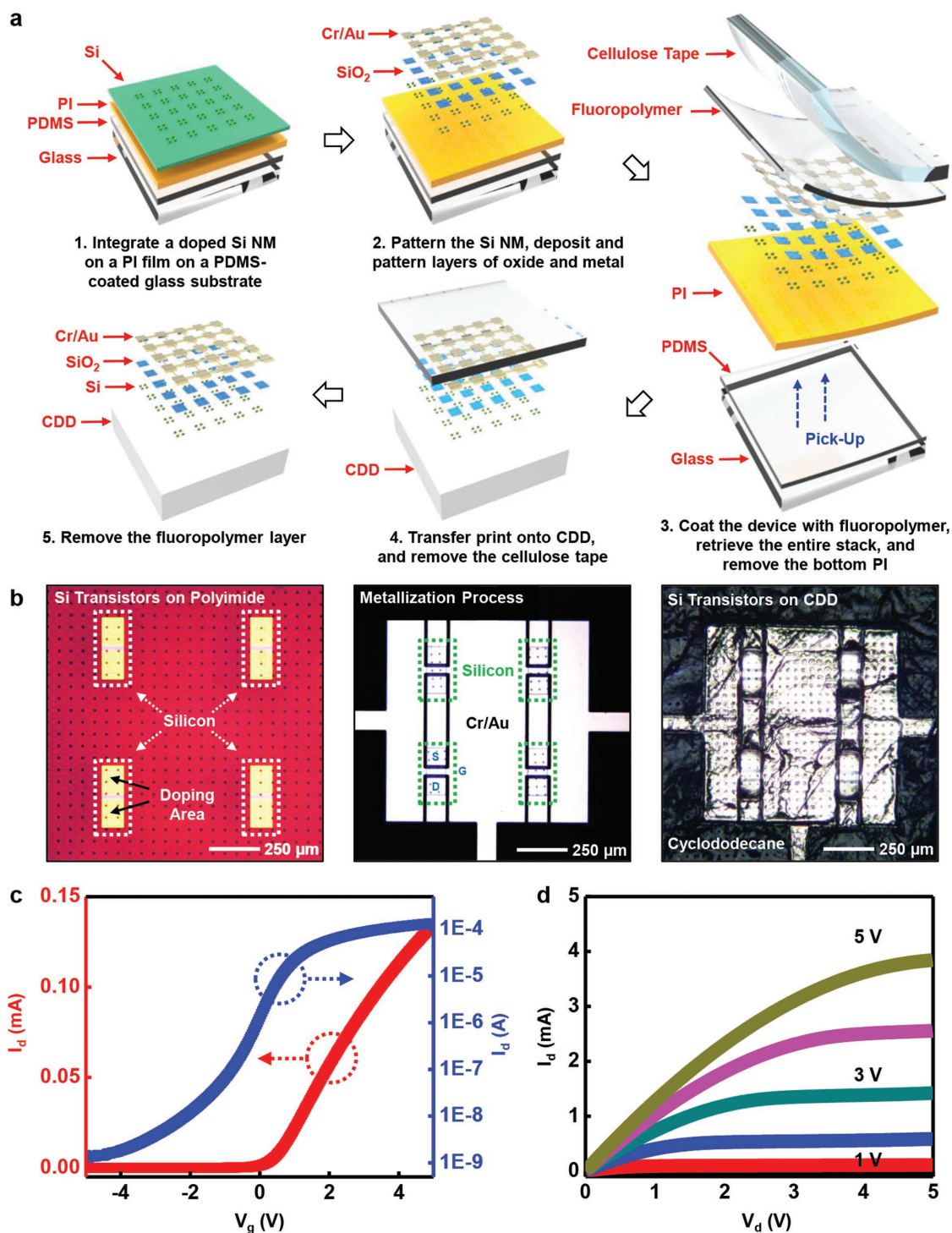
The fabrication of dry transient electronic devices involves conventional microfabrication processes (e.g., thermal annealing, deposition, etching, and lithographic patterning) conducted prior to integration of the sublimating substrates or dielectric layers. This scheme is valuable because most sublimating materials of interest for present purposes sublimate quickly and completely at 100 °C and continuously even under ambient temperature and pressure, thereby severely limiting the ability to perform any form of high temperature or vacuum processing. **Figure 2**a presents a schematic illustration of the process flow. The first step yields a temporary, or handle, substrate by thermally curing a spin-cast layer of diluted polydimethylsiloxane (PDMS) (monomer: cross-linker: hexane: 10: 1: 10, weight ratio, 3000 rpm) on a glass wafer. Next, spin-casting and curing a layer of polyimide (PI: ≈ 6 μm; Sigma-Aldrich, Inc.) form a temporary support. Transfer printing delivers a collection of silicon nanomembranes (Si NMs, ≈200 nm) with patterned regions of doping onto the PI layer in spatial layouts that

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Figure 1. Rate of sublimation of CDD and dependence on loading ratio of TiO$_2$ nanoparticles (NPs). The plots show thickness (top panel) and weight (bottom panel) of free-standing films made with different compositions and under different conditions. In all cases, data are normalized to the initial values. In the images, all scale bars are 1.5 cm. a) CDD films stored under a fume hood at different face velocities. Data collected at typical laboratory conditions serve as comparisons (insets: photographs of a film stored at 1.9 m s^{-1}, at different times. From left to right: photograph of a just-produced sample, and after 24, 70, and 95 h, respectively). b) Pure CDD film and various CDD composites with TiO$_2$ NPs stored under a fume hood at 0 m s^{-1} face velocity (insets: photographs of representative samples. From left to right: TiO$_2$/CCD: 3%, 8%, and 15% w/w, respectively). c) Photographs of composite films at different times. d) Menthol and menthol/TiO$_2$ NP films stored under a fume hood at 0 m s^{-1} face velocity (insets: photographs of representative samples. From left to right: pure menthol, TiO$_2$/menthol: 3%, and TiO$_2$/menthol: 8% w/w, respectively). e) Camphor and camphor/TiO$_2$ NP films stored under a fume hood at 0 m s^{-1} face velocity (insets: photographs of representative samples. From left to right: pure camphor, TiO$_2$/camphor: 3%, and TiO$_2$/camphor: 8% w/w, respectively). f) Perfluorododecane and perfluorododecane/TiO$_2$ NP films stored under a fume hood at 0 m s^{-1} face velocity (insets: photographs of representative samples. From left to right: pure perfluorododecane, TiO$_2$/perfluorododecane: 3% and TiO$_2$/perfluorododecane: 8% w/w, respectively). g) Hexamethylcyclotrisiloxane and hexamethylcyclotrisiloxane/TiO$_2$ NP films stored under a fume hood at 0 m s^{-1} face velocity (insets: photographs of representative samples. From left to right: pure hexamethylcyclotrisiloxane: 3% and TiO$_2$/hexamethylcyclotrisiloxane: 8% w/w, respectively).

match device requirements.[27,28] Photolithography followed by reactive ion etching (RIE; SF$_6$, 50 mtorr, 100 W, 40 sccm, and 120 s) structures the membranes to leave only silicon in the active regions of the devices. Plasma-enhanced chemical vapor deposition (PECVD) of SiO$_2$ (100 nm) forms the gate

oxide layer, patterned by photolithography and buffered oxide etching. Electron beam evaporation of Au/Cr (≈100/5 nm) followed by photolithography and wet etching defines electrodes and interconnects. Spin-casting a thin film of a fluoropolymer (6 µm, OSCoR 2312 photoresist solution, Orthogonal, Inc.)

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Figure 2. Materials and procedures for fabricating dry transient electronic circuits on substrates that sublime. a) Schematic illustrations of the steps for fabrication. The process begins with a silicon nanomembrane (Si NM) on a handle substrate with patterns of doping in the configuration of the array (upper left). Deposition and patterning of a gate oxide and set of electrodes defines nMOS transistors (upper middle). Retrieving the array using a water-soluble tape allows exposure and removal of the bottom layer of polyimide by reactive ion etching (right). Transfer printing onto a CDD substrate (lower middle) and removing the fluoropolymer complete the process (lower left). b) Optical microscopic images of an Si NM on polyimide (left), after gate oxide deposition and metallization (middle); an array of transistors on a substrate of CDD (right). c) Linear and log scale plots of the transfer curves, and d) current–voltage characteristics of a representative device (channel length/width: 15/80 μm).

onto the entire device stack allows retrieval onto a water-soluble cellulose tape. This layer is important because it conformally embeds the devices into its near surface region.[29] The very

low strength of adhesion between the PI and PDMS greatly enhances the yield of retrieval.[30] Next, RIE (O_2 gas, 200 mtorr, 150 W, and 20 sccm) eliminates the PI from the bottom while

the structure remains adhered to the cellulose.[31] The final pair of steps involves transfer onto a CDD substrate (diameter 1.5 cm, thickness 4–5 mm) formed by pouring molten CDD into a metal mold, and removing the cellulose and the fluoropolymer by immersion in deionized water and stripper solution (Orthogonal stripper 700 solution, Orthogonal, Inc.),[32] respectively.

Optical micrographs in Figure 2b show (i) doped Si NM transfer printed onto PI, (ii) patterned Cr/Au metallization, and (iii) an array of n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) on CDD. As the CDD sublimes, the mechanical support for the fragile, ultrathin device structures disappears, thereby leading to their mechanical fracture and fragmentation under naturally occurring, ambient environmental conditions (e.g., wind and rain).

The electrical properties (Figure 2c, linear and log scale plots of the transfer curves; Figure 2d, current–voltage characteristics) of a representative n-channel MOSFET with L (channel length): 15 µm and W (channel width): 80 µm indicate on/off ratios of $\gtrsim 10^5$, saturation and linear regime mobilities of ≈ 400 and ≈ 500 cm^2 V^{-1}s^{-1}, respectively (Figure 2c; Figure S4, Supporting Information). Current–voltage characteristics measured at various gate biases (0–5 V) are shown in Figure 2d. These electrical behaviors are similar to those of analogous devices on nontransient, rigid substrates.[31]

Figure 3a,b shows a time sequence of top and tilted-view images that illustrate the disintegration of a 5 × 5 array of transistors upon sublimation of the CDD in a dry environment at elevated temperature (60 °C, humidity: 25%,). Within ≈ 12 d, the CDD substrate largely disappears and the supported electronics fragment into pieces with characteristic sizes of 200–300 µm, likely due to ambient air flow and rates of sublimation that vary across the substrate according to the local coverage of the overlying electronic layers. Figure 3b shows that a peak forms at the center regions of each silicon device as time passes (red-dotted line at the center of Figure 3b). This effect follows from limited air exposure of the CDD that lies beneath the source, drain, and gate electrodes, which have dimensions that are relatively large compared to those of the interconnects. These differences lead to spatial variations in the rate of undercut removal of the CDD.
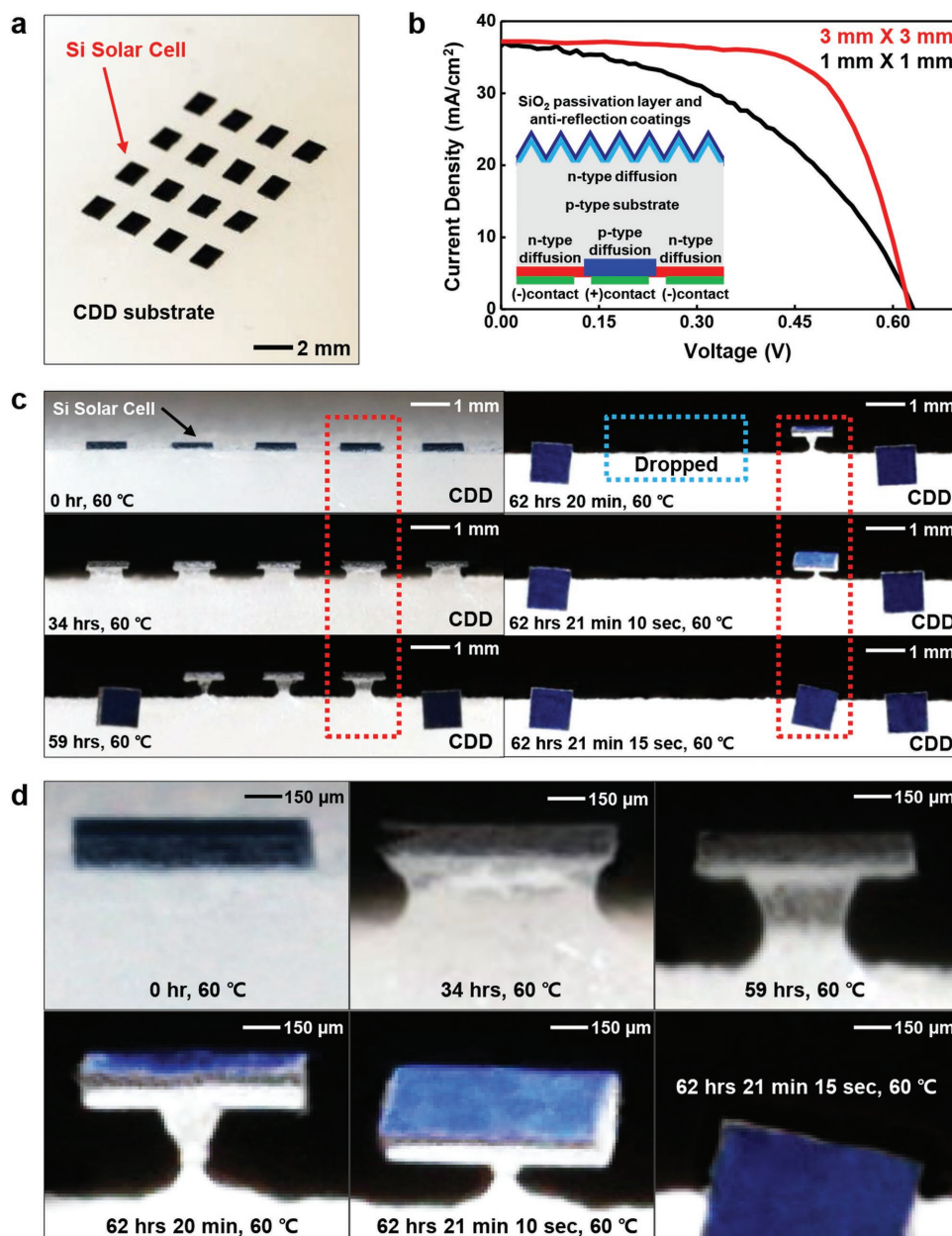
An important aspect of these ideas is that they are compatible with commercial components, as shown in **Figure 4**a, for the case of a silicon solar cell module (DIY Professional Mono Sunpower Solar Cell, Dig Dog Bone Inc.). Here, laser dicing (see the Experimental Section) divides the module into small pieces to facilitate fragmentation in the transience process. Figure 4b shows the efficiencies of cells with dimensions of 1 mm × 1 mm (V_{oc}: 0.63 V; J_{sc}: 36.97 mA cm^{-2}; fill factor: 45%; Eff.: 10.4%) and 3 mm × 3 mm (V_{oc}: 0.62 V; J_{sc}: 37.2 mA cm^{-2}; fill factor: 68%; Eff.: 15.68%) formed in this manner, along with a schematic illustration. Figure 4c presents photographs that capture the time evolution of the sublimation of a CDD substrate for these components. Figure 4d is an enlarged image that corresponds to the region highlighted by the red-dotted line in Figure 4c. Within 3 d, the cells collapse as the CDD disappears. By contrast to the transistors and interconnects described previously, these solar cells are sufficiently rigid that they do not bend or fracture, as shown in Figure 4d, such that air can transport underneath the devices throughout most of the undercut process. The
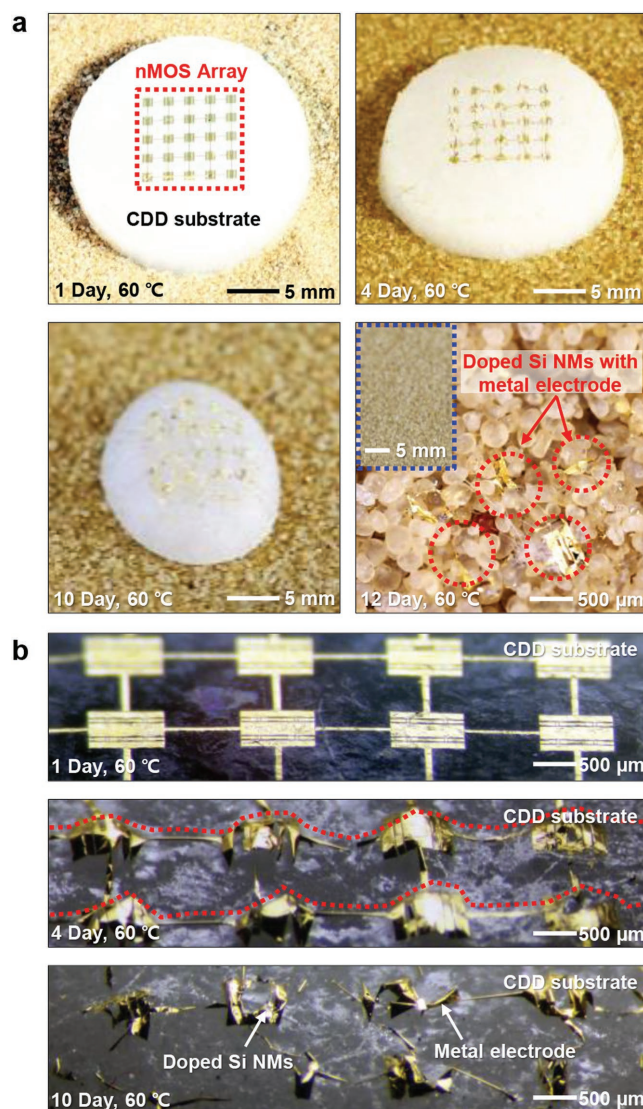
Figure 3. Microscopic images of disintegration of an array of transistors as a result of sublimation of a supporting substrate of CDD. a) Images that illustrate the process of self-destruction after 1, 4, 10, and 12 d, at a temperature of 60 °C. b) Additional images corresponding to each case in part (a).

cells begin to tilt as the sublimation proceeds such that disintegration occurs due to failure of the interconnects, at rates that exceed those of the devices in Figure 3, where bending of the layers frustrates free access of air to the underlying CDD surfaces.

Sublimating materials can also be used as functional layers. **Figure 5**a shows an example of a variable capacitor, in which a layer of CDD with a thickness of 70–100 µm serves as the dielectric and Mg serves as the electrodes (bottom electrode: 2 µm; top electrode: 20 µm). Sublimation causes the capacitance to vary over time, as summarized in Figure 5b,c. The capacitance decreases by 0.07 pF within 40 h and by another 0.12 pF over the following 20 h. This mode, in which critical layers of the devices themselves disappear, provides additional options in the use of sublimation for transient devices.

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Figure 4. Dry transient behavior in an array of solar cells. a) Photographs of an array of solar cells on a CDD substrate. b) Current–voltage curves and schematic illustration of an individual cell. The cells have sizes of 1 mm × 1 mm or 3 mm × 3 mm, laser cut from a commercially available silicon solar cell module. c) Photographs showing the process of undercut by sublimation of CDD beneath a solar cell as a function of time, for a temperature of 60 °C. d) Optical microscope images of the region highlighted by the red dotted boxes in part (c).

3. Conclusion

To summarize, the concepts introduced here provide materials, processing strategies, and designs for dry transient electronic devices that exploit sublimation of key constituent materials. The demonstrated examples, i.e., disintegrating capacitors and arrays of transistors and solar cells under dry and ambient conditions, suggest possibilities for use in other kinds of advanced technologies, ranging from photonics to optoelectronics and microelectromechanical systems. The combined use of wet and dry transient electronic devices might be an interesting direction to explore in future work.

4. Experimental Section
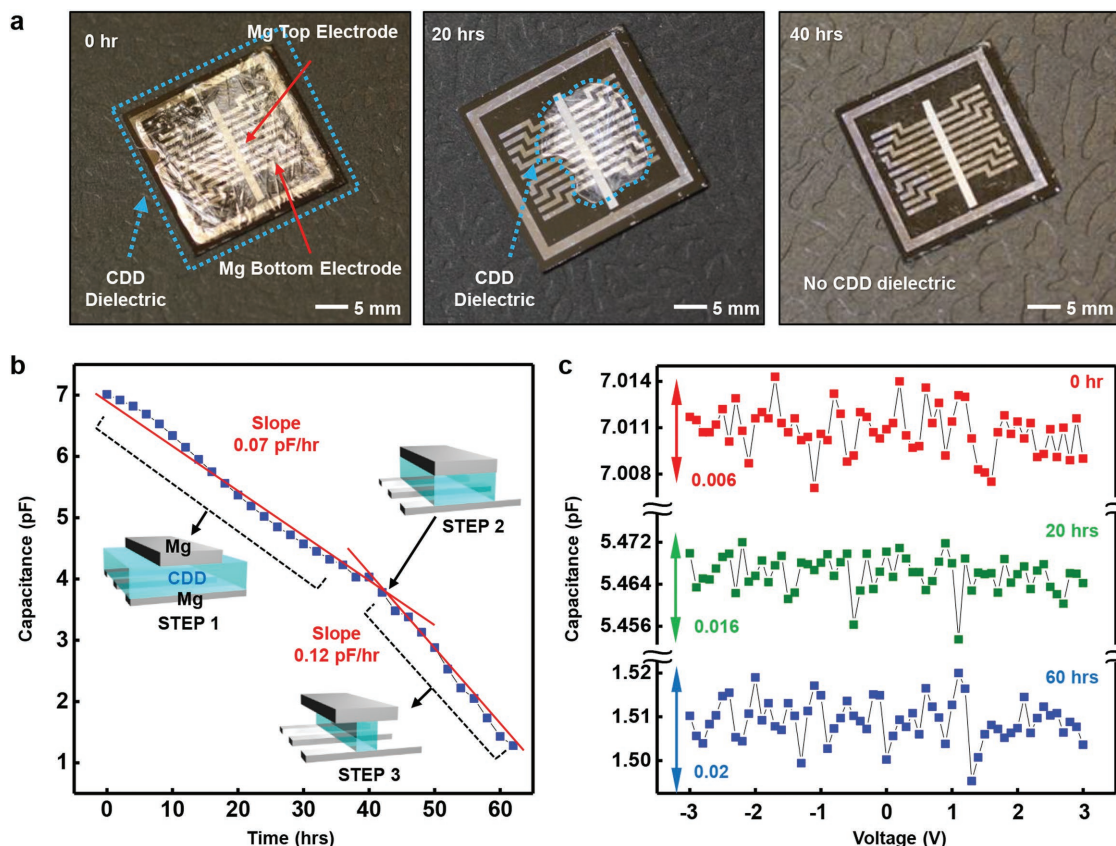
Figure 5. Dry transient capacitor that uses a sublimating dielectric layer. a) Photograph of a device composed of Mg top/bottom electrodes and a CDD dielectric layer. The device self-destructs by sublimation at ambient conditions. b,c) Plot of the capacitance as a function of time and graphs of voltage–capacitance at three representative times.

powder (99%, 10 nm) was purchased from Nanostructured and Amorphous Materials, Inc. (Houston, USA).

Fabrication of Dry Transient Silicon nMOS Transistors: Phosphorus doping at 950 °C defined highly doped areas for source and drain contacts on n-type silicon on insulator (SOI, top silicon ≈300 nm, SOITEC, France) wafers for n-type transistors. Removal of the buried oxide by wet etching with HF released the top device silicon from the SOI, and enabled transfer printing of the resulting Si NMs onto spin-casted films of polyimide/PDMS on a glass carrier substrate. Patterned regions of silicon resulted from RIE (Plasmatherm) with sulfur hexafluoride (SF$_6$) gas. A thin layer of SiO$_2$ (≈100 nm) formed by PECVD served as the gate dielectric. Etching openings in this layer using a buffered oxide etchant (Transene Company, Inc., USA) defined contact pads for source and drain electrodes. A 100/5 nm layer of Au/Cr, deposited by electron beam evaporation, was used for source, drain, gate electrodes, as well as interconnects. After metallization, spin casting yielded a thin film of a fluoropolymer (6 µm, OSCoR 2312 Photoresist Solution, Orthogonal, Inc.) across the entire sample. After retrieving the device stack with a water-soluble cellulose tape, RIE using oxygen (O$_2$) gas removed the bottom layer of polyimide. Transfer printing delivered the device stacks onto a CDD substrate. Finally, DI water and stripper solution (Orthogonal stripper 700 solution, Orthogonal, Inc.) removed the water-soluble tape and fluoropolymer layer, respectively.

Fabrication of Dry Transient Silicon Solar Cells: Commercially available solar cell modules (DIY Professional Mono Sunpower Solar Cell, Dig Dog Bone, Inc.) were laser cut (diode pumped IR laser, wavelength: 790–820 nm; power: 0.5–1 W; pulse width: 15 ns; 20 times) into

1 mm × 1 mm and 3 mm × 3 mm sizes. Transfer printing delivered these components onto a CDD substrate heated to its glass temperature.

Fabrication of Dry Transient Capacitors: Photolithographic patterning of a film (≈2 µm thick) of Mg evaporated onto a clean silicon wafer defined bottom electrodes. Spray coating formed a uniform film of CDD. A mm-scale Mg metal film (≈20 µm) physically laminated on top served as the top electrode.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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