

Ultrathin, transferred layers of thermally grown silicon dioxide as biofluid barriers for biointegrated flexible electronic systems

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Materials that can serve as long-lived barriers to biofluids are essential to the development of any type of chronic electronic implant. Devices such as cardiac pacemakers and cochlear implants use bulk metal or ceramic packages as hermetic enclosures for the electronics. Emerging classes of flexible, biointegrated electronic systems demand similar levels of isolation from biofluids but with thin, compliant films that can simultaneously serve as biointerfaces for sensing and/or actuation while in contact with the soft, curved, and moving surfaces of target organs. This paper introduces a solution to this materials challenge that combines (i) ultrathin, pristine layers of silicon dioxide (SiO₂) thermally grown on device-grade silicon wafers, and (ii) processing schemes that allow integration of these materials onto flexible electronic platforms. Accelerated lifetime tests suggest robust barrier characteristics on timescales that approach 70 y, in layers that are sufficiently thin (less than 1 μm) to avoid significant compromises in mechanical flexibility or in electrical interface fidelity. Detailed studies of temperature- and thickness-dependent electrical and physical properties reveal the key characteristics. Molecular simulations highlight essential aspects of the chemistry that governs interactions between the SiO₂ and surrounding water. Examples of use with passive and active components in high-performance flexible electronic devices suggest broad utility in advanced chronic implants.

thin-film encapsulation | thermal silicon dioxide | transfer printing | reactive molecular simulation | chronic implant

Advanced concepts in materials science and engineering form the foundations for emerging classes of high-performance, flexible electronic/optoelectronic devices, with levels of functionality that far exceed those of passive components and arrays. These systems are of interest because they can conform to the surfaces of biological systems in ways that enable important capabilities of relevance to both biomedical research and clinical practice. Examples include devices for continuous monitoring of health status through the skin (1–9), optical stimulation of targeted neural circuits in the brain (10–13), and electrophysiological mapping on the epicardial surface (14–17). These platforms are unique because their lightweight construction, thin geometry, and low bending stiffness allow high-quality, minimally invasive interfaces to soft, dynamic biological tissues, in a manner that cannot be replicated with conventional wafer-based forms of electronics. Such physical properties and mechanical attributes follow from the successful codevelopment of organic, inorganic, and hybrid inorganic/organic semiconductor materials together with mechanical designs and manufacturing schemes that enable

their deployment in systems that can bend to small radii of curvature and, in some cases, stretch to high levels of elongation (2, 18–22). Skin-mounted devices, sometimes referred to as “epidermal” electronics (1), represent one of the most successful forms of this technology, where commercial embodiments are just now becoming widely available. Extensions of these types of systems for use as chronic implants have the potential to improve capabilities in human health care across broad categories of disease states and disorders (23, 24). A daunting challenge is in the development of materials that can serve as long-lived, perfect barriers to biofluids at thicknesses that allow high-quality sensing/actuating interfaces to the surrounding biology without adversely affecting the compliant mechanics.

In an ideal scenario, this material would encapsulate the entire front and back surfaces of the electronics, to prevent biofluid penetration across any exposed interfaces, with the following additional characteristics: (i) biocompatible molecular composition;

Significance

A critical obstacle of flexible electronics for chronic implants is the absence of thin-film barriers to biofluids with multidecade lifetimes. Previously explored materials are unsuitable due to limitations of (i) extrinsic factors, such as the practical inability to avoid localized defects, and/or (ii) intrinsic properties, such as finite water permeability. The work presented here overcomes these challenges by combining pristine thermal SiO₂ layers with processing steps for their integration onto flexible electronics. Experimental and theoretical studies reveal the key aspects of this material system. Accelerated immersion tests and cyclic bending measurements suggest robust, defect-free operation with various electronic components and an integrated system for multiplexed mapping of electrophysiological signals. The findings have broad relevance to diverse biointegrated electronics and optoelectronics.

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(ii) high electrical capacitance (for electrical interfaces); (iii) low thermal conductivity and thermal mass (for thermal interfaces); (iv) good optical transparency (for optical interfaces); (v) low areal mass density (for minimized inertial load); (vi) low flexural rigidity (for conformal integration onto curved surfaces); (vii) defect-free, material perfection over large areas (several or many square centimeters); (viii) thermal and chemical compatibility with polymer substrates (for device fabrication) and (ix) lifetimes of multiple decades in electrolyte solutions at physiological pH and temperature, under cyclic bending conditions (for robust operation throughout the life of the patient). Despite more than a decade of research on this topic in academic and industrial groups around the world, there is currently no proven material system that offers these properties.

Established encapsulation schemes for conventional electronic implants such as pacemakers, cochlear implants, and deep-brain stimulators, rely on thick (millimeter-scale), rigid enclosures constructed using bulk metal or ceramic parts, incompatible with the types of flexible platforms discussed here (23, 25–27). Strategies based on thin flexible films are suitable for passive arrays of sensing/actuating electrodes or related devices (28–32), but they are not immediately applicable to active, semiconductor-based electronic platforms where continuous, or nearly continuous, applied voltages and induced currents are essential for operation (14, 18, 33–35). Organic/inorganic multilayer encapsulation schemes designed to protect flexible consumer electronic devices from oxygen and moisture have some promise (36–38), but known adaptations of them cannot address the extremely demanding conditions encountered in the body, where full immersion in warm, circulating biofluids on multidecade timescales is required.

Here, we report a different approach, based on an unusual materials solution that offers all of the nine attributes listed above. The scheme combines (i) defect-free, ultrathin layers of SiO_2 grown at high temperatures on the pristine, single crystalline surfaces of device-grade silicon wafers, with (ii) procedures for integrating these layers as uniform, front-side biofluid barriers and biointerfaces on flexible electronic platforms, and as backside barriers on their thin polymer supports. Detailed studies and comparative measurements against many of the most widely explored thin-film encapsulation strategies illustrate the exceptional characteristics that are possible. Thicknesses can range between tens and thousands of nanometers, in robust flexible geometries that are compatible with all important classes of materials and devices for flexible electronics. A combination of temperature-dependent measurements, microscopy investigations, electrical leakage and permeation tests, electrochemical impedance spectroscopic characteristics, and molecular dynamics simulations reveal the essential materials properties. Experiments with basic components, ranging from passive elements such as resistors, capacitors, and diodes to active, metal-oxide semiconductor transistors and multiplexed arrays, demonstrate compatibility with the highest performance types of flexible electronic devices.

Results

Thermal Growth of Ultrathin Layers of SiO_2 and Their Integration onto Flexible Plastic Substrates. Fig. 1A shows the four main steps for thermally growing, transferring, and integrating ultrathin layers of SiO_2 onto flexible electronic platforms. The process begins with thermal oxidation of a silicon wafer at $\sim 1,100^\circ\text{C}$. Standard semiconductor processing techniques and/or more recent methods in growth and transfer printing, enable fabrication of high-quality electronics on this layer of oxide, which for the illustrative example here consists simply of a pattern of gold (Au). The transfer consists of bonding the top surface of this substrate onto a thin polymer film (polyimide, 25 μm thick) on a glass substrate as a temporary, rigid support to facilitate manual manipulation. A combination of dry etching steps removes the silicon in a way

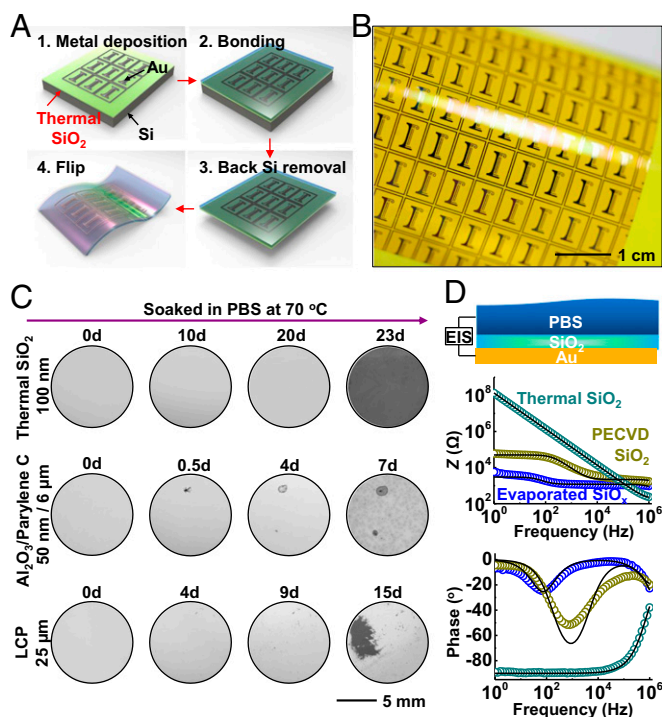


Fig. 1. Materials and integration strategies for use of ultrathin layers of SiO_2 thermally grown on device-grade silicon wafers, as water barriers in flexible electronics. (A) Schematic illustration of schemes for exploiting layers of thermal SiO_2 for encapsulation in test structures: (1) electron beam evaporation, photolithography, and etching of Mg to form "I"-shape patterns as test structures on SiO_2 thermally grown on a silicon wafer; (2) pressure bonding the top surface to a glass substrate that supports a thin film of polyimide (Kapton; 25 μm); (3) removal of the silicon wafer from back side by dry etching; (4) release of the final flexible test structure from the glass substrate. (B) Optical image of a sample produced in this manner, with a $\sim 100\text{-nm}$ -thick layer of thermal SiO_2 on its top surface. (C) Sequential images of Mg encapsulated by layers of thermal SiO_2 and $\text{Al}_2\text{O}_3/\text{Parylene C}$ and a bulk film of liquid crystal polymer (LCP) soaked in PBS solution at 70°C . (D) EIS and modeling results for layers of SiO_2 grown by thermal oxidation and deposited by PECVD and electron beam evaporation.

that terminates at the bottom surface of the SiO_2 (*Materials and Methods*). Peeling the device from the temporary support completes the process, to yield a piece of flexible electronics encapsulated across its entire front surface with a layer of thermal SiO_2 as a defect-free barrier to biofluids, with chronic stability. Unlike traditional processing flows in which deposition of barrier layers occurs last, the scheme reported here starts with a planar, fully formed barrier and then builds device functionality directly on top. Similar growth and transfer processes can deliver a layer of SiO_2 to the bottom of the flexible substrate to prevent biofluid penetration from the back side. Details appear in *Materials and Methods*. Fig. 1B displays an image of a test vehicle that incorporates a front-side layer of SiO_2 with thickness of 100 nm (*SI Appendix, Fig. S1*). These steps can be easily scaled to the largest silicon wafers currently available (450-mm diameter), thereby allowing for systems with overall sizes that can provide nearly full area coverage across any internal organ of the human body. As in semiconductor manufacturing, the cost per unit area will decrease with increasing wafer sizes. In matured manufacturing processes, the costs for implementing these barrier coatings on biomedical implants have the potential to approach costs that are only incrementally larger than those of the wafers themselves.

A thin, uniform layer of magnesium (Mg) (200 nm thick, $\sim 1\text{-cm}^2$ area) formed by electron beam evaporation serves as a convenient

test vehicle for examining the water barrier properties of thin layers of SiO_2 grown and processed in this manner. Here, the strong reactivity of Mg with water [$\text{Mg} + 2\text{H}_2\text{O} \rightarrow \text{Mg}(\text{OH})_2 + \text{H}_2$] quickly produces defects that can be visualized easily by standard microscopy techniques. As shown in Fig. 1C and *SI Appendix, Tables S1 and S2*, a 100-nm-thick layer of thermal SiO_2 survives for 22 d of complete, continuous immersion in phosphate-buffered saline (PBS) solution at pH of 7.4 and a temperature of 70 °C. After this period, the Mg layer dissolves at once, in a spatially uniform fashion across the entire area of the sample. Experiments performed in the same manner but with other candidate barrier materials, including various chemistries, deposition methods, thicknesses, and single/multilayer configurations, provide points of comparison. The results for all cases examined here indicate rapid degradation of the Mg in modes that involve either permeation directly through the barrier materials themselves (e.g., polymers deposited by spin coating), or through isolated, “pinhole” defects in the layers [e.g., silicon nitrides formed by plasma-enhanced chemical vapor deposition (PECVD)]. Specific examples of these intrinsic (former case) and extrinsic (latter case) effects appear in Fig. 1C. The only system, other than thermal SiO_2 , that shows stable operation is a stainless-steel foil with thickness of 50 μm (*SI Appendix, Fig. S2*). This option is, however, not suitable for capacitive, biosensing applications, and it has only limited value in other possible biointerface measurements, such as those based on thermal or optical interfaces. Barrier layers formed by other deposition techniques, such as plasma-assisted atomic layer deposition (ALD), O_3 -assisted ALD, and anodization show pinhole-like defects as well (39–42). For example, although plasma-assisted ALD-deposited SiN_x has a low intrinsic water vapor transmission rate, pinholes lead to extrinsic effects that limit the encapsulation performance of the entire barrier (40). The extent and nature of these types of extrinsic effects are expected to vary depending on the deposition

methods, the deposition tools, and the detailed conditions for deposition and postprocessing, but they are unlikely to reach, on a consistent basis, the completely defect-free levels needed for the uses envisioned here. We note that additional areas of potential application of thermal SiO_2 barriers are in aseptic packaging, food containers, and others. Here, the performance of thermal SiO_2 thin-film barriers surpasses that of polymer-based antimicrobial food packaging layers by many orders of magnitude. Compared with some of the most advanced multilayer systems, such as the Barix barrier (developed by Vitex Systems, Inc.), thermal SiO_2 offers much lower water vapor transmission rates, even at thicknesses that are orders of magnitude smaller (37).

Electrochemical impedance spectroscopy (EIS) analysis of layers of SiO_2 formed by thermal growth and comparisons to those formed by other methods yield additional insights. One can interpret the EIS measurement by the equivalent circuit shown in *SI Appendix, Fig. S3A*. A pinhole-free ideal oxide in contact with the PBS solution can be represented by the solution resistance (R_{sol}) in series with the oxide capacitance (C_{ox}). In practice, the presence of pinholes provides a parasitic branch that contains the resistance of the solution within the pore (R_{po}), in series with a parallel combination of charge transfer resistance (R_{CT}) and double-layer capacitance (C_{dl}).

Fig. 1D presents results obtained in PBS solution. In direct contrast to electron beam evaporated SiO_x and PECVD SiO_2 , thermal SiO_2 exhibits a nearly perfect capacitive response: in the log-log impedance vs. frequency figure (Fig. 1D, *Middle*), a plot of the impedance (Z) as a function of the frequency (f) exhibits a slope of -1 . The results indicate that the oxide defines the total impedance, and that the signal is not corrupted by resistive leakage through pinholes/pores or by direct permeation. The plot in the bottom part of Fig. 1D, *Bottom*, shows that the phase remains fixed at -90° for frequencies up to 10^4 Hz

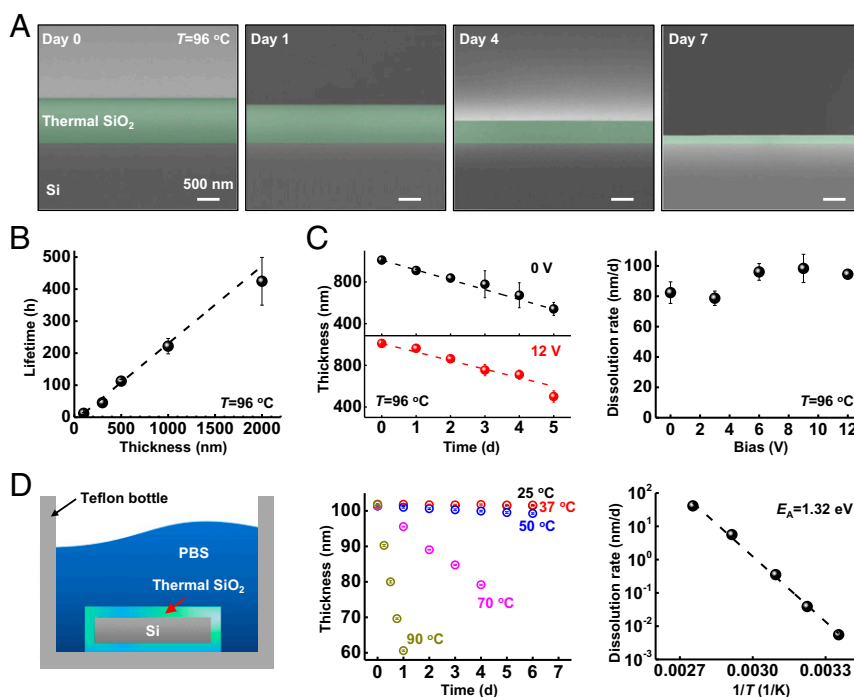


Fig. 2. Failure mechanisms associated with thermal SiO_2 encapsulation layers. (A) SEM images showing decreases in the thickness of a 1,000-nm-thick layer of thermal SiO_2 as a result of soaking in PBS at 96 °C. (B) Time before the leakage current reaches more than 100 nA, for thermal SiO_2 measured in an electrical leakage test (described in *SI Appendix, Fig. S4*). (C) Thickness changes associated with a 1,000-nm-thick layer of thermal SiO_2 without DC bias and with 12-V bias (Left), and extracted dissolution rate for voltages of 0, 3, 6, 9, and 12 V (Right). (D) Thermal SiO_2 on the surfaces and edges of a piece of Si in PBS solution (Left) allowed measurements of changes in thickness at different temperatures (Center). The results indicate a linear relationship between the dissolution rate and $1/T$ (Right).

(capacitive response of a R - C series circuits), as further support of this conclusion. The phase rises to -40° at 10^6 Hz as the solution resistance begins to contribute to the response. The oxide capacitance extracted from the plot (~ 1 nF) is consistent with the known thickness and dielectric constant. Because $C_{dl} \gg C_{ox}$, this parameter does not affect the measurements of thermal SiO_2 (*SI Appendix*, Fig. S3).

Chemical and Physical Effects in Electrical Leakage Through Layers of SiO_2 . Results of electrical leakage tests (see *SI Appendix* for experimental details) conducted using thermal SiO_2 at thicknesses of 100, 300, 500, 1,000, and 2,000 nm at 96°C to accelerate failure-related chemical/physical processes appear in Fig. 2*A* and *SI Appendix*, Fig. S4, with comparison with conventional inorganic and organic materials (*SI Appendix*, Figs. S4 and S5). The results show abrupt transitions to high leakage currents at time durations that depend linearly on the thickness. Fig. 2*A* displays colorized cross-sectional scanning electron microscope (SEM) images of a 1,000-nm-thick layer at various times after immersion. The results indicate a systematic reduction in the thickness, likely due to dissolution by hydrolysis, $\text{SiO}_2 + 2\text{H}_2\text{O} \rightarrow \text{Si}(\text{OH})_4$ (*SI Appendix*, Fig. S6; dissolution occurs also for stainless steel as summarized in *SI Appendix*, Fig. S7). The timescale for complete dissolution is consistent with that for the appearance of large leakage currents, as shown in Fig. 2*B*, which illustrates the linear dependence of lifetime (i.e., time to large leakage current) on thickness. This linear form, and its zero intercept, also suggests that hydrolysis proceeds exclusively by surface reactions without a significant role of reactive diffusion into the bulk of the SiO_2 or of permeation through defect sites. Additional studies show that the dissolution rate for thermal SiO_2 does not depend on electrical bias for values relevant to biointegrated electronics (Fig. 2*C*).

Temperature-dependent studies of the rate of hydrolysis of thermal SiO_2 in PBS reveal additional details. These experiments use thermal SiO_2 grown on all surfaces of the silicon wafer, including its edges (Fig. 2*D*), to avoid any exposed Si, which itself will dissolve according to $\text{Si} + 4\text{H}_2\text{O} \rightarrow \text{Si}(\text{OH})_4 + 2\text{H}_2$ (*SI Appendix*, Fig. S8). The dissolution rates depend exponentially on $1/T$, consistent with Arrhenius scaling and an apparent activation energy $E_A = 1.32$ eV (Fig. 2*D*). This energy is higher than that inferred from previous studies of natural quartz mineral and fused amorphous silica (0.48–1.11 eV) in deionized water or various aqueous solutions (such as NaCl solution), possibly due to the formation of activated complexes on the surfaces of SiO_2 in PBS (43, 44). For comparison, measurement of the dissolution rate at a pH of 7.4 and 70°C yields a value of 5.6 nm/d (2.9×10^{-13} mol/cm 2 ·s), which is roughly one order of magnitude higher than that of quartz or amorphous silica in deionized water at the same temperature (44, 45). This increase is likely due to an expected “salt effect” that leads to enhanced reaction rates in PBS (46). From these measurements, a multiphysics computational model for the temperature and pH dependence of the dissolution rate has been developed and validated (*Materials and Methods*). The dissolution rate is found to have a half-order dependence on hydroxide concentration (*SI Appendix*, Fig. S9). Simulations can yield estimates of the lifetime of thermal SiO_2 layers for pH values ranging from 7 to 12, and temperatures from 25 to 90°C . At a pH of 7.4 and 37°C , the dissolution rate for thermal SiO_2 is $\sim 4 \times 10^{-2}$ nm/d, corresponding to a lifetime of nearly 70 y. This timescale exceeds the lifetime of most patients who might benefit from chronic flexible electronic implants, for a layer with thickness of 1,000 nm, sufficiently thin to meet the key requirements outlined previously.

Theoretical Modeling. Reactive molecular dynamics (RMD) simulations (Fig. 3*A* and *B*) provide some additional insights into the dissolution chemistry. Fig. 3*A* presents schematic illustrations of the simulation box explained in detail in *Materials and Methods*.

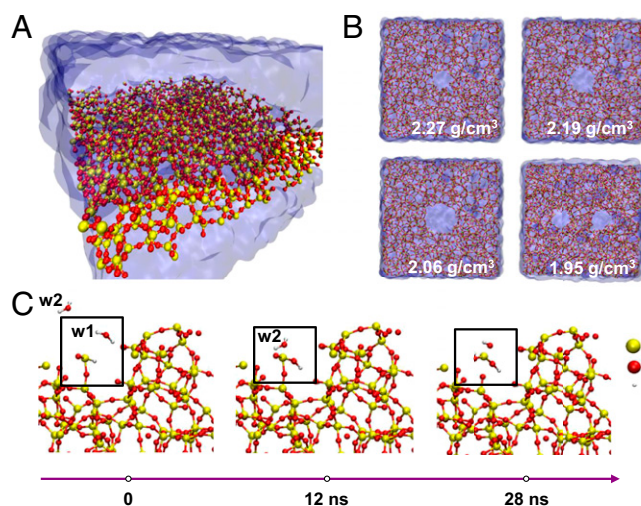


Fig. 3. Reactive molecular dynamics (RMD) simulations of hydrolysis of defective layers of SiO_2 . (A) Perspective snapshot of the SiO_2 slab in water. (B) Top-view representation of four different oxide densities of the SiO_2 slab in water. (C) Simulation snapshots of hydrolysis reactions that lead to the dissociation of one molecule of SiO_2 from the structure.

Adding/removing protons from the system provides a means to adjust the pH of the surrounding bath that is free of ions. As shown in Fig. 3*B*, adding void-like defects in a perfect material serves as a route to reduce the effective density, motivated partly by previous work that shows that voids and defects larger than 1 nm can exist in SiO_2 structures (47, 48). Fig. 3*C* depicts snapshots of sequential reactions that lead to the dissociation of Si from a surface defective site, with a dangling Si–OH, or Si–H bond. On average, $\sim 80\%$ of the Si in the oxide layer are OH terminated and $\sim 20\%$ are H terminated. Analysis therefore focuses on the dissolution chemistry of the former. The frame on the left ($t = 0$ ns) shows two water molecules (labeled w1 and w2) that approach a Si atom at the location of a Si–OH bond. At $t = 12$ ns, the hydrogen of molecule w1 dissociates and forms a bond with the H from the –OH–terminated Si and yields H_2 . This reaction increases the length of the bond between the Si and the O on the bottom side from 2.3 to 2.95 Å, with a corresponding reduction in its strength. At $t = 28$ ns, molecule w2 approaches the Si and one of its hydrogen atoms dissociates in the vicinity of the dissolution site (Fig. 3*C*). This hydrogen chemically bonds with the dangling O of the Si. Cleavage of the previously weakened Si–O bond releases the ionic species $\text{Si}(\text{OH})_2^{2+}$. The w2 remains as OH^- for an additional 3 ns and forms a water molecule by bonding with another H^+ at $t = 31$ ns. The conversion of $\text{Si}(\text{OH})_2^{2+} \rightarrow \text{Si}(\text{OH})_4$ finishes at 80–90 ns at $T = 37^\circ\text{C}$, such that the final product of dissolution is silicic acid, similar to findings from previous studies of dissolution of bulk Si using comparable models (49). These reaction products appear within the 35-ns timescale of the simulations presented here under accelerated conditions, that is, at 100°C , $\text{Si}(\text{OH})_2^{2+} \rightarrow \text{Si}(\text{OH})_3^+ \rightarrow \text{Si}(\text{OH})_4$ occurs in ~ 32 ns (*SI Appendix*, Fig. S10). Simulation results of different mass density, influence of defects, and temperature dependence on intermediate products during Si hydrolysis are detailed in *SI Appendix* (*SI Appendix*, Figs. S11 and S12).

Water Barriers Demonstrated in Key Electronic Devices. The overall process outlined in Fig. 1*A* provides versatility for application with nearly any class of silicon or silicon-compatible electronic systems, and with other forms of flexible electronics. Resistors, capacitors, p-n diodes, and metal–oxide–semiconductor field effect transistors (MOSFETs) based on silicon nanomembranes serve as examples, each constructed with a 1- μm -thick layer of

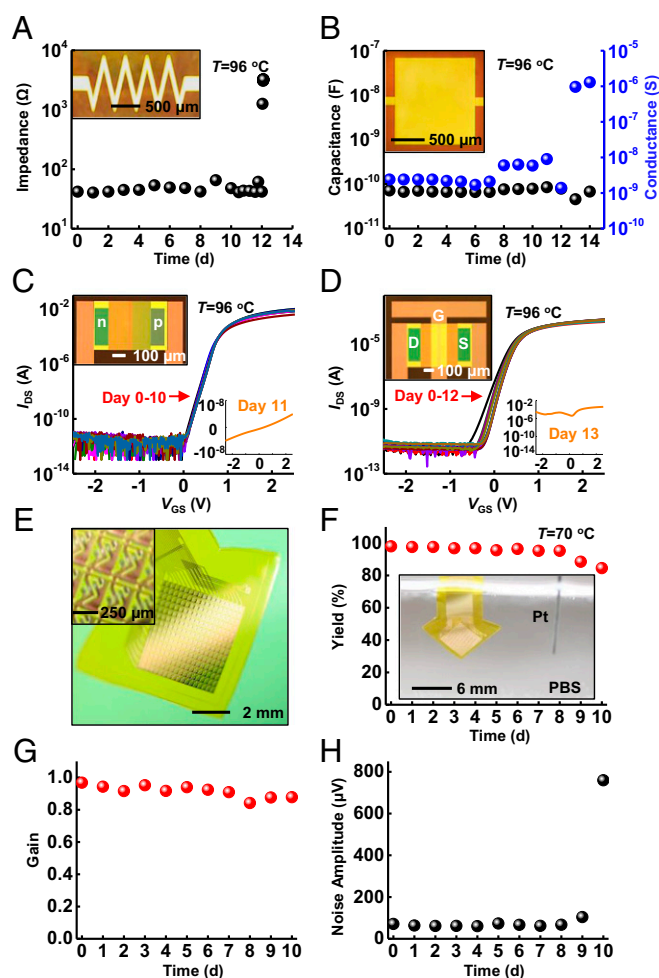


Fig. 4. Demonstration of electronic devices and flexible electronic systems encapsulated with thermal SiO₂. (A–D) Results of soak tests of resistors, capacitors, diodes, and *n*-type metal–oxide–semiconductor transistors with optical images (*Insets*). Tests in PBS solutions at 96 °C indicate that failure occurs at day 12 for all devices. (E) A photograph of a platform of active multiplexed flexible electronics with double-sided thermal SiO₂ encapsulation in a slightly bent configuration. The *Inset* presents a magnified view of the sensing sites, each of which consists of one sensing transistor and one multiplex transistor connected in series. (F–H) Accelerating soak test with in vitro measurement of electrical performance including yield (Y_{Y₀}, defined as the number of working sensing sites divided by the total number of sites), gain (the ideal gain is 1), and mean noise rms. The results indicate device stability throughout 9 d in 70 °C PBS. The *Inset* in F presents a photograph of an active multiplex device fully immersed in PBS.

thermal SiO₂ (Fig. 4 A–D, *SI Appendix*, Fig. S13, and tested in the manner illustrated in *SI Appendix*, Fig. S4, *Left*). All devices retain functionality, without measurable change from their initial state, during complete immersion in PBS at 96 °C (*SI Appendix*, Figs. S14 and S15). The SiO₂ fully dissolves in 12 ± 1 d, consistent with data presented previously. At this time, all devices fail suddenly and catastrophically. For example, the resistor behaves as an open circuit (Fig. 4A). For the capacitor, ions penetrate into the polyimide dielectric, which significantly increases the capacitance and contributes to leakage current across this layer (Fig. 4B). The characteristics of the diode and the *n*-channel MOSFET change to resemble those of a resistor, as illustrated in Fig. 4 C and D. As described previously, an additional transfer step can integrate a layer of thermal SiO₂ on the back side of the polyimide substrate, to prevent water penetration through this surface. *SI Appendix*, Fig. S16A, shows a sample with this type of

design, in which a patterned layer of Mg persists unchanged for up to 15 d during complete immersion (without well structure) in PBS at 70 °C. Under similar conditions, samples without the thermal SiO₂ layer on the back side of the polyimide fail within a few hours due to water permeation directly through the polyimide (*SI Appendix*, Figs. S16 and S17). *SI Appendix*, Fig. S18, demonstrates applicable flexibility of this design with 5 mm of bending radius.

In addition to water, ions present in biofluids such as Na⁺ and K⁺ can also degrade/alter performance, particularly in active semiconductor devices. For example, proximity of Na⁺ to the conducting channel of a MOSFET causes its threshold voltage to shift. The challenge is that these and other ions have a non-negligible mobility inside the bulk of the thermal SiO₂ material. The transport is, in general, dependent on electric field, such that operation of the device can enhance this drift. When the ion transport is drift dominated, the failure time is proportional to the ion transition time $\tau_{trans} = h/\mu\xi = h^2/\mu V = kTh^2/DqV$, where h is the thickness of thermal SiO₂, μ is the mobility of the ion, ξ is the internal electric field, V is the voltage across the SiO₂, k is the Boltzmann constant, T is temperature, D is the diffusivity of the ion, and q is the charge. In practice, the lifetime increases significantly with reductions in voltages (for a fixed thickness) and/or increases in thickness (at fixed voltage). Self-consistent simulations described in *Materials and Methods* show that ions accumulate inside the thermal SiO₂ where they can change the potential distribution in a manner that alters the transport (*SI Appendix*, Figs. S19 and S20). Solutions to the coupled drift-diffusion and Poisson's equation for Na⁺ indicate that devices last several times longer than expected based on purely drift-dominated transport (which provides the lower bound for device lifetime; *SI Appendix*, Fig. S21). Penetration of ions can be further retarded by the incorporation of high-quality silicon nitride or phosphosilicate glass, as adopted by the semiconductor industry since the 1980s (50, 51). An ideal barrier for both water and ions may come from thin layers of thermal nitride, oxide/nitride bilayers, or even oxynitrides. Exploration of these possibilities is a topic of current work.

Integration of 900-nm thermal SiO₂ as encapsulation for actively multiplexed electronics designed to allow high-speed spatiotemporal mapping of biopotentials highlights the compatibility of the materials and concepts introduced here with the most sophisticated classes of flexible electronics. Fig. 4E and *SI Appendix*, Fig. S22, present exploded view schematic illustrations of the system and an image of a completed device with top- and bottom-side thermal SiO₂ encapsulation, respectively. This platform provides 252 sensing sites (18 rows by 14 columns) with silicon transistors at each site for actively multiplexed addressing, over an area of 4.5 mm × 4.6 mm. The multiplexing is realized by connecting a pair of transistors in series, one of which functions for capacitive sensing of biopotentials through thermal SiO₂ by connecting its gate terminal to an electrode pad. The other transistor serves as a switch to allow multiplexed readout from the sensing site (*SI Appendix*, Figs. S23 and S24). In addition to its barrier role, the front-side SiO₂ layer acts as the dielectric layer for capacitive coupling. Fig. 4 F–H shows excellent yield, stable high average gain values with low noise operation during complete immersion in PBS solution at 70 °C for 10 d. *SI Appendix*, Fig. S25, illustrates robust performances in bending test. Although the approaches presented here do not encapsulate the exposed edges at the periphery of the overall device platforms, this constraint seems to have little practical effect on the lifetimes for the cases examined. One potential limitation is that SiO₂/polymer interface might suffer from delamination, especially under external stimuli such as thermal cycles (52). Ongoing efforts seek to eliminate edges entirely by use of slightly oversized layers of thermal SiO₂ together with SiO₂/SiO₂ bonding chemistries adapted from the semiconductor industry.

Conclusions

In summary, the results presented here establish materials strategies and integration schemes for use of ultrathin layers of SiO₂

thermally grown on device-grade Si wafers as long-lived water barriers for active, flexible electronic systems. Comparisons against conventional encapsulation strategies highlight the advantages. Detailed experimental and theoretical investigations reveal that a slow hydrolysis process defines the ultimate lifetimes, consistent with the exceptionally high quality of SiO₂ films formed and manipulated in the schemes introduced here. In regimes of thicknesses compatible with mechanically flexible form factors, and in layouts that can support high-quality electrical interfaces, accelerated testing and modeling at both atomistic and continuum length scales suggest robust operation over many decades at physiological temperatures. Results presented here used PBS as the test solution. Lifetimes in biofluids may be somewhat different, due to differences in composition. Demonstrations at wafer-level sizes and in dual-sided encapsulation geometries illustrate the scalability of these approaches to devices of relevance for nearly all envisioned applications in biointegrated electronics. It is important to acknowledge practical difficulties in application of the ideas presented here to systems with challenging topography such as those that involve arrays of penetrating pin-type electrodes. Future efforts include developing schemes to address

such applications, exploring advanced embodiments that can inhibit both water and ion permeation, and implementing these concepts in electronic and optoelectronic devices for neural and cardiac applications.

Materials and Methods

Details of fabrication steps, device structures of Mg tests, impedance measurement, and electrical leakage tests are shown in [SI Appendix](#). Theoretical analysis including EIS modeling, multiphysics simulations of thermal SiO₂ dissolution, molecular simulations, and sodium ion transport simulations also appear in [SI Appendix](#).

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Ultra-thin, Transferred Layers of Thermally Grown Silicon Dioxide as Biofluid Barriers for Bio-Integrated Flexible Electronic Systems

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Supplementary Information

Supplementary Note 1

Supplementary Figure Legends

Supplementary Figure S1-S25

Supplementary Table S1 and S2

Supplementary Note 1: Materials and Methods

Fabrication Methods for Devices and Test Structures with Thermal SiO₂ Barrier Layers

Fabrication of samples with layers of thermal SiO₂ as encapsulation began with wet oxidation (in O₂/H₂O) at high temperatures (typically at ~1150 °C) on the surfaces of standard silicon wafers (100-1000 nm thermal SiO₂, 500 μm Si substrate, 100 mm diameter, University Wafer). A mechanical grinding process (with an initial coarse grind and a final fine grind to achieve mirror like finish with thickness variance under 5 μm) reduced the thickness to 200 μm (Sygarus Systems). Photolithography and wet etching patterned layers of Ti/Mg (5 nm/100 nm) deposited by electron-beam evaporation into targeted resistor shapes (*SI Appendix*, Fig. S13A). For the capacitors (*SI Appendix*, Fig. S13B), sequential deposition and photolithography patterning of two layers of Cr/Au (5 nm/ 100 nm) between a dielectric layer of polyimide (1.5 μm, PI-2545, HD Microsystems) yielded simple, parallel-plate designs (1 mm×1 mm capacitor plate). For the diodes and NMOS devices (*SI Appendix*, Fig. S13C and D), transfer printing delivered devices prefabricated on an SOI substrates using previously reported recipes onto the SiO₂/Si substrate, forming the Si nanomembrane diode and transistor (channel length $L = 600\ \mu\text{m}$, width $W = 20\ \mu\text{m}$, thickness $t = 100\ \text{nm}$). A layer of Cr/Au (5 nm/100 nm) served as metal interconnects to reach probe pads outside the PDMS well (*SI Appendix*, Fig. S14A-C). For each type of device,

spin-coating, soft-baking and curing formed an overcoat of polyimide (PI-2545, HD MicroSystems) with a thickness of 3.5 μm . ALD produced a layer of Al_2O_3 on the polyimide, to facilitate bonding to a thick layer of polyimide (25.4 μm , Kapton, DuPont) coated with a bilayer of Ti/ SiO_2 (5 nm/100 nm) deposited by electron-beam evaporation and laminated on a glass slide with a layer of PDMS. The bonding involved application of a commercial adhesive (Kwik-Sil, World Precision Instruments) applied at a pressure of ~ 50 kPa and cured at room temperature. Reactive ion etching (RIE) with SF_6/O_2 (Plasma Therm) followed by Inductively Coupled Plasma RIE (ICP-RIE, Surface Technology System) with SF_6 removed the Si substrate to leave a largely unaltered, pristine surface of the SiO_2 as a biofluid barrier and bio-interface.

Mg Test Structures for Evaluation of Water Barrier Performance of Conventional Materials

Photolithography with a positive photoresist (AZ nLOF 2070, MicroChemicals) formed 1 cm^2 square area on a clean glass substrate. Subsequent electron-beam evaporation and lift-off yielded a layer of Ti/Mg (5 nm/300 nm) in the pre-defined area. Various deposition techniques yielded different types of encapsulation layers for soak testing in PBS (*SI Appendix*, Table S1 and Table S2). Spin coating then prepared a photo-definable epoxy (SU-8 2000, MicroChem), polyimide (PI-2545, HD MicroSystems) and PDMS. PECVD formed SiO_2 and SiN_x both with deposition frequencies of 13.56 MHz. Al_2O_3 and HfO_2 were grown by ALD at 150 $^\circ\text{C}$.

SI Appendix, Table S1 and S2 summarizes all of the Mg test results. Popular organic passivation materials, for instance, SU-8 and PDMS, failed within 1 day at body temperature, indicating poor water barrier quality. Inorganic/organic multilayers can be more effective than simple bilayers with the same overall thickness due to the tortuous paths for water permeation through defects and interfaces in multiple layers. In certain cases, however, such as with

Parylene C, the multilayer yields poor results, possibly due to non-trivial thickness dependent effects for permeation through Parylene C.

Impedance Measurements and Modeling

Impedance measurements used a Gamry Reference 600 potentiostat system (Gamry Instrument). The SiO₂ coated Au electrodes individually connected as the working electrode, with the Ag/AgCl as the reference electrode and a Pt wire as the counter electrode. The experiments used an AC potential of 10 mV with a frequency range of 1 Hz to 1 MHz, and a DC bias of 1 V. PBS solution served as the electrolyte at room temperature. Analysis used an equivalent circuit model shown in *SI Appendix*, Fig. S3, where R_s is the solution resistance, C_c represents the capacitance of pristine material, and R_{po} is the cumulative resistance of all pores, pinholes, microcracks and other defects. Additional liquid/metal interfaces form as the solution penetrates the coating. R_{CT} corresponds to the charge transfer resistance and C_{dl} is the double-layer capacitance associated with these interfaces. In all three types of SiO₂ materials:

$$C_c = \frac{\epsilon_r \epsilon_0 A}{t} \approx 0.86 \text{ nF}$$

where the coating area $A = 0.25 \text{ cm}^2$, thickness $t = 1 \text{ }\mu\text{m}$, relative permittivity $\epsilon_r = 3.9$ and vacuum permittivity $\epsilon_0 = 8.854 \times 10^{-12} \text{ F} \cdot \text{m}^{-1}$. Non-linear least squares fitting yielded values for the various parameters.

Results for SiO₂ formed by electron beam evaporation and PECVD interpreted using similar methods suggest pore resistances and charge transfer resistances that originate from defect sites (*SI Appendix*, Fig. S3). Moreover, in these material systems, C_{dl} cannot be ignored. As expected from the EIS model, the phase response is characterized by two valleys both for these cases. The

lower valley ($\sim 10^2$ Hz for evaporated and $\sim 10^3$ Hz for PECVD materials) can be attributed to R_{po} and R_{CT} in parallel with C_{dl} . The valley at 10^6 Hz arises from the oxide capacitance and the solution resistance. Discrepancies between theory and experiment likely reflect limitations of the assumption that the pore/pinhole regions and the rest of the otherwise undamaged regions can be treated as parallel branches for charge transfer. In practice, the flow may be two-dimensional. In addition, the complexity of the electrode surface may require a modified representation for C_{dl} (ref. 1). Nonetheless, the simple compact model captures the general trends of the experimental findings, and it is sufficiently sophisticated to identify qualitative differences between thermally grown and deposited forms of SiO_2 , and their critical role in barrier performance.

Electrical Leakage Tests

Measurements of electrical leakage for different thicknesses of thermal SiO_2 and other conventional oxides as an additional comparison involved application of a voltage, comparable to that relevant for operation of standard electronics, between a surrounding bath of PBS and an underlying doped silicon wafer, as in *SI Appendix*, Fig. S4A and Fig. S5. These studies involved PECVD or ALD to form thin layers of SiO_2 or Al_2O_3 on n-type Si wafers ($1\text{--}10\ \Omega\cdot\text{cm}$), and SiO_2 grown thermally. In these tests, the wafer connects to the cathode to prevent the possibility of anodizing the silicon; the anode is a wire of platinum in the PBS solution. A well structure made of poly(dimethylsiloxane) (PDMS) confines the PBS to the central regions of the layers ($\sim 1\ \text{cm}^2$), thereby eliminating any effects of the edges of the samples. Ultraviolet ozone (UVO) treatment of the surfaces of these materials and the bottom surfaces of PDMS well ($\sim 1\ \text{cm}$ in depth) structures enabled strong bonding upon physical contact, thereby yielding a waterproof seal around an exposed area of $1\ \text{cm}^2$. The well formed in this way confined the PBS solution during

the course of the testing. A Platinum (Pt) electrode dipped into the PBS served as an anode and the n-type Si substrate served as the cathode for measurements with the potentiostat system with two-terminal configuration under a constant 3 V DC bias.

As shown in *SI Appendix*, Fig. S4, at a pH of 7.4 and a temperature of 37 °C, leakage currents quickly (within 60 hours) reach levels that significantly exceed 10^{-6} A/cm² for 100 nm thick layers of PECVD SiO₂, and ALD Al₂O₃. Most polymers, including photocurable epoxies (SU-8) and elastomers such as PDMS exhibit leakage almost instantaneously after immersion in PBS solution (*SI Appendix*, Fig. S5). At the same thickness, thermal SiO₂ exhibits zero leakage, to within measurement uncertainties, throughout the 350-hour duration of the experiment. Leakage current here is a function of applied voltage for different organic layers at room temperature.

Measurement and Modeling of Rates of Dissolution of Thermal SiO₂

These measurements used pieces of Si wafers (1 cm × 2 cm dies) with thermal SiO₂ layers (100 nm thickness) grown across the top and bottom surfaces and the edges. Soaking occurred in plastic bottles containing PBS solution (25-30 ml) at room temperature, 37 °C, 50 °C, 70 °C and 90 °C separately. Ellipsometry defined the thickness of the SiO₂ as a function of soaking time.

Measurement results were also utilized to validate multiphysics models of the dissolution process coupling of all relevant continuum-scale physics: chemical species transport (using the Nernst-Planck equations), chemical reaction kinetics, electrostatics, and moving boundaries. Reaction kinetics were modeled using the Arrhenius form, with rate constant and activation energy for the primary SiO₂ dissolution reaction calculated from measurements and those of other reactions (forward and backward ionization of salts, PBS and water self-ionization) estimated to proceed much more quickly than SiO₂ dissolution. As seen in *SI Appendix*, Fig. S9A,

the dissolution rate is dominated by a half-order dependence on hydroxide concentration. The moving boundary velocity was calculated based on a mass balance at the boundary interface based on the local dissolution rate and assuming a baseline density of 2.19 g/cm^3 . This model allows the time-dependent evolution of a SiO_2 layer with arbitrary initial thickness to be directly calculated and visualized for arbitrary pH and temperature, and the lifetime to be predicted (*SI Appendix*, Fig. S9B). Simulations were performed on both 2-D and 3-D geometries using COMSOL Multiphysics®.

Reactive Molecular Dynamics (RMD) Simulations

Reactive Molecular Dynamics (RMD) simulations provided molecular insights into the effects of temperature and defects/oxide density on the dissolution process. The RMD used the Reaxff potential, integrated in a Large-scale Atomic/Molecular Massively Parallel Simulator (LAMMPS) package(2, 3). Previous work establishes the accuracy of this potential for interactions between SiO_2 and H_2O , through comparison to the macroscale experimental properties of these interfaces(4). The calculations involved initially pristine slabs of SiO_2 (density of 2.33 g/cm^3 and thickness of 2 nm, in lateral dimensions of $5 \text{ nm} \times 5 \text{ nm}$) solvated in water (Fig. 3A). Removing a few SiO_2 molecules from the center of the slab yielded effective oxide densities of 2.27, 2.19, 2.06 and 1.95 g/cm^3 , each of which was then solvated again in water (Fig. 3B). The pH of the solution was fixed at 7.4 by balancing the number of protons in the system. Periodic boundary conditions were applied in all the directions. Energy minimization of the system was performed for 1,000,000 steps. The time step was 0.1 fs(ref. 5). The Nosé-Hoover thermostat(6) held the temperature constant. Simulations included 10 runs at temperatures between 10°C - 100°C at intervals of 10°C , for each oxide density. To generate statistical data, five replicas were

performed for each set. The presented data correspond to the average of five simulation runs, each for a total of 35 ns with data collection at 0.1 ps intervals.

The root mean square displacement (RMSD) of each Si atom in each simulation step defined the dissociation events. In particular, the RMSD of bound Si atoms is 1.56 Å. Upon dissociation, this value sharply increased to >10 Å. The molecular species associated with the dissociated Si was defined by the atoms that exist within a distance of 3.2 Å from the center of the Si.

Similar simulations can yield results on the influence of mass density and the density of pinhole defects (Fig. 3B and *SI Appendix*, Fig. S11). As might be expected, the number of Si dissolution events is highest for the lowest density (1.95 g/cm³) and the highest temperature (100 °C) (*SI Appendix*, Fig. S11A). Specifically, the dissolution process increases exponentially with temperature (for temperatures between 10 °C and 100 °C) and density (for densities between 1.95 and 2.33 g/cm³, at 80 °C and 100 °C), respectively (*SI Appendix*, Fig. S11). The rate of dissociation from defective sites greatly exceeds that from pristine sites, thereby suggesting that most dissolution occurs at defective/low density regions (*SI Appendix*, Fig. S12A). This phenomenon is consistent with the defect-assisted dissolution mechanisms presented elsewhere(7, 8). Although the modeling involves many simplifying assumptions, both of these trends are qualitatively consistent with experimental results. The dissolution rates, for all densities, increase with temperature in an Arrhenius manner, consistent with the previous studies(9, 10, 11).

In addition to these qualitative insights, the results allow quantitative extraction of weighted activation energies of dissolution for different densities, based on the ratio of the population of dissolution events (P and P_0) at corresponding temperatures (T and T_0) according to the Boltzmann distribution law, $E = -K \ln(\frac{P}{P_0}) / (\frac{1}{T} - \frac{1}{T_0})$, where K is a constant. *SI Appendix*,

Fig. S12B summarizes the results normalized by the maximum E . The findings suggest that the energy needed to dissociate Si atoms from oxide layers with densities of 1.95 g/cm^3 is 70% of that for layers with densities 2.33 g/cm^3 . The energy for dissociation increases with the density. This trend is consistent with previous experimental observations on deposited/grown oxides(11). Previously mentioned multiphysics models coupling reactive diffusion kinetics with electrostatics and moving boundaries can capture certain aspects based on continuum, non-atomistic effects(11). The results presented here complement the continuum modeling work by suggesting that low-density oxides present additional Si-OH dangling sites and therefore accelerated chemical reaction rates.

In order to see the intermediates and final products of Si in the solution, the simulation tracked the molecular identity of each Si which is dissolved in different temperatures. Simulations show that Si first forms Si(OH)_2^{2+} and dissolves into solution. In the solution Si(OH)_2^{2+} forms bonds with two more OH^- groups to yield Si(OH)_4 (ref. 12). The timescale for the reaction $\text{Si(OH)}_2^{2+} \rightarrow \text{Si(OH)}_4$ is 60-70 ns at 37°C (ref. 12). Results did not indicate any Si(OH)_2^{2+} conversions for temperatures below 80°C within the simulation time i.e. 35 ns while at 80°C and 90°C , the simulation observed the $\text{Si(OH)}_2^{2+} \rightarrow \text{Si(OH)}_3^+$ (*SI Appendix*, Figure S12). For 100°C , we the reaction $\text{Si(OH)}_2^{2+} \rightarrow \text{Si(OH)}_3^+ \rightarrow \text{Si(OH)}_4$ occurs in 32 ns. The hypothesis is that high temperatures boost the conversion of intermediates and the formation of Si(OH)_4 .

Cyclic Bending of Active Electronics with Thermal Oxide Encapsulation

As shown in *SI Appendix*, Fig. S25, cyclic bending test was applied to the flexible electronic system with dual-side thermal oxide encapsulation by bending the device to a radius of 5 mm for

10,000 cycles. Yield, gain and mean noise RMS remain nearly unchanged after 10,000 bending cycles.

Sodium Ion Transport Simulations

Modeling of sodium ion transport processes used the drift-diffusion equation and Poisson's equation. These equations were solved on a one-dimensional domain shown in *SI Appendix*, Fig. S19 using COMSOL Multiphysics®. A value of the diffusivity (D) of Na^+ in wet thermal SiO_2 from previous reports allowed calculation of the corresponding ion migration mobility (μ) using the Nernst-Einstein relation(13). Physically, $x = 0$ and $x = h$ correspond to the PBS/ SiO_2 and SiO_2/Si interfaces, respectively, where h is the thickness of thermal SiO_2 . The boundary condition for the drift-diffusion equation is $[Na^+] = 2 \times 10^{25} m^{-3}$ at $x = 0$. This value corresponds to the solid solubility limit of Na^+ in wet thermal SiO_2 because the concentration of Na^+ in PBS solution is a very large $[8.24 \times 10^{25} m^{-3} (137 mmol/L)]$. At $x = h$, the simulation used a reflective boundary condition based on the assumption that Na^+ diffusivity inside the underlying Si is so low that most Na^+ ions are reflected at the SiO_2/Si interface. The boundary conditions for the electrostatic potential are $V = V_{app}$ at $x = 0$ and $V = 0$ at $x = h$. The assumption is that the resistance of SiO_2 is much larger than the PBS solution. The voltage drops primarily across the oxide layer.

SI Appendix, Fig. S20 shows the Na^+ concentration and potential distribution within a thick ($h = 900 nm$) SiO_2 layer at 37 °C after 2 years of operation. The potential bias V_{app} swept from 0 V to 2 V with an increment of 0.5 V. The Na^+ concentration decreases significantly near $x = 0$ and Na^+ accumulates at the other side, namely, at $x = 900 nm$. A time-dependent rise in the potential barrier retards the Na^+ transport process. In this simulation, failure corresponds to the

point at which the shift in the threshold voltage ΔV_T for an 100 nm equivalent oxide thickness (EOT) reaches 1 V. ΔV_T can be expressed as a function of spatially distributed Na^+ density(14):

$$\Delta V_T(t) = \frac{1}{C_0} \left[\frac{1}{h} \int_0^h x \cdot \rho_{Na^+}(x, t) dx \right]$$

where C_0 is the gate capacitance.

SI Appendix, Fig. S21A shows ΔV_T as a function of time with different bias voltages. The red dashed horizontal lines correspond to the failure criteria of threshold voltage shift. In *SI Appendix*, Fig. S21B, a normalization of the time to $\tau_{trans} = \frac{h}{\mu\xi} = \frac{h^2}{\mu V} = \frac{kTh^2}{DqV}$ corresponds to the drift-dominated ion transport with time-independent linear potential drop. In other words, this transport time does not account for charge accumulation self-consistently. If self-consistent were unimportant, the lines would be scaled to a universal curve which cross the horizontal threshold voltage line at $t/\tau_{trans} = 1$. However, the curves in *SI Appendix*, Fig. S21B all shift to the right, i.e. a longer failure time. This non-linear electric field dependency arises from changes in the potential associated with spatially distributed Na^+ .

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Supplementary Figure Captions

Fig. S1. The SEM image in a 45° view of a ~100-nm-thick thermal SiO₂ above the polyimide layer, of the test vehicle shown in Fig. 1B.

Table S1. Summary of Mg soak tests for different candidate barrier materials.

Table S2. Summary of properties of all different encapsulation strategies examined.

Fig. S2. Mg soak test of a 50-μm-thick stainless steel foil in 70 °C PBS solution throughout 84 days.

Fig. S3. Theoretical modeling of EIS measurement of different SiO₂. (A) Equivalent circuit consists of both pristine and defective parts. (B) Parameters used for SiO₂ produced by evaporation, PECVD and thermally grown.

Fig. S4. (A) Schematic illustration of the two-terminal potentiostat system (*left*) used to measure leakage current through 100-nm-thick layers of PECVD SiO₂, ALD Al₂O₃ and thermal SiO₂ at 37 °C. Measurements involved a 3V DC bias continuously applied between a Pt electrode immersed in the PBS solution and a highly doped n-type silicon substrate using a two-electrode configuration. The results (*right*) highlight that thermal SiO₂ maintained leakage current below 100 nA throughout 360 hours while both PECVD SiO₂ and ALD Al₂O₃ failed within 50 hours. (B) Leakage currents associated with thermal SiO₂ encapsulation layers with different thickness at 96 °C.

Fig. S5. Leakage current as a function of applied voltage for different organic layers with a thickness of 1 μm, tested at room temperature.

Fig. S6. The SEM image in a 45° view of a 1000 nm thermal SiO₂ dissolved after accelerating PBS soak test at 96 °C, compared with unchanged thickness in the area of PDMS covered side.

Fig. S7. A sequence of SEM images in a 45° view illustrate dissolution of the 50-μm-thick stainless steel foil in accelerating PBS soak test at 96 °C throughout 60 days.

Fig. S8. The edge effect in thermal SiO₂ dissolution rate test.

Fig. S9. Multiphysics simulations of thermal SiO₂ dissolution. (A) Dissolution rate dependence on pH (Order 1: $k_0=3.85\times10^9 \text{ m}^4\text{mol}^{-1}\text{s}^{-1}$, Order 0.5: $k_0=6.11\times10^7 \text{ m}^{2.5}\text{mol}^{-0.5}\text{s}^{-1}$, Order 0.25: $k_0=7.68\times10^6 \text{ m}^{1.75}\text{mol}^{-0.25}\text{s}^{-1}$). (B) Visualization of layer after 0 and 300 days separately (pH = 7.4, $T = 50 \text{ }^\circ\text{C}$).

Fig. S10. Number of reaction products during simulation of Si dissolution at $100 \text{ }^\circ\text{C}$.

Fig. S11. Theoretical analysis of density and temperature effect on Si dissolution. (A) Number of Si dissolved in different temperatures and for different oxide densities. (B) Number of Si dissolved for different oxides at temperatures $80 \text{ }^\circ\text{C}$ and $100 \text{ }^\circ\text{C}$.

Fig. S12. (A) The probability of SiO₂ dissolved from defective sites versus pristine regions. (B) Weighted activation energy associated with reaction of SiO₂ dissolution as a function of oxide density. (C) Number of Si compounds that exist in the solution at different temperatures.

Fig. S13. (A-D) Cross-sectional sketch of resistors, capacitors, diodes and NMOS transistors.

Fig. S14. Optical microscope images of capacitor (A), p-n diode (B) and MOSFET (C) encapsulated with 1,000-nm-thick thermal SiO₂ for accelerating soak test. Device part sealed in PDMS well, with gold metal wire extended to contact pad.

Fig. S15. Electrical characteristics of control devices including capacitor (A), p-n diode (B) and MOSFET (C) in PBS soak test at $96 \text{ }^\circ\text{C}$.

Fig. S16. Cross-section illustrations of Mg device with double-sided thermal SiO₂ encapsulation layers (A), and control device (B).

Fig. S17. $70 \text{ }^\circ\text{C}$ PBS soak test of Mg device with double-sided thermal SiO₂ encapsulations (A), and control device (B).

Fig. S18. Bending the Mg device with double-sided thermal SiO₂ encapsulations to a radius of 5 mm exhibits high flexibility.

Fig. S19. Set up of sodium ion transport simulation with constant boundary condition at $x = 0$ and reflective boundary condition at $x = h$.

Fig. S20. Na⁺ concentration and potential distribution within thermal SiO₂ ($h = 900 \text{ nm}$) layer at the end of 2-years simulation at $T = 37 \text{ }^\circ\text{C}$.

Fig. S21. ΔV_T threshold voltage shift as a function of time (A) and normalized time (B) with different SiO₂ bias voltage at $T = 37$ °C.

Fig. S22. Exploded-view schematic illustration of sensing system with top and bottom side thermal SiO₂.

Fig. S23. Images of active multiplexed electronics in four key fabrication steps: 1. isolated Si transistors above thermal SiO₂; 2. photolithographic patterning of 1st metallization for source, drain, gate (connected to sensing electrode pad) and row wires for multiplexing; 3. 2nd metallization of the column wires for signal output; 4. final device layout after removing Si substrate with exposed thermal SiO₂ as frontside encapsulation.

Fig. S24. Si transistor performances of the active multiplexed electronics. (A) Optical microscope image of a test transistor layout. (B) Transfer characteristics in both linear and semi-log scale, with supply voltage $V_{DS}=0.1$ V. (C) Output characteristics, V_{GS} ranging from -1 V to 4 V with a step of 1 V.

Fig. S25. (A-C) Yield, gain and mean noise RMS remain unchanged after 10^4 bending cycles. Inset in the left figure shows a photograph of a device bent to a radius of ~5 mm on a glass tube.

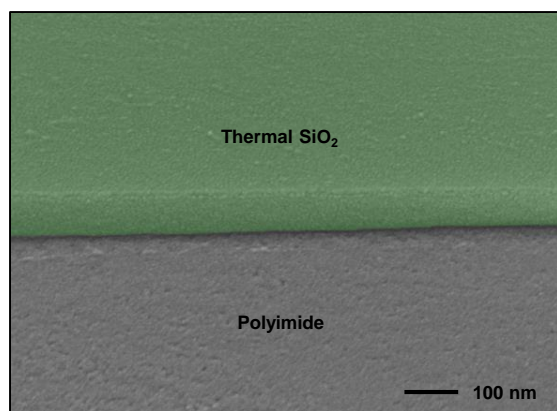


Figure S1

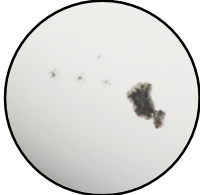


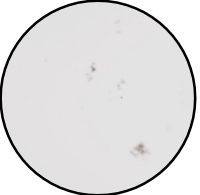


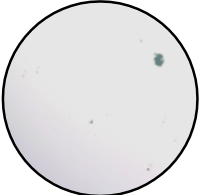
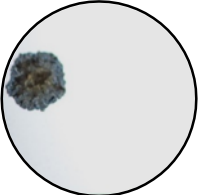

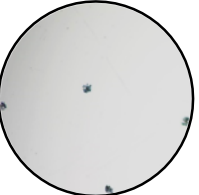
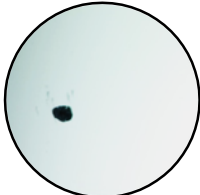



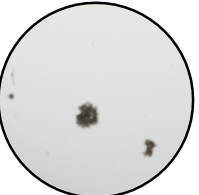


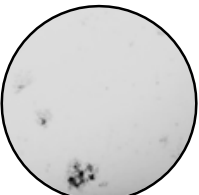
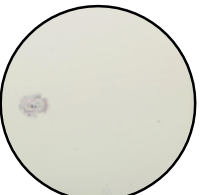

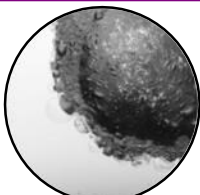
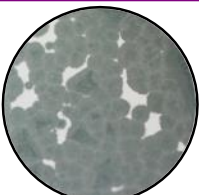
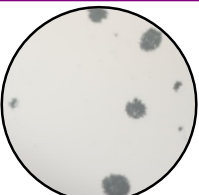
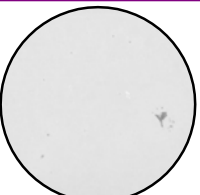

| | | | | |
|---------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| SU-8 1μm 37°C, 20min | PI2545 1μm 37°C, 20.5hr | Parylene C 1μm 37°C, 1.5hr | PDMS 1μm 37°C, 65min | LCP 25 μm 70°C, 9d |
|  |  |  |  |  |
| PECVD low-dep SiO ₂ 1μm 37°C, 15min | PECVD SiN _x 1μm 37°C, 25min | ALD Al ₂ O ₃ 100nm 37°C, 10min | ALD HfO ₂ 100nm 37°C, 80min | SiO ₂ /SiN _x ×3 16.6/16.6nm×3 37°C, 15min |
|  |  |  |  |  |
| Al ₂ O ₃ /HfO ₂ ×3 16.6/16.6nm×3 37°C, 37min | Al ₂ O ₃ /Parylene C 50/1000nm 70°C, 7.5hr | Al ₂ O ₃ /Parylene C 50/6000nm 70°C, 12hr | Al ₂ O ₃ /Parylene C×3 50/283.3nm x3 37°C, 50min | Al ₂ O ₃ /PI2545 50/950nm 37°C, 30min |
|  |  |  |  |  |
| Al ₂ O ₃ /PI2545×3 50/283.3nm×3 37°C, 13.5hr | HfO ₂ /Parylene C 50/950nm 70°C, 250hr | HfO ₂ /Parylene C x3 50/283.3nm x3 70°C, 46min | HfO ₂ /PI2545 50/950nm 37°C, 5hr | HfO ₂ /PI2545×3 50/283.3nm×3 37°C, 10hr |
|  |  |  |  |  |
| SiN _x /Al ₂ O ₃ /Parylene C 50/50/900nm 37°C, 62.5hr | Ti/Pt 5/100nm 37°C, 5min | Cr/Au 5/100nm 37°C, 5min | Cr/Au 5/1000nm 37°C, 75min | |
|  |  |  |  |  |

Table S1

| Category | # | Material | Deposition method | Thickness for Mg test | Barrier lifetime (at 37 °C) | Leakage mode |
|------------------------------|----|--------------------------------------------------------------|-------------------|-----------------------|-----------------------------|------------------|
| Organic | 1 | SU-8 | Spin coating | 1 µm | < 1 day | Bulk |
| | 2 | Polyimide (PI) | Spin coating | 1 µm | < 1 day | Bulk |
| | 3 | Parylene C | CVD | 1 µm | < 1 day | Bulk |
| | 4 | PDMS | Spin coating | 1 µm | < 1 day | Bulk |
| | 5 | LCP | -- | 25 µm | 147 – 309 day* | Bulk |
| Inorganic | 6 | SiO _x | PECVD | 1 µm | < 1 day | Bulk |
| | 7 | SiN _x | PECVD | 1 µm | < 1 day | Bulk |
| | 8 | Al ₂ O ₃ | ALD | 100 nm | < 1 day | Pinhole |
| | 9 | HfO ₂ | ALD | 100 nm | < 1 day | Pinhole |
| Inorganic Multilayer | 10 | SiO _x /SiN _x x 3 | PECVD | 16.6/16.6 nm x3 | < 1 day | Pinhole |
| | 11 | Al ₂ O ₃ /HfO ₂ x 3 | ALD | 16.6/16.6 nm x3 | < 1 day | Pinhole |
| | 12 | Al ₂ O ₃ /Parylene C | ALD/CVD | 50/950 nm | 3 - 7 day* | Pinhole |
| | 13 | Al ₂ O ₃ /Parylene C | ALD/CVD | 50/6000nm | 5 – 11 day | Pinhole |
| Inorganic/organic Multilayer | 14 | Al ₂ O ₃ /Parylene C x3 | ALD/CVD | 50/283.3 nm x3 | < 1 day | Pinhole |
| | 15 | Al ₂ O ₃ /PI | ALD/Spin coating | 50/950 nm | < 1 day | Pinhole |
| | 16 | Al ₂ O ₃ /PI x3 | ALD/Spin coating | 50/283.3 nm x3 | < 1 day | Pinhole |
| | 17 | HfO ₂ /Parylene C | ALD/CVD | 50/950 nm | 102 - 214 day* | Pinhole |
| | 18 | HfO ₂ /Parylene C x3 | ALD/CVD | 50/283.3 nm x3 | 22 - 39 day | Pinhole |
| | 19 | HfO ₂ /PI | ALD/Spin coating | 50/950 nm | < 1 day | Pinhole |
| | 20 | HfO ₂ /PI x3 | ALD/Spin coating | 50/283.3 nm x3 | < 1 day | Pinhole |
| | 21 | SiN _x /Al ₂ O ₃ /Parylene C | PECVD/ALD /CVD | 50/50/900 nm | 2 - 3 day | Pinhole |
| Thermal Oxide | 22 | SiO ₂ | Thermally grown | 100 nm | 6-7 years** | Slow dissolution |

Permeability measured at 37°C, 90% Relative Humidity

* Indicates data from accelerated soak test. Reaction Rate Factor Q10 = 2 - 2.5.

** Barrier lifetime defined as the soaking time period before any defect area on Mg pad reach 30mm².

Table S2

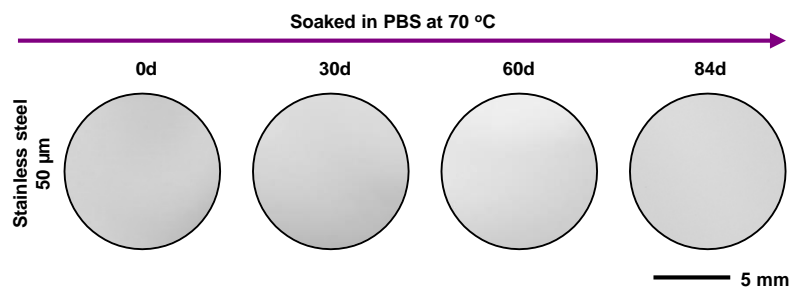
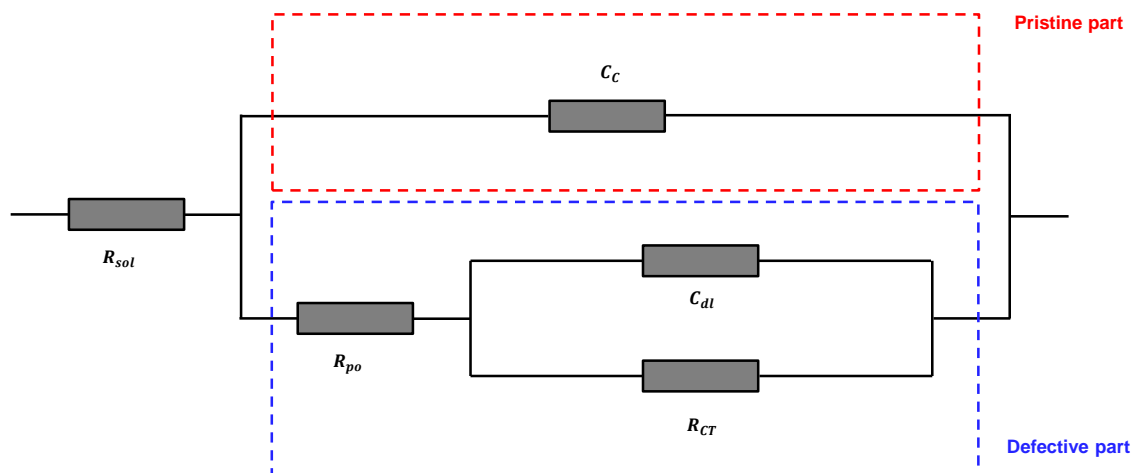


Figure S2

A



B

| Circuit element | Physical Meaning | Expression of impedance | Evaporated SiO_x | PECVD SiO_2 | Thermal SiO_2 |
|------------------------|----------------------------|----------------------------|---------------------------|----------------------|------------------------|
| R_{sol} / Ω | Solution resistance | R_{sol} | 600 | 200 | 180 |
| R_{po} / Ω | Pore resistance | R_{po} | 600 | 2000 | N/A |
| R_{CT} / Ω | Charge transfer resistance | R_{CT} | 1800 | 48000 | N/A |
| $C_{dl} / \mu\text{F}$ | Double layer capacitance | $\frac{1}{j\omega C_{dl}}$ | 1.9 | 0.018 | N/A |
| C_c / nF | Coating capacitance | $\frac{1}{j\omega C_c}$ | 0.3 | 0.86 | 1.17 |

Figure S3

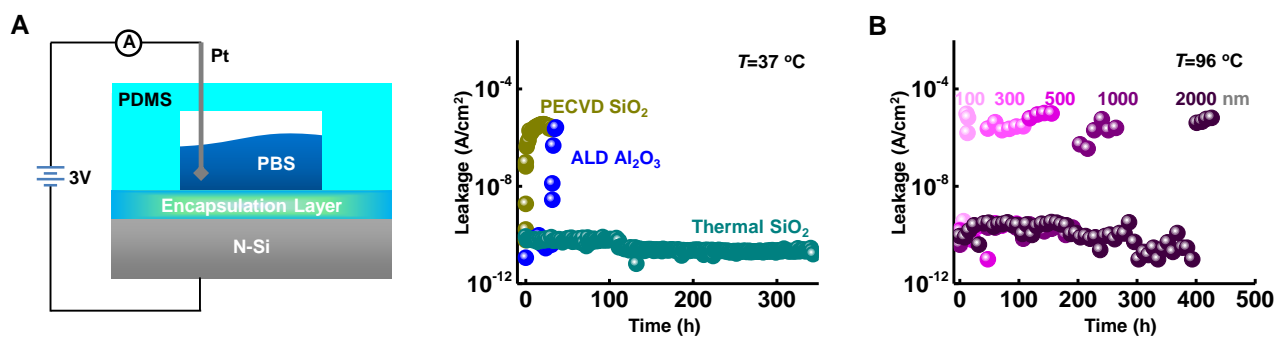


Figure S4

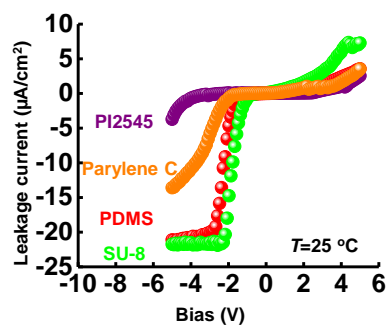


Figure S5

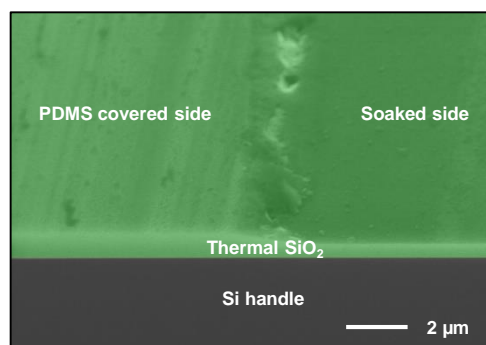


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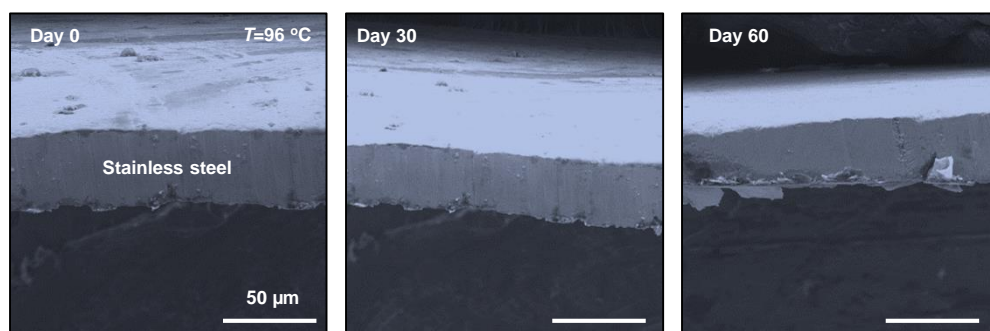


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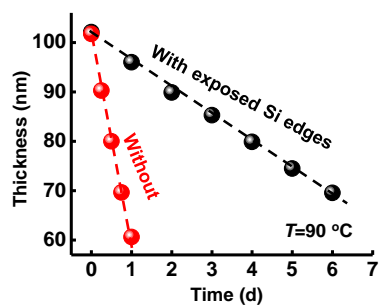


Figure S8

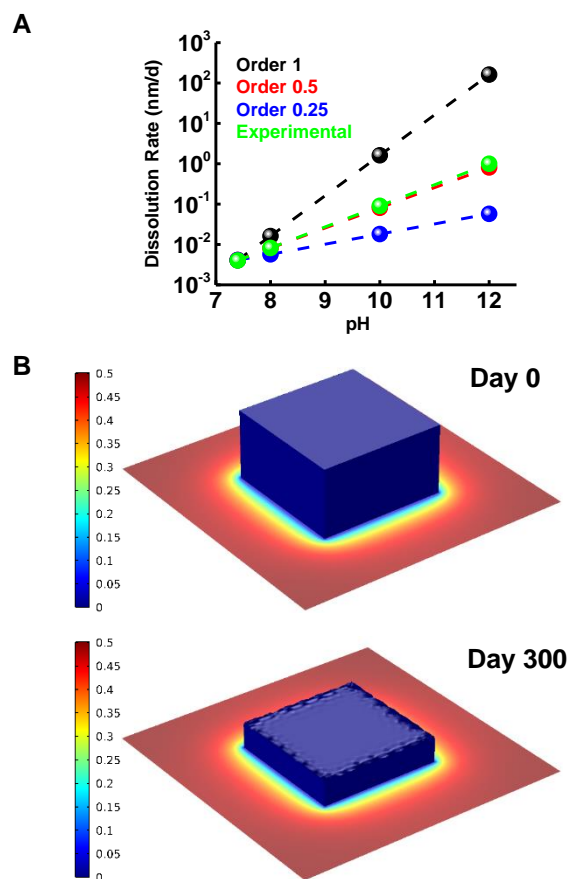


Figure S9

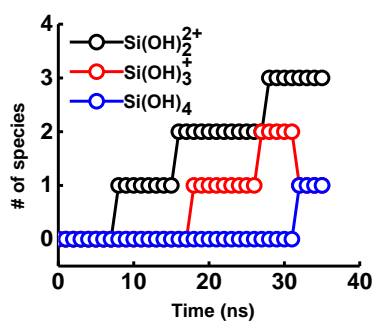


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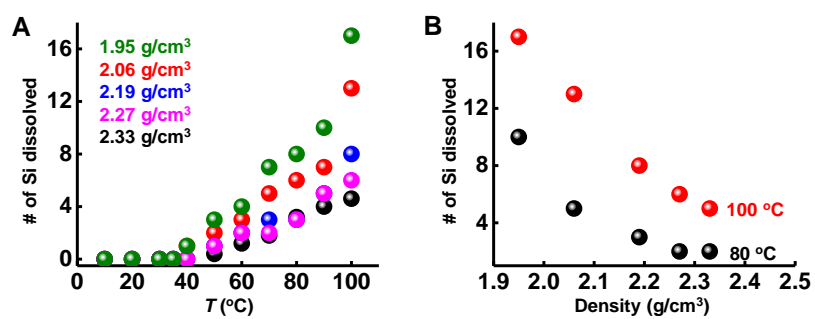


Figure S11

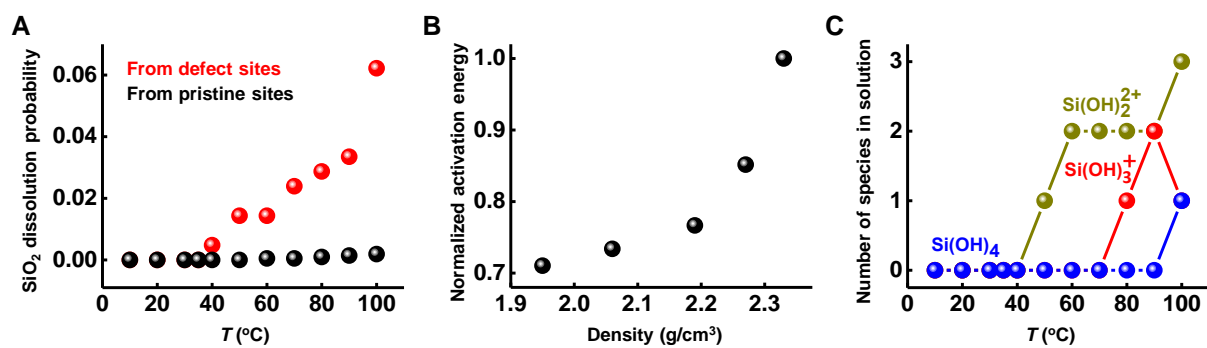


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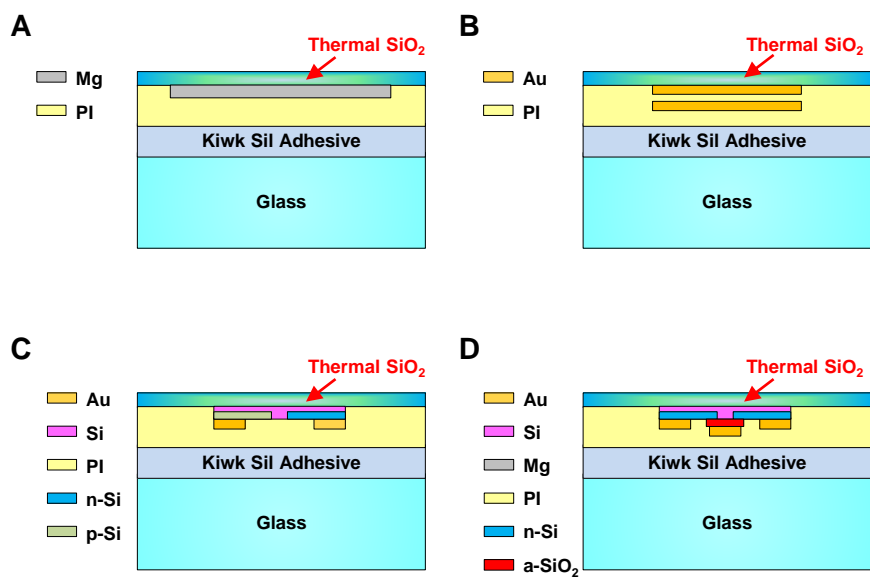


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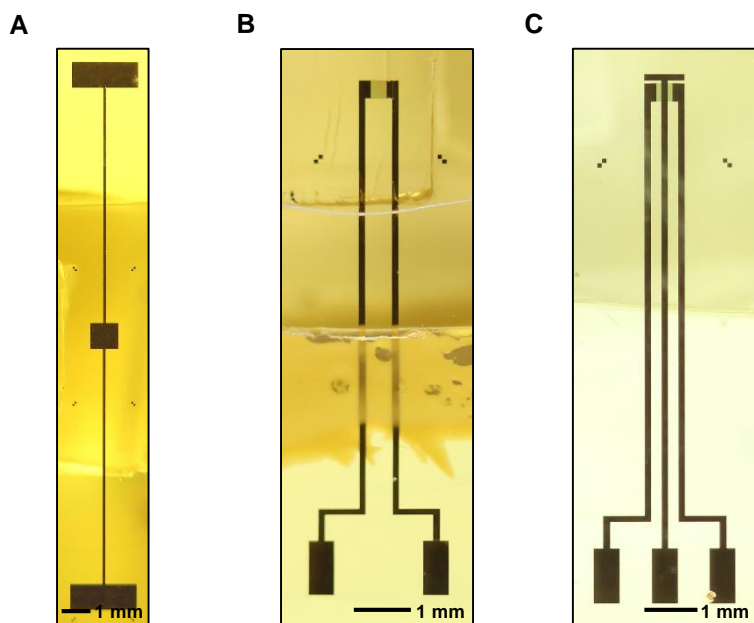


Figure S14

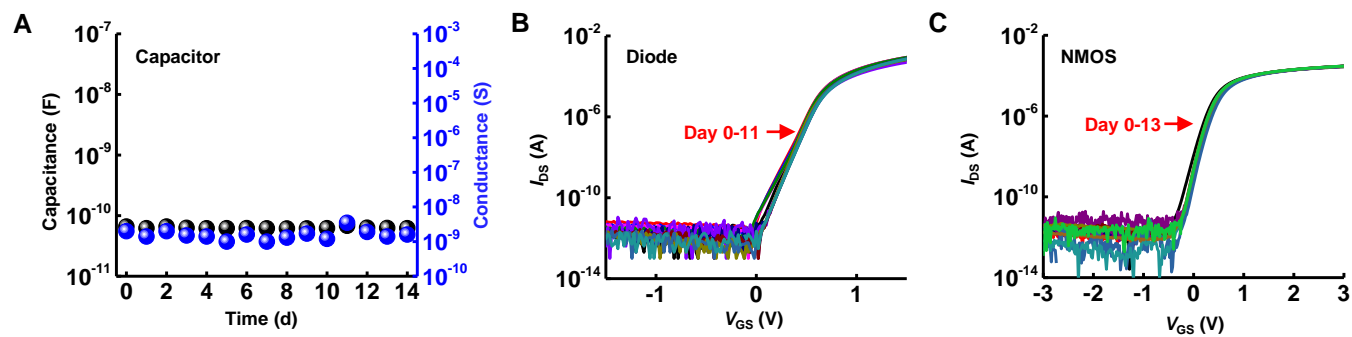
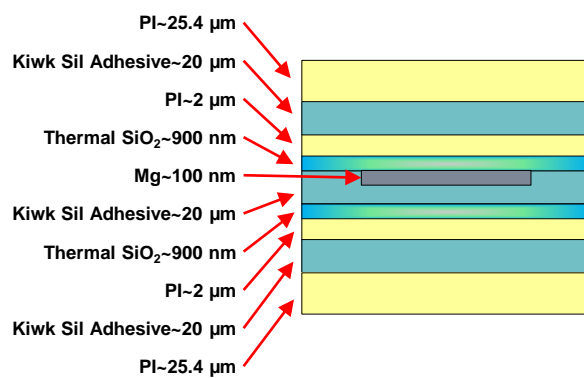


Figure S15

A



B

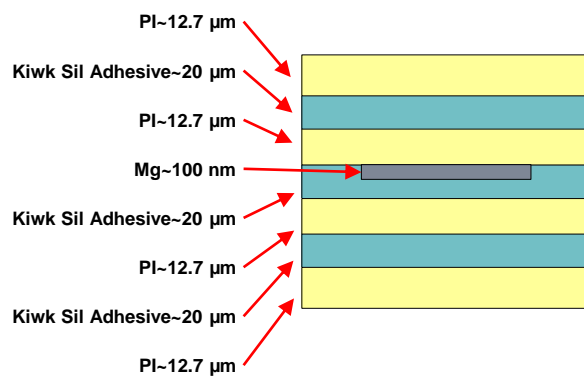


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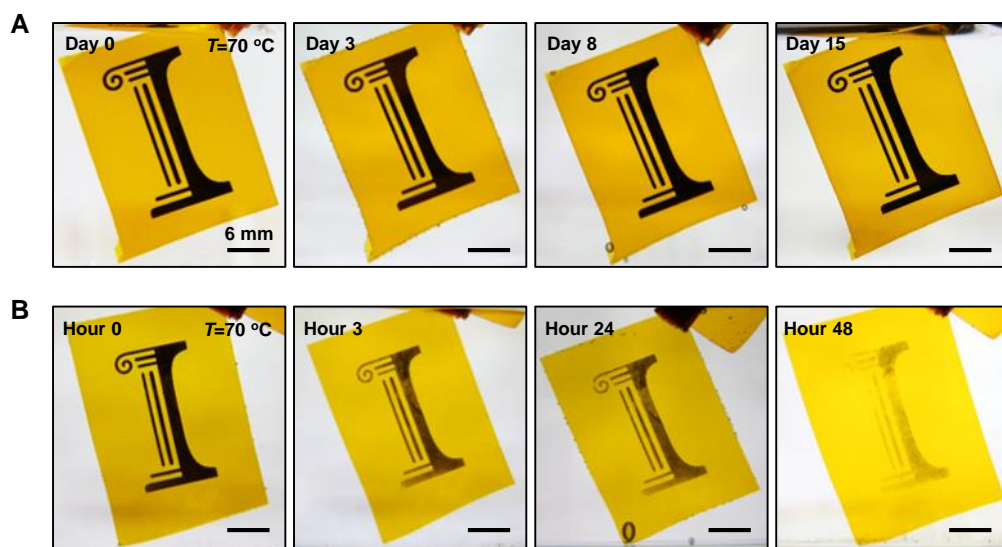


Figure S17



Figure S18

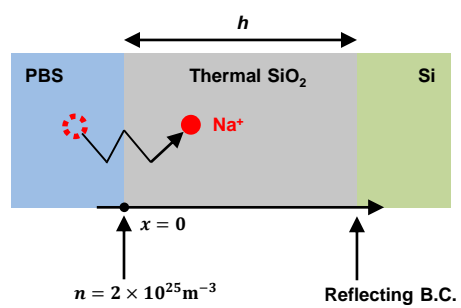


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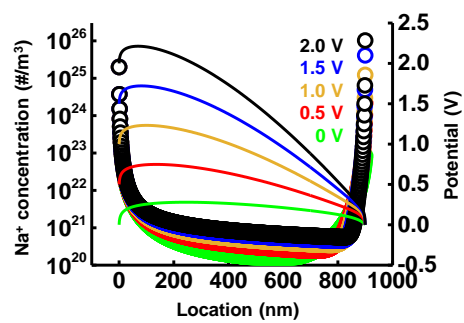


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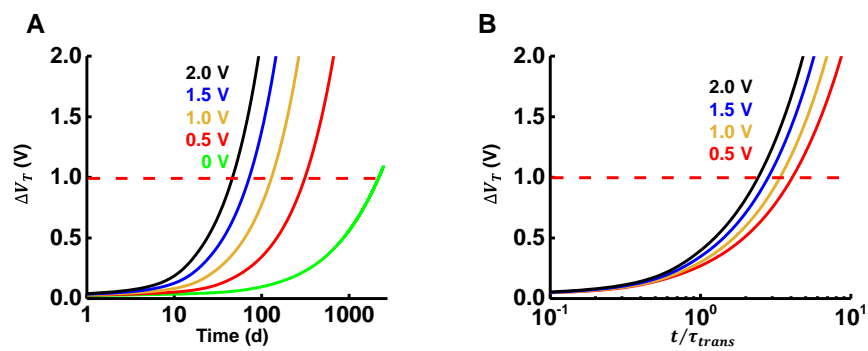


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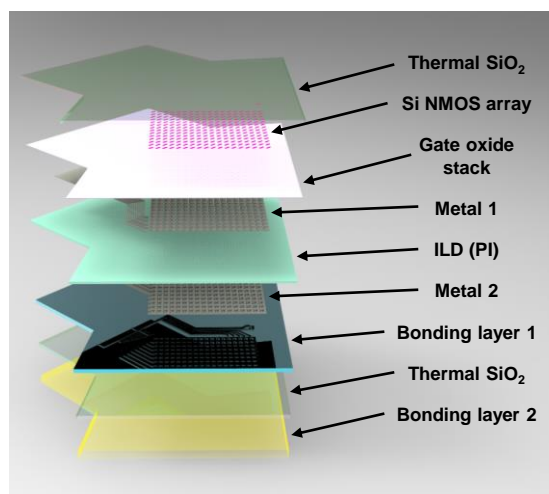


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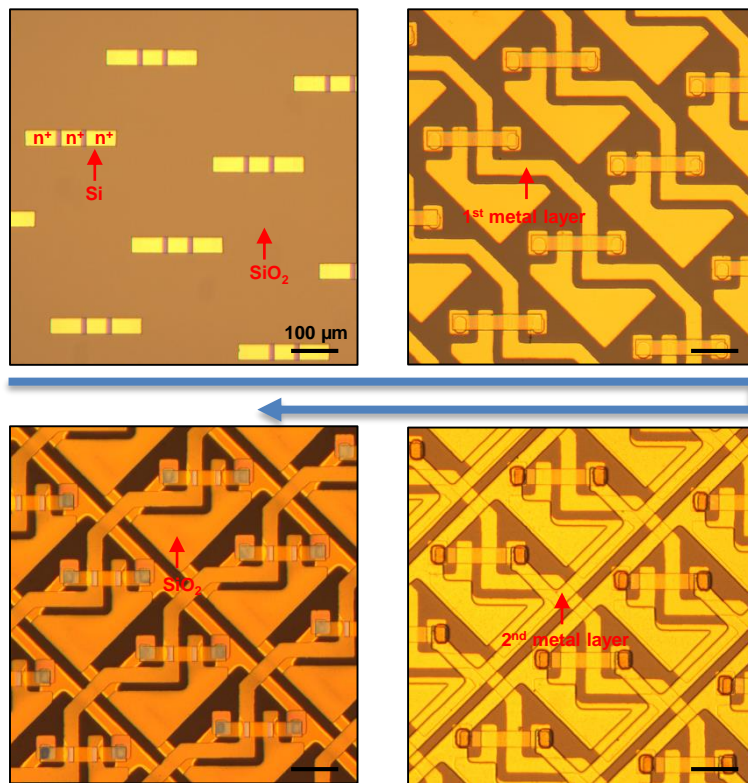
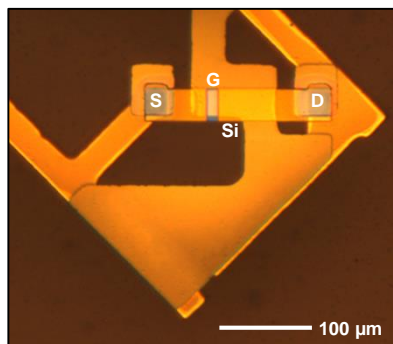
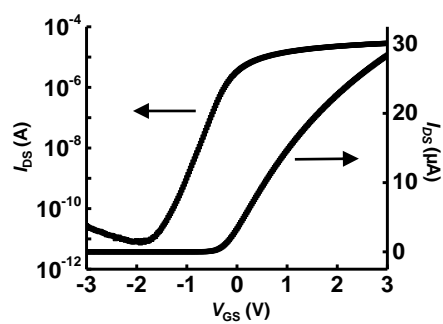
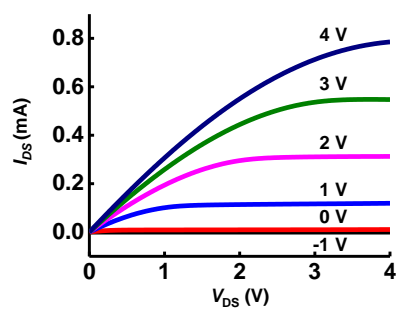


Figure S23

A**B****C****Figure S24**

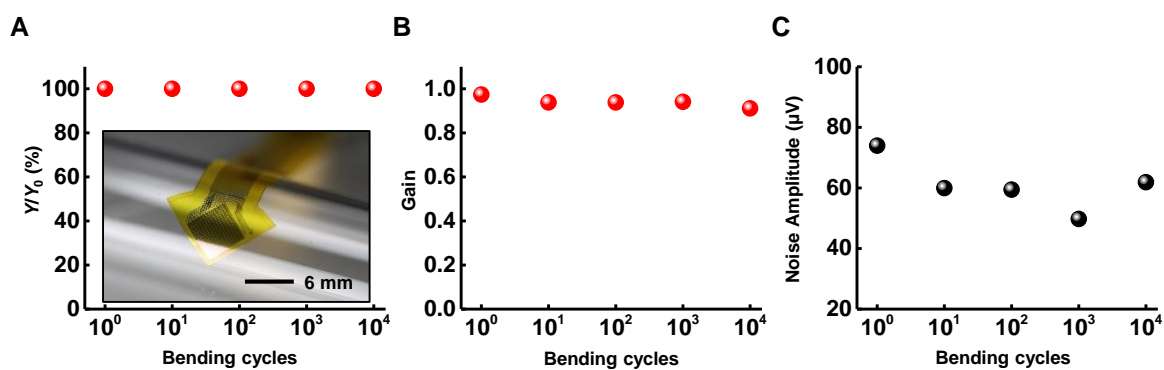


Figure S25