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Using nanoscale thermocapillary flows to create arrays of purely semiconducting single-walled carbon nanotubes

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Among the remarkable variety of semiconducting nanomaterials that have been discovered over the past two decades, single-walled carbon nanotubes remain uniquely well suited for applications in high-performance electronics, sensors and other technologies. The most advanced opportunities demand the ability to form perfectly aligned, horizontal arrays of purely semiconducting, chemically pristine carbon nanotubes. Here, we present strategies that offer this capability. Nanoscale thermocapillary flows in thin-film organic coatings followed by reactive ion etching serve as highly efficient means for selectively removing metallic carbon nanotubes from electronically heterogeneous aligned arrays grown on quartz substrates. The low temperatures and unusual physics associated with this process enable robust, scalable operation, with clear potential for practical use. We carry out detailed experimental and theoretical studies to reveal all of the essential attributes of the underlying thermophysical phenomena. We demonstrate use of the purified arrays in transistors that achieve mobilities exceeding 1,000 $cm^2 V^{-1} s^{-1}$ and on/off switching ratios of ~10,000 with current outputs in the milliamp range. Simple logic gates built using such devices represent the first steps toward integration into more complex circuits.

Exploiting the exceptional electrical properties[1,2] of arrays of single-walled carbon nanotubes (SWNTs) in advanced applications[3–9] demands an ability to meet challenging requirements on degrees of alignment and purity in semiconducting behaviour. Direct, selective growth of purely semiconducting SWNTs (s-SWNTs) remains a topic of continuing study. Synthetic strategies that offer the greatest near-term potential fall into two categories: (i) purifying the SWNTs and then assembling them into arrays and (ii) assembling the SWNTs into arrays and then purifying them. The first has the advantage that it can build on recently developed wet chemical methods (ultracentrifugation[10,11], chromatography[12–14] and others[15,16]) for purification. The disadvantages are that the resulting SWNTs are typically short (~1 μm), chemically modified and/or coated, and difficult to assemble into arrays with high degrees of alignment[15,17–19]. The second approach overcomes these limitations through the use of chemical vapour deposition techniques that, when used with quartz substrates, can yield nearly perfectly linear (>99.9% of SWNTs within 0.01° of perfect alignment), aligned arrays of long (100 μm and up to a few millimetres) and chemically pristine SWNTs[3,20–23]. The main difficulty is in removing the metallic SWNTs (m-SWNTs) from such arrays. Techniques based on optical[24], electrical[25] or chemical[26–28] effects involve some combination of drawbacks, including incomplete removal of the m-SWNTs, partial removal and/or degradation of the s-SWNTs, inability to operate on aligned arrays, and/or reliance on uncertain underlying mechanisms. Among these methods, electrical breakdown is noteworthy because it operates directly on the basis of relevant distinguishing characteristics in charge transport[25]. This scheme, however, has two critical disadvantages. First, the required high-power operation (~90 μW $μm^{-1}$ for channel lengths >1 μm, increasing as channel length decreases to values >1 mW $μm^{-1}$)[29–31] leads to shifts in threshold voltage, avalanche effects[32], band-to-band tunnelling, failure in gate dielectrics, and significant heatsinking at the contacts[29], all of which can prevent proper operation of the process. More significantly, breakdown only removes the m-SWNTs in isolated, narrow regions (~100 nm lengths) at locations that are not well controlled[33]. As a result, the vast majority of the m-SWNTs remain in the arrays[34], thereby preventing generalized use in subsequently fabricated devices.

Purification based on thermocapillary flow and etching

We introduce an approach for eliminating m-SWNTs in which thermocapillary effects in thin organic coatings allow their use as selective, self-aligned etch resists. Here, physical mass transport occurs via surface tension gradients generated through spatial variations in temperature[35] associated with selective heating in the m-SWNTs. We illustrate these concepts through the complete physical removal of all m-SWNTs from linear, horizontally aligned arrays

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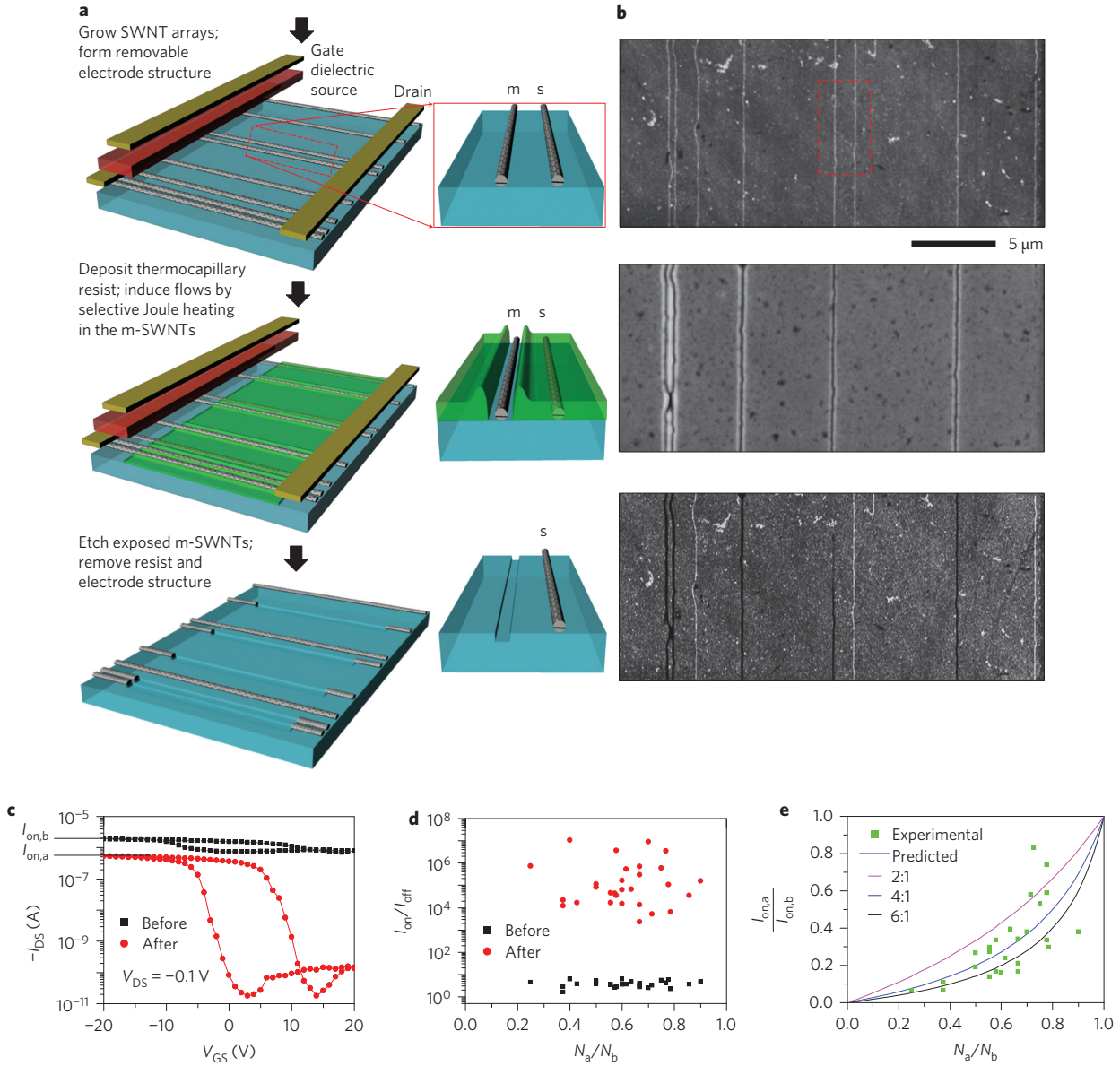

Figure 1 | Process for exploiting thermocapillary effects in the purification of arrays of SWNTs. a,b, Schematic illustration (**a**) and corresponding AFM images (**b**) of various stages of the process applied to an array of five m-SWNTs and three s-SWNTs. Uniform thermal evaporation forms a thin, amorphous organic coating that functions as a thermocapillary resist. A series of processing steps defines a collection of electrodes and dielectric layers for selective injection of current into the m-SWNTs. The Joule heating that results from this process induces thermal gradients that drive flow of thermocapillary resist away from the m-SWNT, to form open trenches with widths, measured near the substrate, of ~100 nm. Reactive ion etching physically eliminates the m-SWNT exposed in this fashion, while leaving the coated s-SWNTs unaltered. Removing the thermocapillary resist and electrode structures completes the process, to yield arrays comprising only s-SWNTs. **c**, Typical transfer characteristics for a transistor built with an array of SWNTs in a partial gate geometry, evaluated before and after purification. Quantities $I_{on,b}$ and $I_{on,a}$ correspond to currents measured in the on states before and after purification, respectively. Here, the on/off ratio improves by a factor of 2×10^4, while $I_{on,a}/I_{on,b}$ remains relatively large (~0.25). **d**, Ratios between currents in the on and off states before and after purification ($I_{on,b}$ and $I_{off,a}$, respectively) as a function of the ratio of the number of SWNTs after purification (N_a) to the number of SWNTs before purification (N_b). All devices show on/off ratios $>2 \times 10^3$, with most $>1 \times 10^4$. This result is consistent with complete removal of all m-SWNTs. **e**, Ratio of $I_{on,a}$ to $I_{on,b}$ as a function of N_a/N_b for the entire set of devices with $N_b > 7$. The results are consistent with modelling (lines) that assumes complete retention of s-SWNTs through the purification process, expected relative populations of s-SWNTs and m-SWNTs in the arrays, and ratios of conductivities of m-SWNTs and s-SWNTs (in their on state) that lie in an experimentally expected range.

that contain both m-SWNTs and s-SWNTs, without any measurable adverse effects on the latter. Figure 1a,b presents schematic illustrations and corresponding atomic force microscope (AFM) images of the process applied to a heterogeneous collection of SWNTs grown on quartz. Arrays formed in this fashion consist of individual, isolated SWNTs, with very few multiwalled nanotubes or bundles of SWNTs, but with a distribution of diameters between ~0.6 nm and ~2.0 nm and a range of chiralities[23,31]. The key element in the purification process is an ultrathin (~25 nm) amorphous layer of a small-molecule organic species, in this example α,α,α′-tris(4-hydroxyphenyl)-1-ethyl-4-isopropylbenzene[36], deposited uniformly over the arrays of SWNTs by thermal evaporation. We refer to this film (Supplementary Fig. S2) as a thermocapillary resist. As well as having favourable thermophysical properties, this particular material is well suited for the present purposes because it combines hydroxyl and phenyl moieties to

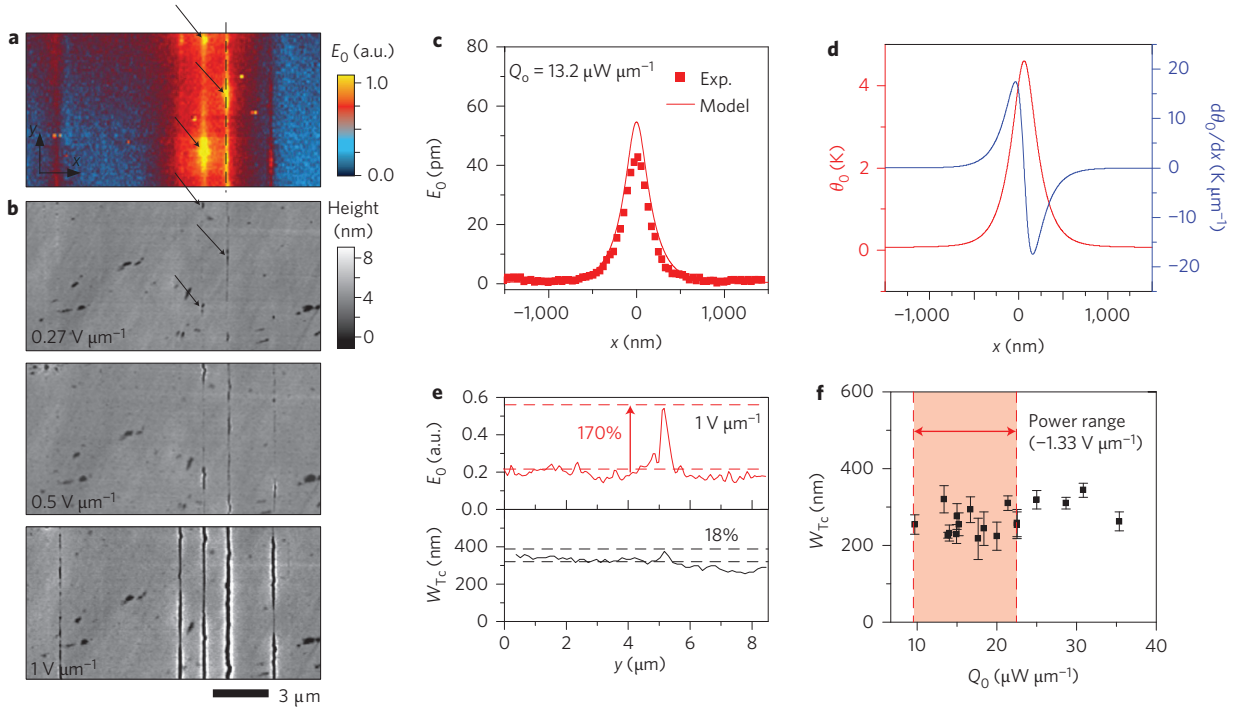

Figure 2 | Thermal origins and power scaling in behaviour of the thermocapillary resists. a, Scanning Joule expansion microscope image of an array of SWNTs in an operating, two-terminal device on quartz. The electrodes (separation of ~30 μm) are above and below the image, out of the field of view. Coordinates *x* and *y* lie perpendicular and parallel to the direction of alignment of the SWNTs, respectively. **b**, Topographical images of the device in **a**, coated with a thin (~25 nm) layer of thermocapillary resist, collected after operation at bias conditions of 0.27 V μm^{-1} (top), 0.5 V μm^{-1} (middle) and 1.0 V μm^{-1} (bottom). Comparison of these images with those collected by scanning Joule expansion microscopy reveals a clear correlation between a.c. expansion (E_0, and therefore temperature) and the formation of trenches in the thermocapillary resist (d.c. heating). **c**, Thermal expansion E_0 (a.c.) induced by Joule heating in an individual SWNT with input power density $Q_0 \approx 13$ μW μm^{-1} (peak to peak), measured by scanning Joule expansion microscopy (symbols) as a function of position *x*, where $x = 0$ is the location of the SWNT on a SiO_2/Si substrate. Results of thermomechanical modelling are shown as a line. **d**, Computed a.c. temperature rise θ_0 and thermal gradients $d\theta_0/dx$ at the surface of the thermocapillary resist using experimentally validated models, for the case of the SWNT in **c**. The results indicate small increases in temperature for levels of Joule heating that induce trenches in the thermocapillary resist (~3–10 μW μm^{-1}). **e**, Top graph: a.c. thermal expansion (arbitrary units) measured by scanning Joule expansion microscope along the length *y* of the fourth SWNT from the left in the array that appears in **a** and **b**. Bottom graph: width of the corresponding trench that appears in the thermocapillary resist (W_{Tc} measured at the top of the film) for an applied bias of ~1 V μm^{-1}. The results show variations in W_{Tc} that are nearly ten times smaller than those in expansion (and therefore temperature). **f**, Measurements of the average W_{Tc} as a function of Q_0. The results reveal no systematic dependence on Q_0 over this range. The highlighted region corresponds to the values of Q_0 associated with optimized conditions for the purification process. Error bars indicate the standard deviation of the range of measured widths.

facilitate the formation of uniform, continuous coatings on the surfaces of both the quartz and the SWNTs. This behaviour is critical for its role as an effective etch resist with extremely small thicknesses.

Metal and dielectric layers patterned at the edges of an area of interest enable current injection primarily into only the m-SWNTs, due to controlled electrostatically induced increases in the heights and widths of the Schottky barriers at the source ends of the s-SWNTs (Fig. 1a; Supplementary Figs S4, S25–S27). These layers represent removable, transistor structures in which the gates extend beyond the source electrodes by a distance that is small (~5 μm) compared to the separation between the source and drain (~30 μm). Applying a positive voltage to the gate (~20 V) and a negative voltage to the drain (−40 V to −50 V), while holding the source at electrical ground, leads to selective Joule heating only in the m-SWNTs as a result of approximately unipolar p-type behaviour in the s-SWNTs. (Supplementary Figs S21 and S22 illustrate the good stability in the current outputs.) This set of bias conditions produces small increases in temperature only in the vicinity of the m-SWNTs. The large thermal gradients associated with nanoscale localization of these heat sources in turn drive mass transport in the thermocapillary resist. In typical experiments (fields of $V_{DS}/L_{ch} \approx 1.33$–$1.66$ V μm^{-1} along the SWNTs for 5 min, with substrate heating to 60 °C in vacuum, where V_{DS} is the drain–source bias and L_{ch} is the distance between the electrodes), the resulting flows yield trenches centred at the m-SWNTs and extending throughout the thickness of the thermocapillary resist (Fig. 1b). Although most experiments were performed in vacuum (1×10^{-4} torr), inert environments can also be used (for example, dry nitrogen or argon). Excluding oxygen can help to prevent electrical breakdown in extreme cases of hot spots along the lengths of the SWNTs with localized defects. Reactive ion etching (RIE, O_2/CF_4) after thermocapillary flow eliminates only the m-SWNTs. Removing the residual thermocapillary resist and the metal/dielectric structures leaves a purified array of s-SWNTs, in a configuration well suited for planar integration into diverse classes of devices and sensors.

Efficiency of the purification process

A key feature of this process is its exceptional efficiency in removing the m-SWNTs completely and exclusively. Such operation is important because most envisioned applications of s-SWNTs in electronics require purity at the level of 99.99% or better. For present purposes, we define a SWNT as metallic if the ratio between the on (I_{on}) and off (I_{off}) currents (that is, the on/off ratio) in a well-designed transistor structure that incorporates this SWNT is less

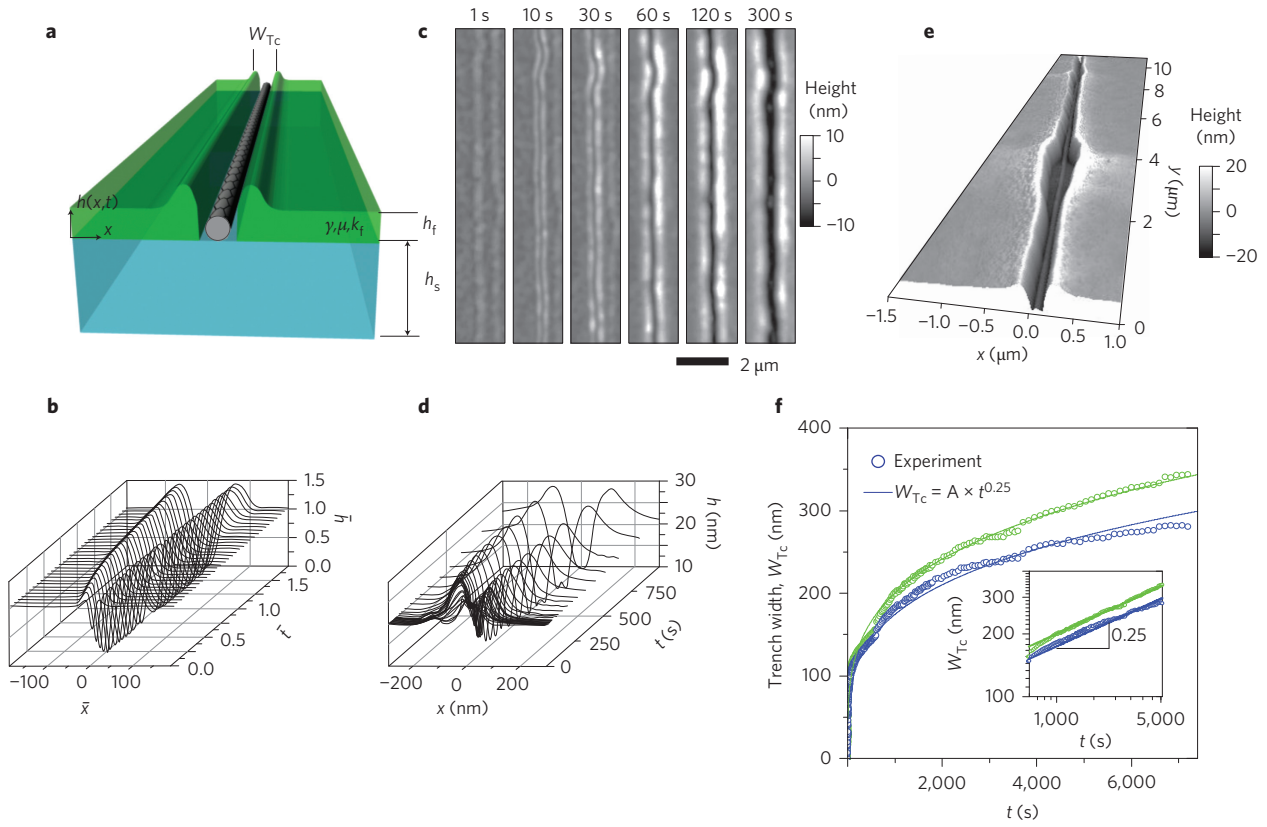

Figure 3 | Nanoscale thermocapillary flows in thermocapillary resists induced by Joule heating in SWNTs. a, Schematic illustration of the geometry of the system, with key parameters defined. The SWNT, thermocapillary resist and substrate are grey, green and blue, respectively. **b**, Theoretically calculated normalized surface profiles of the thermocapillary resist, $\bar{h}$, as a function of normalized distance $\bar{x}$ and time $\bar{t}$, showing the evolution of the trench geometry with thermocapillary flow. The simulations used polystyrene because relevant materials parameters were available in the literature. **c**, AFM images of a SWNT coated with thermocapillary resist (~25 nm) after Joule heating (0.66 V μm^{-1}) for 1, 10, 30, 60, 120 and 300 s, induced by current injection at electrodes that lie outside of the field of view. Thermocapillary flow creates a trench that aligns to the SWNT and grows in width over time. **d**, Averaged cross-sectional profiles extracted from measurements like those shown in **c**. The results compare favourably to the modelling in **b**. **e**, AFM image, rendered in a three-dimensional perspective view collected at a duration of 1,800 s. The width in this case is sufficiently large that AFM measurements clearly reveal that thermocapillary flow completely and cleanly exposes the SWNT. **f**, Widths of trenches measured by AFM from the ridges that form at the top surface (W_{Tc}), shown as a function of time of Joule heating for two different SWNTs, with a field of 0.66 V μm^{-1}. Both model and experiment show a power-law time dependence with an exponent of 0.25.

than ~100, and define it as semiconducting if this ratio is greater than ~100. This definition places SWNTs that are sometimes referred to as quasi-metallic into the m-SWNT classification. (In all cases, for populations of SWNTs grown on quartz, we observe a clear distinction between the behaviour of m-SWNTs and s-SWNTs defined in this way; in particular, of the hundreds of SWNTs studied here and elsewhere, none exhibit on/off ratios between ~50 and ~1,000.[37]) Detailed electrical characterization (that is, I_{on} and I_{off} before and after purification) and assessment of statistics (that is, total numbers of SWNTs before and after) performed on significant numbers of devices (35 devices, each with an active area of ~30 × 30 μm^2 to enable full visualization by AFM; 377 SWNTs in total) provide quantitative insights into the effectiveness of the process. Figure 1c shows a representative transfer characteristic for a device before and after purification, measured in air using the same metal/dielectric structures that enable selective Joule heating. The results illustrate a dramatic reduction in I_{off} (from 0.7 μA to 2 × 10^{-5} μA), thereby improving the on/off ratio from 2.7 to a value of 3 × 10^4. All devices demonstrated on/off ratios of less than 10 (median = 3.7) before and greater than 2 × 10^3 (median = 6.6 × 10^4) after purification, independent of the number of SWNTs removed (Fig. 1d). The relatively small numbers (<30) of SWNTs in each device used to examine the statistics led to the conclusion that the observed on/off ratios correspond to complete removal (that is, 100%) of the m-SWNTs.

Other results suggest that the process also preserves most or all of the s-SWNTs. First, of the 377 SWNTs present initially, 63% (that is, 238 SWNTs) remain after purification. This outcome is consistent with the expected percentage (~66%) of s-SWNTs in collections of SWNTs grown by chemical vapour deposition[3,38]. Second, among the 28 devices where SWNT type could be determined from electrical behaviours measured before and after purification (that is, those that incorporate ≤2 SWNTs), all the m-SWNTs and none of the s-SWNTs show trenches (for optimized conditions; see Supplementary Fig. S1). Third, reductions in I_{on} induced by purification are modest; for the device shown in Fig. 1c the ratio of I_{on} after the process to its value before is $I_{on,a}/I_{on,b} \approx 25\%$. The weighted average from all of the devices is $I_{on,a}/I_{on,b} \approx 30\%$. These results can be interpreted by examining the dependence of $I_{on,a}/I_{on,b}$ on the percentage of SWNTs removed (Fig. 1e). The trends are consistent with models that assume 100% preservation of s-SWNTs, expected populations of s-SWNTs and m-SWNTs, and ratios of conductances of m-SWNTs to s-SWNTs (in their on state) that are within an experimentally observed range of 6:1 and 2:1 (Supplementary Fig. S3). Collectively, then, all observations suggest highly selective and efficient purification, in which all m-SWNTs are eliminated, and most

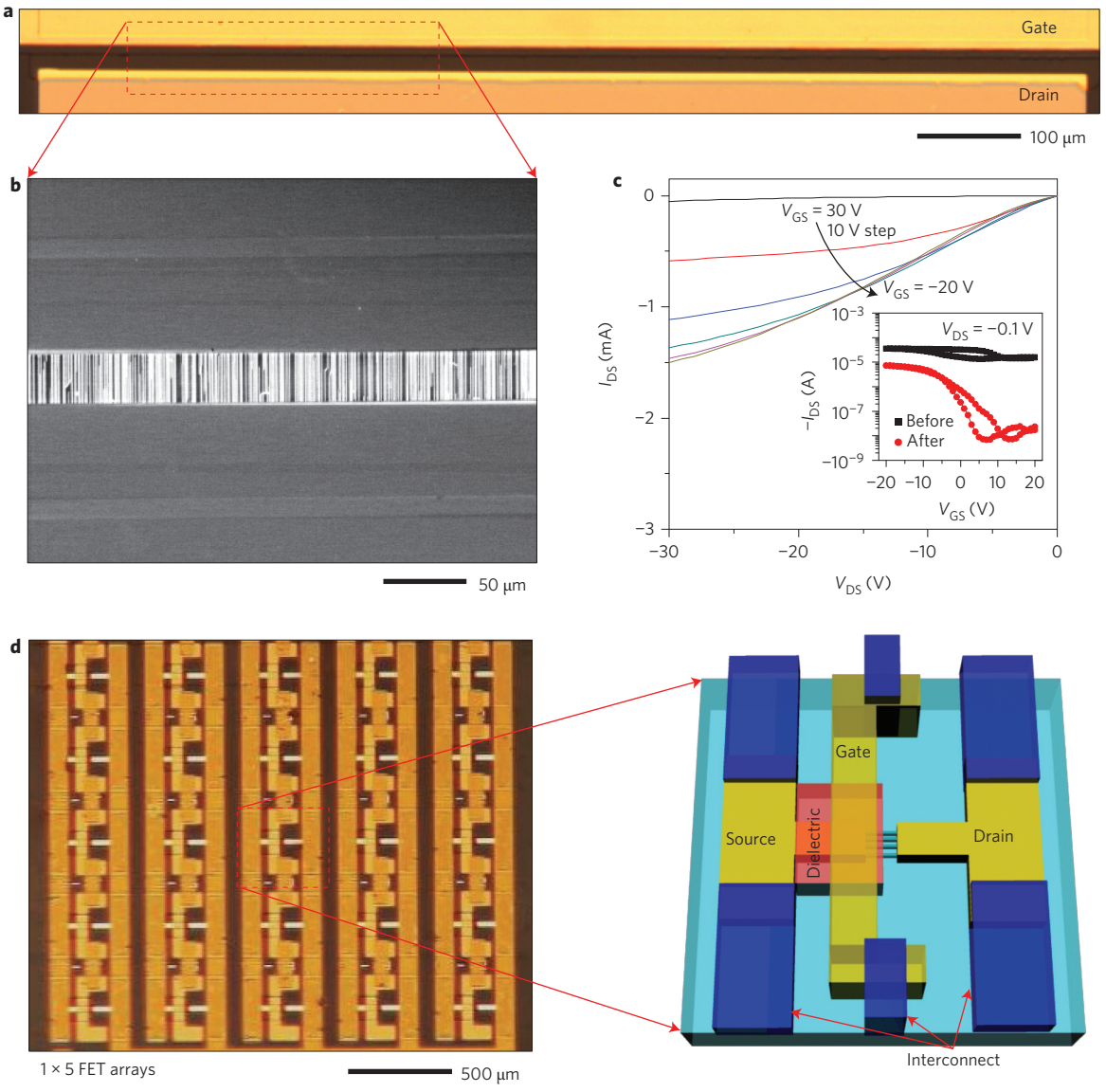

Figure 4 | Description of two alternative approaches to scale thermocapillary separation for large-area applications. a, Optical microscope image of a set of electrodes for thermocapillary purification of an array of many hundreds of SWNTs. **b**, Scanning electron microscope image of a small region of the structure shown in **a**. **c**, Transfer characteristics before and after removal of m-SWNTs from the region between the electrodes shown in **a**. The results indicate outcomes consistent with observations from small-scale demonstrations, that is, high on/off ratios of $\sim 1 \times 10^3$ and modest reductions in on current ($I_{on,a}/I_{on,b} \approx 20\%$). **d**, Optical micrograph and schematic illustration of an alternative mode for scaled implementation. An interconnected array of 25 sets of electrodes allows purification over a collection of small regions, in a parallel fashion. Associated transfer curves are similar to those shown in **c**.

or all s-SWNTs are preserved without degradation. Rigorous electrostatic analysis indicates mobilities of $\sim$1,000 cm^2 V^{-1} s^{-1} for the s-SWNTs (see Supplementary Fig. S18 for details), similar to values previously reported from unpurified arrays[3,4].

Studies of nanoscale thermocapillary flow

Detailed experimental and theoretical studies reveal quantitative aspects of heat transport and thermocapillary flow. We start by examining the distributions of temperature generated during Joule heating and their role in the behaviour of the thermocapillary resist. Figure 2a presents a scanning Joule expansion microscope[39,40] image of the thermal expansion that results from Joule heating in an array of SWNTs, at a drain–source bias condition of $V(t) = V_{DS}\cos(2\pi ft)$, with $V_{DS} = 5$ V and $f = 386$ kHz. Here, Joule heating with a power density of $Q(t) = Q_0[1 + \cos(4\pi ft)]/2$ yields a.c. thermal expansion at a frequency of $2f$, according to $E(t) = [E_1 + E_0\cos(4\pi ft)]/2$. Components E_1 and E_0 correspond to d.c. and a.c. thermal expansion, respectively. The image signal corresponds to the peak-to-peak value of the a.c. expansion, E_0. Figure 2b shows topographical images of the same array coated with thermocapillary resist after application of several increasing values of V_{DS} (direct current for 5 min; substrate temperature 60 °C). A key observation is that the distributions in expansion, and therefore temperature (Fig. 2a), correspond directly to the geometries of trenches that appear in the thermocapillary resist (Fig. 2b). For instance, trenches progressively form with increasing V_{DS} in an order consistent with the temperatures revealed by the scanning Joule expansion microscopy; trenches at the second and fifth SWNT from the right appear first and last, respectively. Related effects can be observed along an individual SWNT, where trenches nucleate in areas of enhanced temperature ('hot spots'; arrows in Fig. 2a and the top frame of Fig. 2b). These indications establish a clear, although qualitative, connection between temperature and operation of the thermocapillary resist.

The first step towards quantitative understanding is an experimentally validated model for nanoscale heat flow in this system. Raw data from measurements by scanning Joule expansion microscopy indicate relative temperature increases but not their absolute values. Figure 2c shows a representative cross-sectional profile of E_0 for the case of a SWNT of length ~3.5 μm (the corresponding scanning Joule expansion microscopy image is shown in Supplementary Fig. S5). The power density per unit length is $Q(t)$, with Q_0 estimated to be ~13 μW μm^{-1} based on the total input power into the device, which includes three SWNTs on an SiO_2/Si substrate. Analytical models of temperature distributions that treat the SWNT as a line heat source with length L and input power density $Q(t)$ can be developed (Supplementary Fig. S6). Boundary conditions involve continuous temperature and heat flow at all material interfaces except those with the SWNT, negligible heat flow at the top surface, and a constant temperature at the base of the substrate. At the SWNT interface, discontinuous heat flow $Q(t)$ is assumed as a means to introduce the source of Joule heating. The results, together with materials constants taken from the literature (Supplementary Table S1) and analytical treatments of the resulting thermal expansion, yield expansion profiles that have both peak magnitudes ($E_0 \approx 50$ pm) and spatial distributions (characteristic widths ~340 nm) consistent with the scanning Joule expansion microscopy results (~40 pm and ~320 nm, respectively) when $Q_0 \approx 13$ μW μm^{-1}, the estimated experimental value. Figure 2d shows the associated a.c. temperature increases θ_0 and thermal gradients $d\theta_0/dx$, where $\theta(t) = [\theta_1 + \theta_0 \cos(4\pi ft)]/2$. When applied to the case of d.c. heating ($f = 0$ Hz), and quartz substrates, the same analytical model yields an expression for the rise in temperature of the surface of the thermocapillary resist, $\theta = T - T_\infty$, where T_∞ defines the temperature of the background,

$$\theta(x,y) = \frac{1}{2k_s\pi}\int_{-L/2}^{L/2} d\eta \int_0^\infty \frac{Q_0 J_0\left(\xi\sqrt{(\eta - y)^2 + x^2}\right)}{\cosh(\xi h_f) + \frac{k_f}{k_s}\sinh(\xi h_f)} d\xi \quad (1)$$

Here, k_s and k_f are the thermal conductivities of the thermocapillary resist and quartz substrate, respectively, and h_f is the thickness of the resist. This solution, which is also consistent with three-dimensional finite-element analysis (ABAQUS), suggests small increases in temperature at the SWNTs (~2–5 °C) for the power densities needed to achieve trenches. The flows arise from large associated gradients in temperature (~20 °C μm^{-1}) (Supplementary Fig. S6). Studies of flow induced with heated tips in an AFM verify the low-temperature operation (Supplementary Fig. S10).

The characteristics of this flow provide several attractive features for present purposes, one of which is immediately evident from inspection of Fig. 2a,b. At large V_{DS} ($V_{DS}/L_{ch} > 1$ V μm^{-1}), the trenches associated with SWNTs that have pronounced hot spots exhibit uniform widths. Likewise, SWNTs that show vastly different temperatures at a given V_{DS} display similar trench widths at sufficiently large V_{DS} ($V_{DS}/L_{ch} > 1$ V μm^{-1}). Figure 2e presents results for the second SWNT from the right, extracted from Fig. 2a and the bottom frame of Fig. 2b. Clearly, the variations (between the mean value and maximum value) in expansion measured along the length of the SWNT are much larger than those in the trench widths (W_{Tc}), as quantified by separations between the raised regions of thermocapillary resist at the edges of the trench. This physics provides an ability to realize trenches with small, uniform widths, even across large-scale arrays that incorporate m-SWNTs with wide ranges of conductances and diameters, and consequently, peak temperatures and thermal gradients. Figure 2f shows the average W_{Tc} for a number of different, individual SWNTs as a function of Q_0. Similar values occur over ranges of power (~10–40 μW μm^{-1}) that exceed those associated with optimized conditions for purification. This behaviour is much different from that expected from other thermally driven processes, such as sublimation or ablation, which typically involve abrupt temperature thresholds (Supplementary Fig. S13).

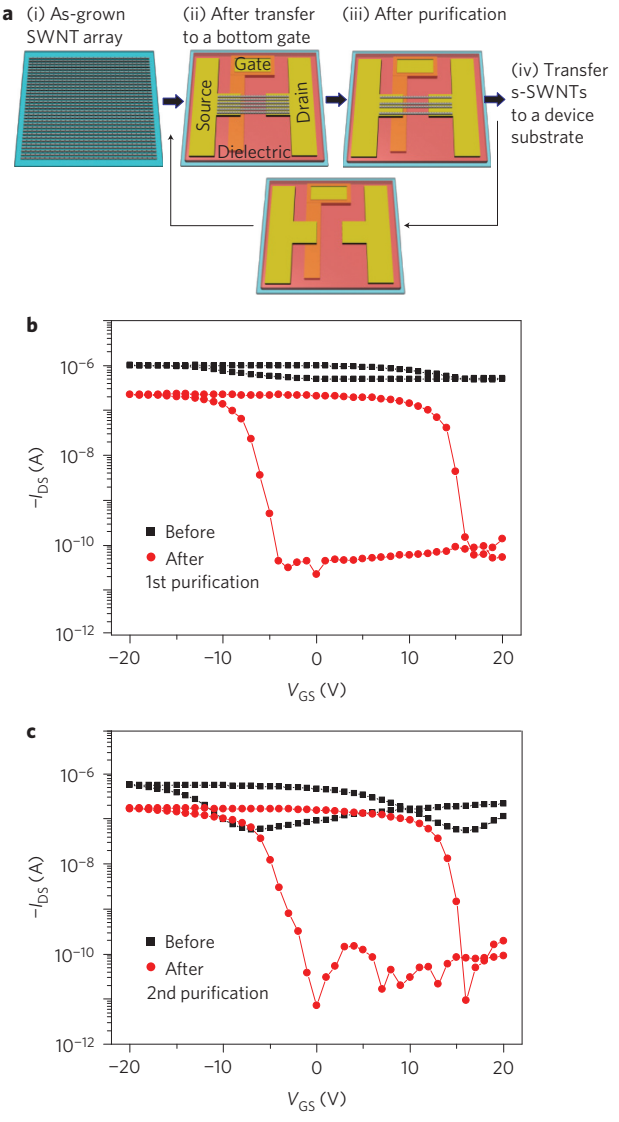

Figure 5 | Thermocapillary purification process performed with a reusable bottom split gate structure. a, Schematic illustration of two purification processes implemented on different arrays of SWNTs using a single bottom split gate electrode structure. (i) As-grown array of aligned SWNTs. (ii) Bottom electrode after transfer of these SWNTs (gate dielectric, red; source and drain electrodes, gold; gate electrode, gold). (iii) s-SWNTs remaining after purification. (iv) Transfer of s-SWNTs to a device substrate. **b**, Transfer characteristics before and after a first purification process with a bottom electrode structure: $I_{on,a}/I_{on,b} = 23\%$ and the on/off ratio after purification is ~1×10^4. **c**, Transfer characteristics before and after a second purification process with the same bottom electrode structure: $I_{on,a}/I_{on,b} = 30\%$ and the on/off ratio is ~2×10^4. This reusable structure has $W = L = 30$ μm.

The governing equation of motion for thermocapillarity in systems where the dimension along the SWNTs can be considered infinite corresponds to unidirectional flow in which the thickness profile in the thermocapillary resist can be written as $h(x,t)$ with

$$\frac{\partial \bar{h}}{\partial \bar{t}} + \frac{\partial}{\partial \bar{x}}\left[\frac{\bar{\tau}\bar{h}^2}{2\bar{\mu}} + \frac{\bar{h}^3}{3\bar{\mu}}\frac{\partial}{\partial \bar{x}}\left(\bar{\gamma}\frac{\partial^2 \bar{h}}{\partial \bar{x}^2}\right)\right] = 0 \quad (2)$$

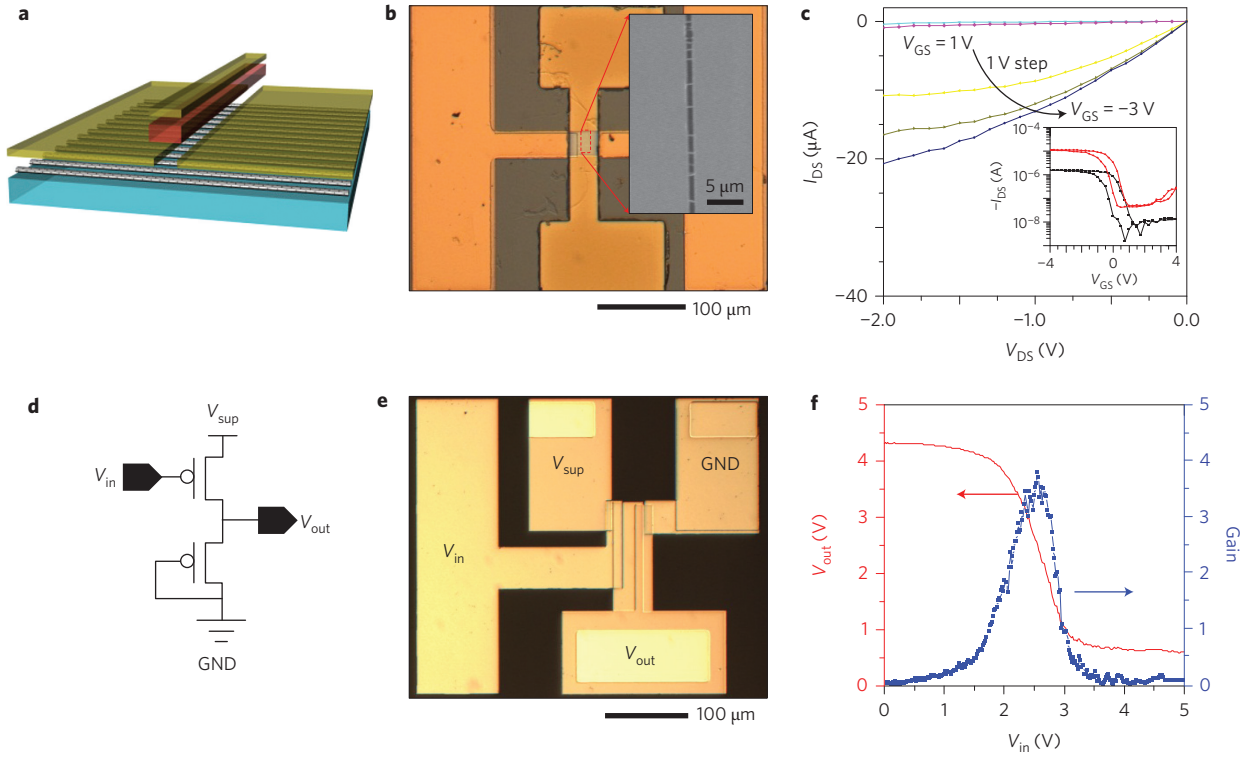

Figure 6 | Short channel transistors and logic gates that use s-SWNT arrays created by thermocapillary purification. a, Schematic illustration of the geometry of a short channel ($L \approx 800$ nm) transistor that incorporates an array of s-SWNTs formed by the thermocapillary purification process (~10 s-SWNTs). **b**, Optical micrograph and scanning electron microscope image of the device (taken before deposition of the gate dielectric). **c**, Output characteristics for gate bias of $V_{GS} = -3, -2, -1, 0, 1$ V and $V_{DS} = -2$ to 0 V. Inset: transfer characteristics for $V_{DS} = -0.1$ V (black) and -1 V (red). **d**,**e**, Circuit diagram (**d**) and optical micrograph (**e**) of an inverter formed with two transistors that use arrays of s-SWNTs formed by thermocapillary purification. **f**, Voltage transfer characteristics of the inverter.

where $\bar{h} = h/h_f$, $\bar{x} = x/h_f$, $\bar{t} = \gamma_1 Q_0 t/(\mu_0 k_f h_f)$, $\bar{\mu} = \mu/\mu_0$, $\bar{\gamma} = k_f \gamma/(Q_0 \gamma_1)$, $\bar{\theta} = k_f \theta/Q_0$, $\bar{\tau} = \partial\bar{\theta}/\partial\bar{x}$ is the thermocapillary stress, μ is viscosity at temperature T, μ_0 is the viscosity at the background temperature $T = T_\infty$, γ is the surface tension, which often exhibits a linear dependence on temperature (that is, $\gamma = \gamma_0 - \gamma_1\theta$) and the bars over symbols indicate the normalized nondimensional variables. Figure 3a shows the geometry. The appropriate initial condition is $\bar{h}(\bar{x}, \bar{t} = 0) = 1$. The boundary conditions are $\bar{h}(\bar{x} = \pm\infty, \bar{t}) = 1$ and zero pressure, $(\partial^2\bar{h}/\partial\bar{x}^2)(\bar{x} = \pm\infty, \bar{t}) = 0$. With equation (1) for the temperature, numerical solutions to this system yield $\bar{h} = h/h_f$, based on assumptions that (i) at each point along x, the temperature throughout the thickness of the thermocapillary resist is equal to the temperature at its interface with the substrate and (ii) flow in the thermocapillary resist does not change the temperature distributions. Figure 3b shows results for the case of polystyrene[41], which exhibits behaviours like the thermocapillary resist (Supplementary Fig. S12) but has a known temperature-dependent surface tension: $\gamma = 50.40 - 0.0738\theta$ mJ m^{-2}. For this example, $\bar{\mu} = 1$, consistent with the small rise in temperature, and $Q_0 = 16.7$ μW μm^{-1} (from experiment). The trenches gradually widen and deepen with time, as the displaced material forms ridges at the edges. Topographical measurements of a representative SWNT coated with thermocapillary resist after Joule heating for various time intervals ($V_{DS}/L_{ch} \approx 0.7$ V μm^{-1}, 30 °C background heating, Supplementary Movie S1) show similar behaviours and profiles (Fig. 3c,d). At longer times, wider trenches result, to the point where SWNTs can be clearly observed at the base (Fig. 3e). Although the specific time durations needed to form complete trenches ($\bar{t} \approx 1$) yield computed values of W_{Tc} that are larger than those observed experimentally, the theory captures the essential time dependence. For example, Fig. 3f shows the measured time dependence of W_{Tc} for two SWNTs; both roughly follow the expected theoretical behaviour, namely $W_{Tc} \approx t^{0.25}$ (Supplementary Figs S7–S9 and Supplementary Movie S1). Another prediction of the theory is that, for a given time $t = 300$ s, the value of W_{Tc} depends only weakly on Q_0 over a remarkably large range, that is, from ~10 μW μm^{-1} to ~35 μW μm^{-1} (Supplementary Fig. S9). This finding is consistent with observations discussed in the context of Fig. 2. Finally, besides capturing the underlying physics, these models also suggest that optimal materials properties for thermocapillary resists include large temperature coefficients of surface tension and low viscosities. Furthermore, decreasing the thickness reduces the trench widths. Empirical studies of various materials for thermocapillary resists (Supplementary Fig. S12) led to the selection of the molecular glass reported here.

Application of the purification process

The envisioned use of thermocapillary-enabled purification is in a preparatory mode, where it serves as one of several steps including substrate cleaning, SWNT growth, transfer, and others that occur before device processing. Such a scheme decouples purification from any detailed consideration of component or circuit layout, and is made possible by the ability to entirely eliminate all m-SWNTs. Two approaches can be considered. In the first, one or a small number of electrode structures, each with large lateral extent as illustrated in Fig. 4a.b, enable elimination of m-SWNTs over significant areas. Here, processing occurs on hundreds or thousands of SWNTs at once, using pulsed currents to avoid cumulative heating (Supplementary Fig. S11). Figure 4c shows the electrical characteristics of the structure in Fig. 4a before and after purification, where $I_{on,a}/I_{on,b}$ is ~20% and the on/off ratio after the process is ~1×10^3,

similar to the results achieved on small arrays discussed previously. Current outputs can reach the milliamp range, as shown in Fig. 4c and Supplementary Fig. S23. Additional details and examples of outputs up to ~3 mA appear in Supplementary Fig. S24. Figure 4d illustrates an alternative approach, in which smaller pairs of interconnected electrodes provide for purification in distributed regions, capable of lithographic alignment at a coarse level to areas of interest in a final application. Effects on I_{on} and I_{off} in this case are in the range of those achieved in other geometries (Supplementary Fig. S15, Table S2). The process can be applied to arrays of SWNTs that have both local (Supplementary Fig. S14) and area-averaged (Supplementary Fig. S11) densities of a few per micrometer. Improved densities can be realized using transfer techniques[42–44]. Although high densities can be important in electronics, modest or low densities can be useful in sensors and other devices.

To simplify implementation, a reusable bottom electrode structure can be constructed to eliminate cycles of processing that would otherwise be necessary for the repetitive fabrication of top electrode structures described previously. As shown in Fig. 5a, a single, reusable substrate provides a fully formed, bottom split gate structure for use in the purification process. Aligned arrays of SWNTs transferred to this substrate using techniques described previously[42–44] can be processed to remove m-SWNTs. The remaining s-SWNTs can then be transferred to a final device substrate. Figure 5a schematically illustrates two cycles of this process. Figure 5b,c presents transfer characteristics of arrays of SWNTs before and after purification, performed with a single back-gate structure in two separate cycles of use. Additional details appear in Supplementary Figs S19 and S20.

Because the purification occurs on entire arrays SWNTs, the resulting s-SWNTs can be easily integrated into nearly any type of component or circuit layout. Devices with short channel lengths (~800 nm) defined using a near-field phase-shift lithography technique[45] were used to provide a demonstration, as shown in Fig. 6a,b. Figure 6c presents electrical properties that are consistent with those of long-channel devices when effects of contact resistance are included. The observed hysteresis has known origins that can be minimized using strategies described elsewhere[46–49]. A simple logic gate, consisting of two transistors using arrays of s-SWNTs, provides an additional example of the utility of this process, as illustrated in Fig. 6d,e. Figure 6f shows the voltage transfer characteristics and gain associated with this p-type inverter. The peak gain is ~4, consistent with expectation for this design (Supplementary Figs S16 and S17).

Conclusions

In summary, the purification method introduced here provides scalable and efficient means for converting heterogeneous arrays of SWNTs into those with purely semiconducting character. An important advantage is that the processing steps are fully compatible with fabrication tools used for the commercial manufacture of digital electronics and display backplanes. Enhanced control might also allow refined forms of purification, based not just on differences between m-SWNTs and s-SWNTs, but also on values of threshold voltage or other more subtle characteristics among the s-SWNTs themselves. Other promising opportunities for future work include the development of schemes for purifying high-density arrays, and for eliminating the need for electrode structures by electromagnetically induced heating in spectral ranges where m-SWNTs exhibit stronger absorption than s-SWNTs.

Methods

Fabricating top-electrode structures. Photolithography, electron-beam evaporation (2 nm Ti, 48 nm Pd; AJA) and liftoff were used to define source and drain electrodes. RIE (100 mtorr, 20 s.c.c.m. O_2, 100 W, 30 s; Plasma-Therm) removed SWNTs everywhere except for regions between these electrodes. Prebaking (250 °C, 2 h, in a glovebox) a spin-cast (4,000 r.p.m., 60 s) solution to a spin-on glass (SOG; Filmtronics, methylsiloxanes 215F, 15:1 diluted in isopropyl alcohol)[50] and then curing the material formed films of SOG (35 nm) uniformly across the substrate. Atomic layer deposition (80 °C; Cambridge NanoTech) created films of Al_2O_3 (30 nm) on top of the SOG. Photolithography (AZ 5214) and etching (6:1 buffered oxide etchant for 50 s) removed the SOG/Al_2O_3 bilayer from the region between the source and drain electrodes. Prebaking (110 °C, 10 min) a spin-cast (4,000 r.p.m., 60 s) solution of polyvinyl alcohol (PVA; M_w between 89,000 and 98,000, 99%, hydrolysed, Sigma-Aldrich; solvent, deionized water) mixed with photosensitizer (ammonium dichromate, >99.5% at 40:1 by weight[49]) followed by photolithographic patterning and postbaking (110 °C, 30 min) defined a layer of PVA (~400 nm) on top of and aligned to the SOG/Al_2O_3. Photolithography (AZ 5214), electron-beam evaporation (50 nm Ti or Cr) and liftoff were then used to define a gate electrode on top of this dielectric stack.

Thermocapillary flow and etching to remove m-SWNTs. Thermal evaporation (0.5Ås^{-1}) was used to form thin layers (25 nm) of thermocapillary resist (α,α,α′-tris(4-hydroxyphenyl)-1-ethyl-4-isopropylbenzene; TCI International). Applying a voltage between the source and drain electrodes ($V_{DS} = -40$ to -50 V, corresponding to fields of $V_{DS}/L_{ch} \approx 1.33$–$1.66$ V μm^{-1}) while biasing the source/gate to +20 V under vacuum (~1×10^{-4} torr, Lakeshore) and holding the substrate temperature at 60 °C, all for ~5 min, yielded trenches in the thermocapillary resist at the locations of the m-SWNTs. RIE (10 mtorr, 1 s.c.c.m. O_2, 1 s.c.c.m. CF_4, 75 W, 20 s; Plasma-Therm RIE) eliminated the m-SWNTs exposed in this manner, without affecting the s-SWNTs. Immersion in acetone for 30 min removed the thermocapillary resist, to complete the process.

Scanning Joule expansion microscopy. Devices were wire-bonded to a sample holder (Spectrum Semiconductor Materials) to allow contact-mode AFM (Asylum MFP 3D and Cantilever Asylum # Olympus AC240TS) while applying suitable biases to the electrode structures. A function generator (Agilent 33250A) provided the a.c. bias and the reference signal for lock-in (Stanford SR844) detection of the amplitude and phase of the signal associated with thermal expansion. Measurements on quartz were performed with thick layers (~100 nm) of thermocapillary resist deposited on arrays of SWNTs between two electrodes (that is, two-terminal devices with $L = 30$ μm and $W = 30$ μm). The bias consisted of a sinusoidal voltage with amplitude of 5 V and frequency of 386 kHz. Measurements on SiO_2(200 nm)/Si were carried out with similar two-terminal devices, but with spin-cast overcoats of poly(methylmethacrylate) (Microchem 950 A2) with thicknesses of ~120 nm. The bias in such cases consisted of a sinusoidal voltage with amplitude of 3 V and frequency of 30 kHz, with the substrate electrically grounded.

Studying the kinetics of thermocapillary flow. Thermal evaporation formed thin layers of thermocapillary resist (~25 nm) on two-terminal devices ($L = 30$ μm, $W = 100$ μm) configured for electrical connection while in the AFM (Asylum Research ORCA sample mount). Images collected by fast scanning (~30 s acquisition times) defined the topography of a small region of interest. Between scans, application of electrical biases for durations short compared to the normalized flow rates (0.1 s at short times and increasing to 30 min at long times) caused the trenches to increase in width by controlled amounts. A total of ~400 scans, corresponding to the device being under bias for a total accumulated time of ~8 h, revealed the kinetics of trench formation throughout and well beyond the time of interest.

Fabricating reusable bottom electrode structures. Photolithography and etching defined gate electrodes (2 nm Cr and 13 nm Pd). A bilayer of silicon nitride (STS 200 nm by plasma-enhanced chemical vapour deposition) and SOG (35 nm)[45] served as a gate dielectric. Source and drain electrodes (2 nm Cr and 13 nm Pd) were formed using the same procedures as those for the gate, thereby completing the fabrication.

Finite-element modelling of heat flow. The three-dimensional finite-element model for the temperature distributions used eight-node, hexahedral brick elements in a finite-element software package (ABAQUS) to discretize the geometry. The SWNT was treated as a volume heat source, with a zero heat flux boundary at the top surface of Tc-resist, and a constant temperature T_∞ at the bottom of the quartz substrate.

Numerical modelling of thermocapillary flows. The equations of motion represent a pair of coupled partial differential equations

$$\frac{\partial \bar{h}_1}{\partial \bar{t}} = \frac{\partial}{\partial \bar{x}}\left(-\frac{\bar{\tau}\bar{h}_1^2}{2\bar{\mu}} - \frac{\bar{h}_1^3}{3\bar{\mu}}\frac{\partial \bar{\gamma}}{\partial \bar{x}}\bar{h}_2 - \frac{\bar{h}_1^3}{3\bar{\mu}}\bar{\gamma}\frac{\partial \bar{h}_2}{\partial \bar{x}}\right)$$

and

$$\frac{\partial^2 \bar{h}_1}{\partial \bar{x}^2} - \bar{h}_2 = 0$$

where $\bar{h}_1 = \bar{h}$. The boundary conditions are $\bar{h}_1(\bar{x}, \bar{t} = 0) = 1$ $\bar{h}_2(\bar{x}, \bar{t} = 0) = 0$, $\bar{h}_1(\bar{x} = \pm\infty, \bar{t}) = 1$ and $\bar{h}_2(\bar{x} = \pm\infty, \bar{t}) = 0$. A Fortran routine (PDE_1D_MG) was used to solve these two partial differential equations directly.

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Author contributions

S.H.J., S.N.D. and J.A.R. conceived and designed the experiments. S.H.J., S.N.D., X.X., A.I., J.K., F.D., J.S., J.F., M.M., E.C. and K.G. performed the experiments. J.S., C.L., Y.L., F.X., M.A.W., M.A.A. and Y.H. performed modelling and simulations. E.P., M.A.A., B.K., Y.H. and J.A.R. provided technical guidance. S.H.J., S.N.D., X.X., J.S., Y.H. and J.A.R. analysed the experiments and simulations. S.H.J., S.N.D., J.S. and J.A.R. wrote the manuscript.

Additional information

Supplementary information is available in the online version of the paper. Reprints and permissions information is available online at www.nature.com/reprints. Correspondence and requests for materials should be addressed to J.A.R.

Competing financial interests

The authors declare no competing financial interests.

Correction notice
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Using nanoscale thermocapillary flows to create arrays of purely semiconducting single-walled carbon nanotubes

Sung Hun Jin, Simon N. Dunham, Jizhou Song, Xu Xie, Ji-hun Kim, Chaofeng Lu, Ahmad Islam, Frank Du, Jaeseong Kim, Johnny Felts, Yuhang Li, Feng Xiong, Muhammad A. Wahab, Monisha Menon, Eugene Cho, Kyle L. Grosse, Dong Joon Lee, Ha Uk Chung, Eric Pop, Muhammad A. Alam, William P. King, Yonggang Huang and John A. Rogers

In the original version of this file posted online on 28 April 2013 there were some typos: Author names should have read Muhammad A. Wahab and Kyle L. Grosse. Page 44, last line 'V_{GS}, V_{DS} using[22].' should have read 'V_{GS}, V_{DS} using Eq. (22).' On Fig. S1c it should have read 'No trench, image missing'. In Fig. S27 caption: '…V_{DS} = 20 V and, therefore, calculated on/off ratio (that is, I_{DS}@V_{GS} = -20 V/I_{DS}@V_{GS} = 20 V.' should have read '…V_{GS} = 20 V and, therefore, calculated on/off ratio (that is, I_{DS}@V_{GS} = -20 V/I_{DS}@V_{GS} = 20 V) goes down.'; 'parallel-gate FET' should have read 'partial-gate FET'. These errors have been corrected in this file 16 May 2013.

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SUPPLEMENTARY INFORMATION

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Using Nanoscale Thermocapillary Flows to Create Purely Semiconducting Arrays of Single Walled Carbon Nanotubes

(Online Supplementary Information)

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Individual SWNT thermocapillary trench experiments

Thermocapillary flows in thermocapillary resists (Tc-resists) were studied (5 min, 60 ˚C background heating) using devices that incorporate single or several SWNTs. Devices were fabricated in geometries to ensure that only 1 or 2 SWNTs were present in the channel, as confirmed by AFM. In the case of single SWNT devices, the electronic type could be determined directly from the electrical properties (on/off ratio > 100, s-SWNT; on/off ratio < 100, m-SWNT). For devices with 2 SWNTs that exhibited high on/off ratio, both SWNTs must be s-SWNTs. For similar devices with low on/off ratio before thermocapillary enabled purification (TcEP) and high on/off ratio after TcEP, one SWNT must be a m-SWNT and the other a s-SWNT. Devices with two m-SWNTs were not used for these experiments. Biases were applied to increase the resistance of the s-SWNTs (i.e. their "off" state, at +20 V_{GS}), resulting in relatively low (high) current levels for all s-SWNTs (m-SWNTs). As a result, all 2 SWNT devices fell into one of two cases: their currents were dominated by a single m-SWNT or they contained two s-SWNTs. For the second case, one s-SWNT is likely to dominate, but at worst, the s-SWNT have roughly equal current levels in which case the data served as an upper limit for the actual current and could be as little as half that level. The large number of devices that were studied and the observation that most s-SWNTs showed current levels more than ten times below the threshold for trench formation suggest that assumptions concerning relative current distributions in s-SWNTs are unlikely to affect the broad conclusions. The thresholds were accurately defined by devices with just one SWNT. We performed systematic studies of trenches formed under a range of input powers for single s-SWNTs and single m-SWNTs. A range of outcomes for input powers between 0.1-30 μW/μm (SWNT length = 30 μm) were observed by AFM (Fig. S1a). For all experiments, powers below 3.3 μW/μm led to no trenches.

For powers between 3.3-10 μW/μm most devices exhibited trenches, but only partly along the lengths of the SWNTs. For all experiments with powers greater than 10 μW/μm, trenches with widths W_{Tc}~250-300 nm, were observed along the entire lengths of the SWNTs. This analysis provides information on threshold powers for trench formation, which, via analytical modeling, can be correlated to peak temperatures of ~2-5 ˚C. By sorting these same results by input field and SWNT electronic type (Fig. S1b), optimized conditions can be established. At fields below the optimal range, the heating is insufficient to yield trenches along the entire lengths of all of the m-SWNTs; at higher fields, the most conductive s-SWNTs begin to show partial trench formation. However, for optimized conditions, all s-SWNTs yielded no trenches, while all m-SWNTs yield complete trenches, as required for proper operation of TcEP.

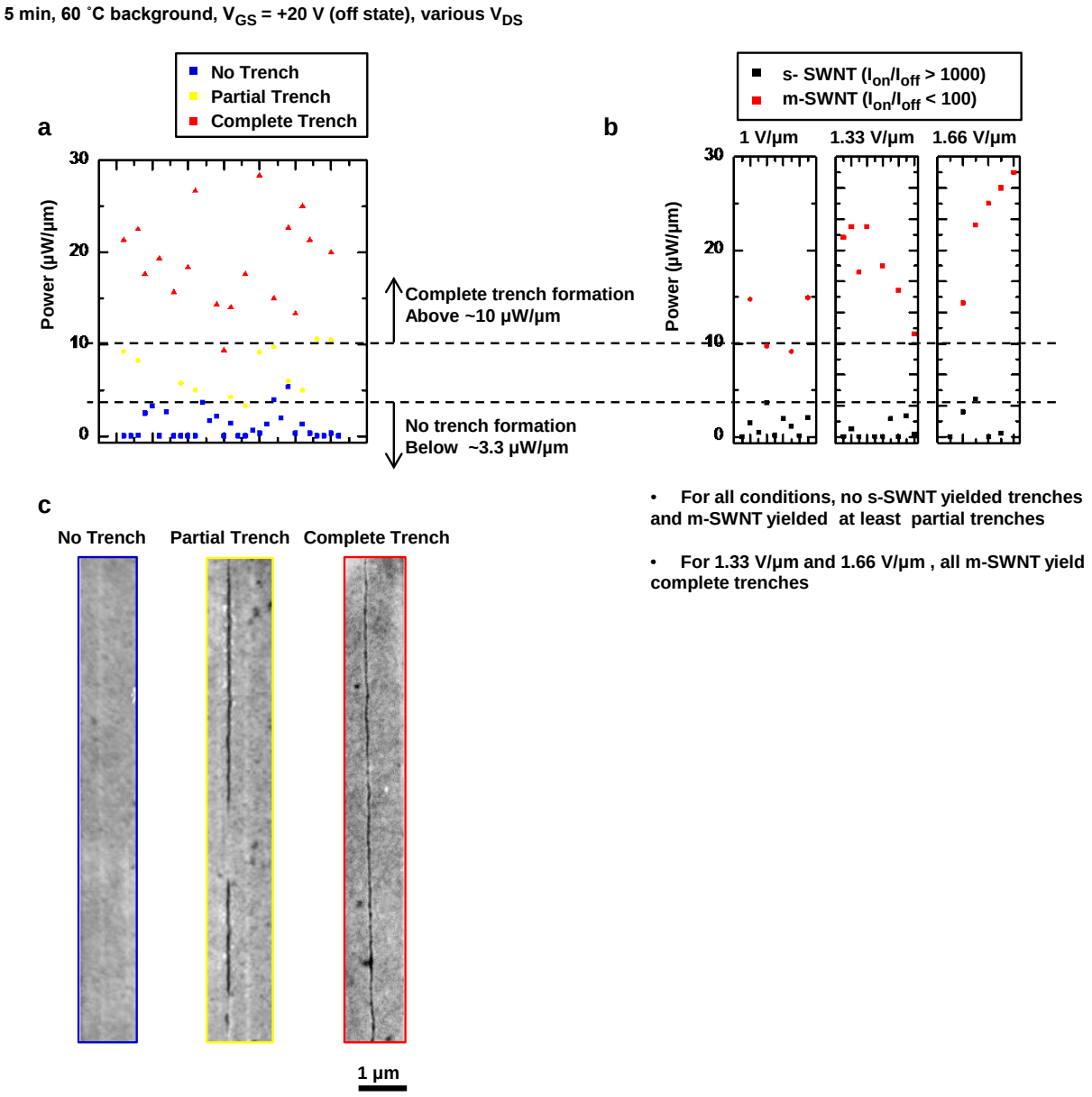

Figure S1. Critical power for trench formation. Summary of results on experimental investigations of trench formation (5 min, 60 ˚C) in devices with single or several SWNT, in which an individual SWNT contributed a majority of the current. The findings define the critical power density to form trenches. All experiments were performed with s-SWNT in their "off" state (+20 V_G). (a) Scatter plot of device-level power density associated with the experiments. All devices with power density below 3.3 μW/μm show no trenches (blue), all devices with power density above 10 μW/μm show complete trenches along the entirety of their length (red), while those with intermediate powers show trenches along part of their length (yellow). Here, local variations in resistance along the length of the SWNT yield powers sufficient for trench formation in some, but not all regions of the SWNT. (b) The same set of experiments, organized by source-drain bias and SWNT electronic type. Although there is a large variation in the power associated with various SWNT at a given bias condition, for optimized conditions (-1.33 and -1.66 V/μm) all s-SWNT exhibit no trenches, while all m-SWNT exhibit complete trenches along their entire length. (c) Representative AFM images for: no trench (left), partial trench (middle), and complete trench (right) formation.

Deposition conditions for the Tc-resist and its properties

Figure S2a shows the chemical structure of the Tc-resist. The material was deposited via thermal evaporation. Figure S2b shows AFM images of a film deposited on a SiO_2/Si substrate. The surface roughness is comparable to that of the underlying substrate, i.e. 2-3 Å. Experiments that involved heated substrates (quartz or SiO_2/Si) with thin coatings of Tc-resist (~25 nm thickness) showed an onset of dewetting between 80-120 ˚C, depending on substrate hydrophobicity. Clean, hydrophilic surfaces yielded higher dewetting temperatures. In vacuum (~1×10^{-4} torr), sublimation began at ~100 ˚C, as determined by experiments using lithographically patterned, calibrated resistive heaters of Pt (lengths ~1-3 mm, widths ~6-10 μm). Differential Scanning Calorimetry (dry nitrogen) yielded a specific heat of ~1.5 J/C/cm^3 (Fig. S2c, T_m= 225 ˚C, T_g= 95 ˚C, T_{rc}=155 ˚C). Time resolved, picosecond pump-probe experiments based on thermoreflectance[1] using relatively thick films (300 nm, Fig. S2d) yielded thermal conductivities of ~0.2 W/m/K, similar to most organic thin films. Furthermore, similar experiments with relatively thin films (~25, ~50, ~75 nm), suggest that the thermal interface resistance between quartz and the Tc-resist is ~50-150 MW/m^2/K.

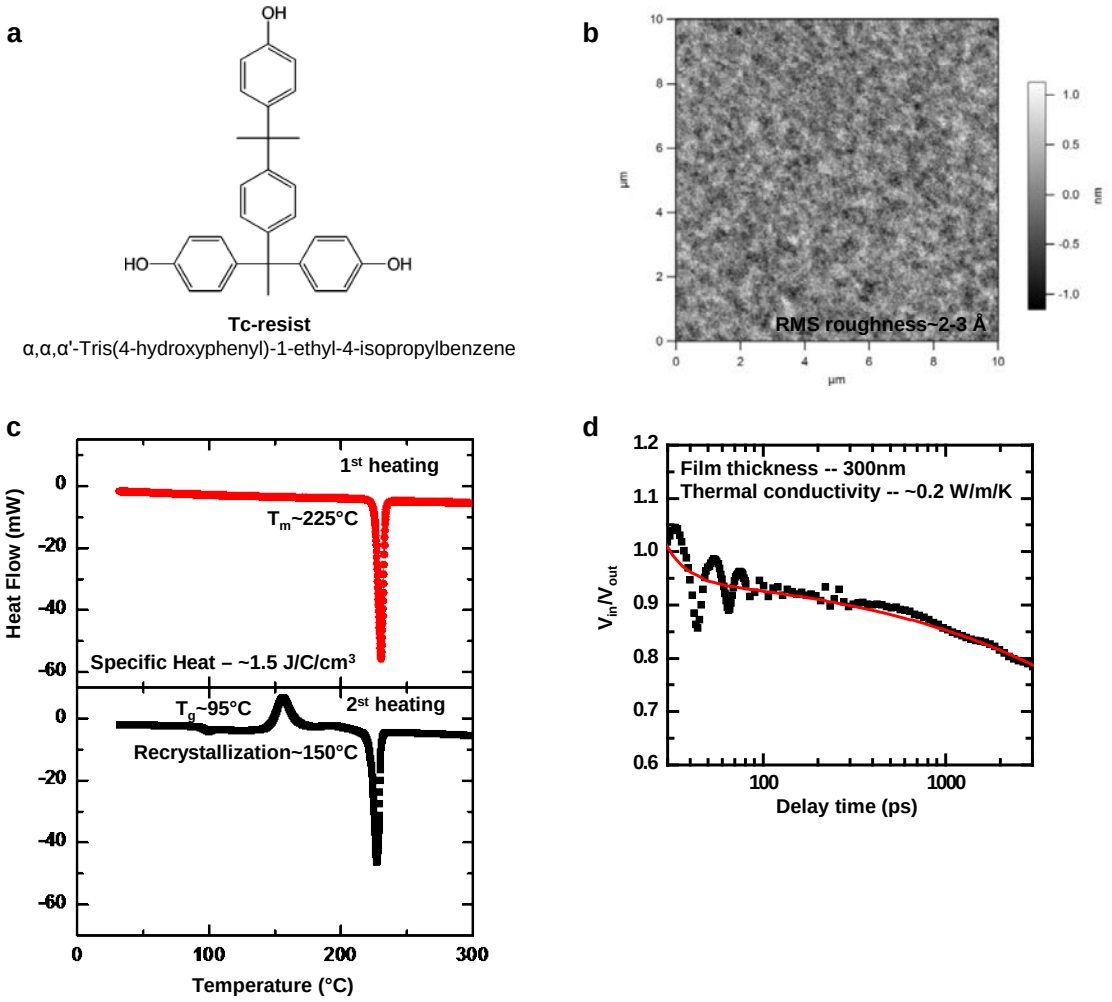

Figure S2. Tc-resist characterization. (a) Chemical structure for Tc-resist. (b) AFM of a pristine film deposited by thermal evaporation (25 nm, ~1Å/s) showing a very smooth surface (2-3 Å RMS roughness, similar to underlying Si substrate). (c) DSC of Tc-resist showing specific heat (~1.5 J/C/cm^3), melting temperature (~225 ˚C), recrystallization (~150 ˚C), and glass transition (~95 ˚C) for a bulk sample. (d) Thermoreflectance for a 300 nm thick film of Tc-resist. Fitting yields thermal conductivities of ~0.2 W/m/K.

Single SWNT conductance statistics

The large number of SWNTs studied by TcEP on devices with small arrays of SWNTs provided statistics on the process. For each array, the number of SWNTs and the values of $I_{on,\,b}$ and $I_{on,\,a}$ (shown for a typical device, Fig S3b) together with an assumption that all of the removed SWNTs are m-SWNTs and all of the remaining SWNTs are s-SWNTs, yields estimates for the average conductance of these two types of SWNTs, for each device. Figure S3a shows a histogram of the conductances of individual SWNTs determined in this way. (We note that a device with 3 s-SWNTs and an average conductance of 50 kΩ/μm is counted 3 times.) The mean conductances for m-SWNTs and s-SWNTs (in their on state) are 17 kΩ/μm and 75 kΩ/μm, respectively. These distributions are in the range of those reported for single SWNTs studied previously[2]; with values of 35 kΩ/μm (m-SWNTs) and 55 kΩ/μm (s-SWNTs) for backgated devices (Fig. S3c)[2]; and 140 kΩ/μm (m-SWNTs) and 1000 kΩ/μm (s-SWNTs) for top gated devices[2]. Using the experimentally observed ratios of numbers of m-SWNTs to s-SWNTs, and a ratio of mean conductances of ~4:1, the assumption that TcEP preserves all s-SWNT is consistent with observations.

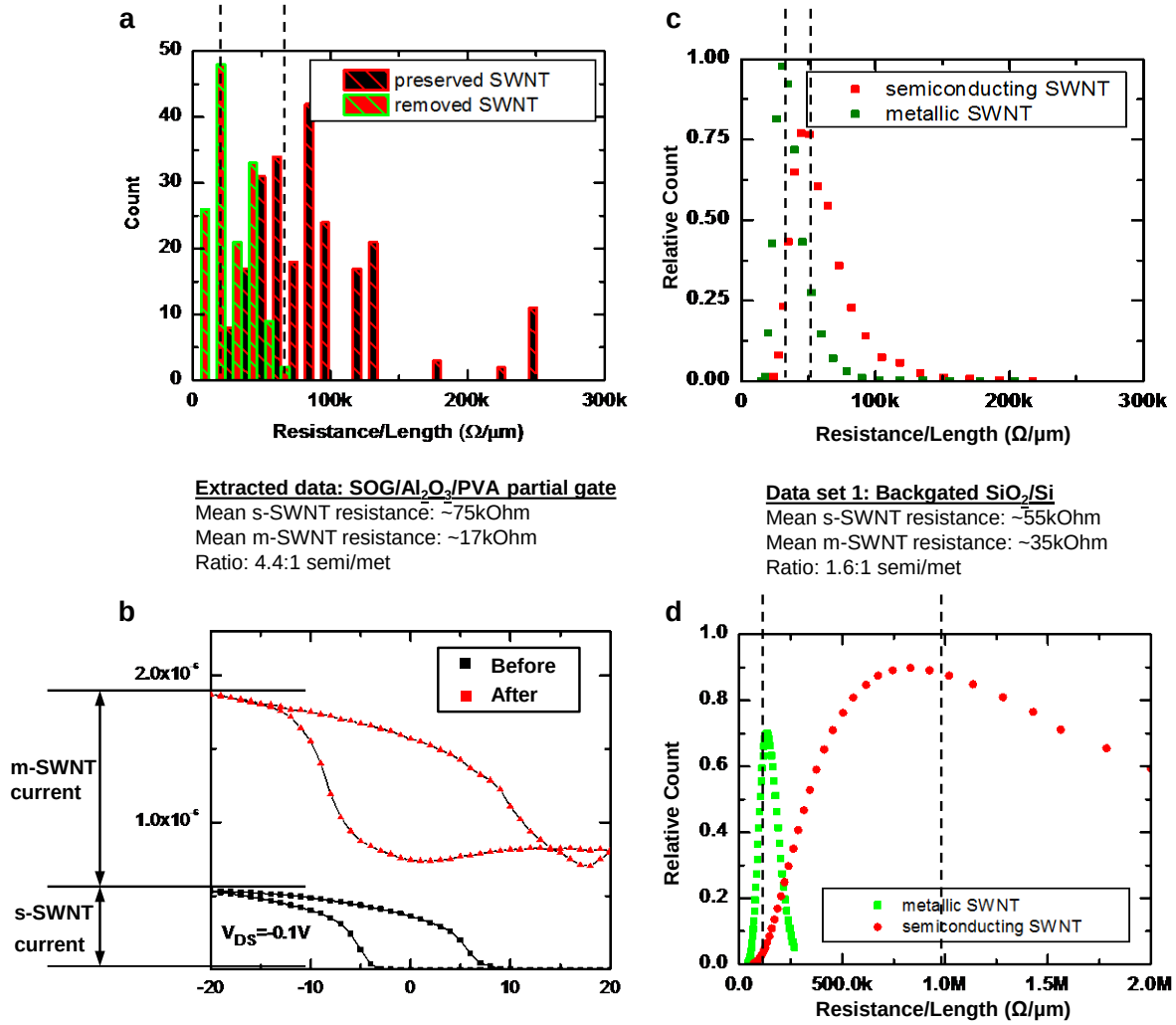

Figure S3. SWNT resistivity data. (a) Extracted average resistivity for m-SWNTs and s-SWNTs based on sorted small area arrays. Average resistivity for each of 37 devices based on device resistance changes before and after TcEP and the number of SWNTs removed and remaining (based on AFM). (b) Typical I-V for an array before and after TcEP showing the relative conductance attributed to both m-SWNT and s-SWNT. (c,d) Histograms showing distributions of individual SWNT resistivities for two data sets, one based on back-gated devices on SiO_2/Si and the other based on top-gated devices with a gate dielectrica of SOG/HfO_2. Distributions representative of previously published results on arrays of SWNT.

Partial gate device properties

The electrode geometries used for TcEP involved a partial gate structure shown schematically in Fig. 1a. This configuration results in reduced gate-drain fields, which minimize Schottky barrier tunneling, band-to-band tunneling and avalanche phenomena[3]. The operation avoids ambipolar conduction at the bias conditions needed for TcEP (characterization at conditions consistent with TcEP, 60 ˚C background heating, ~1×10^4 torr). These effects are clearly observed in transfer characteristics for devices based on an individual s-SWNT in partial gate (Fig. S4a) and full gate (Fig. S4b) layouts. Here, the same SWNT, same pair of source-drain electrodes, and dielectric were used for both devices. The only difference is the length of gate extension into the channel. Both configurations exhibit ideal device behavior at low bias (V_{DS}=-0.1 V). At high bias (V_{DS}<-10 V, L=30 μm), however, the full gate device shows pronounced ambipolar conduction, unlike the partial gate case. Figure S3c illustrates the effect of source-drain bias and gate overlap (L_{ov}) on on/off ratio, where all measurements were performed on the same SWNT. The device with 5 μm gate overlap (i.e. the configuration used for TcEP) exhibits on/off ratios 2-3 orders of magnitude higher than the device with full overlap (L_{ov}=30 μm). Figure S4d shows the ability of the partial gate configuration to maintain current levels several orders of magnitude lower than that of the full gate configuration, even for long bias durations ("off" state, V_{DS}=-40V, V_{GS}=+20V, 5 min, consistent with TcEP experiments).

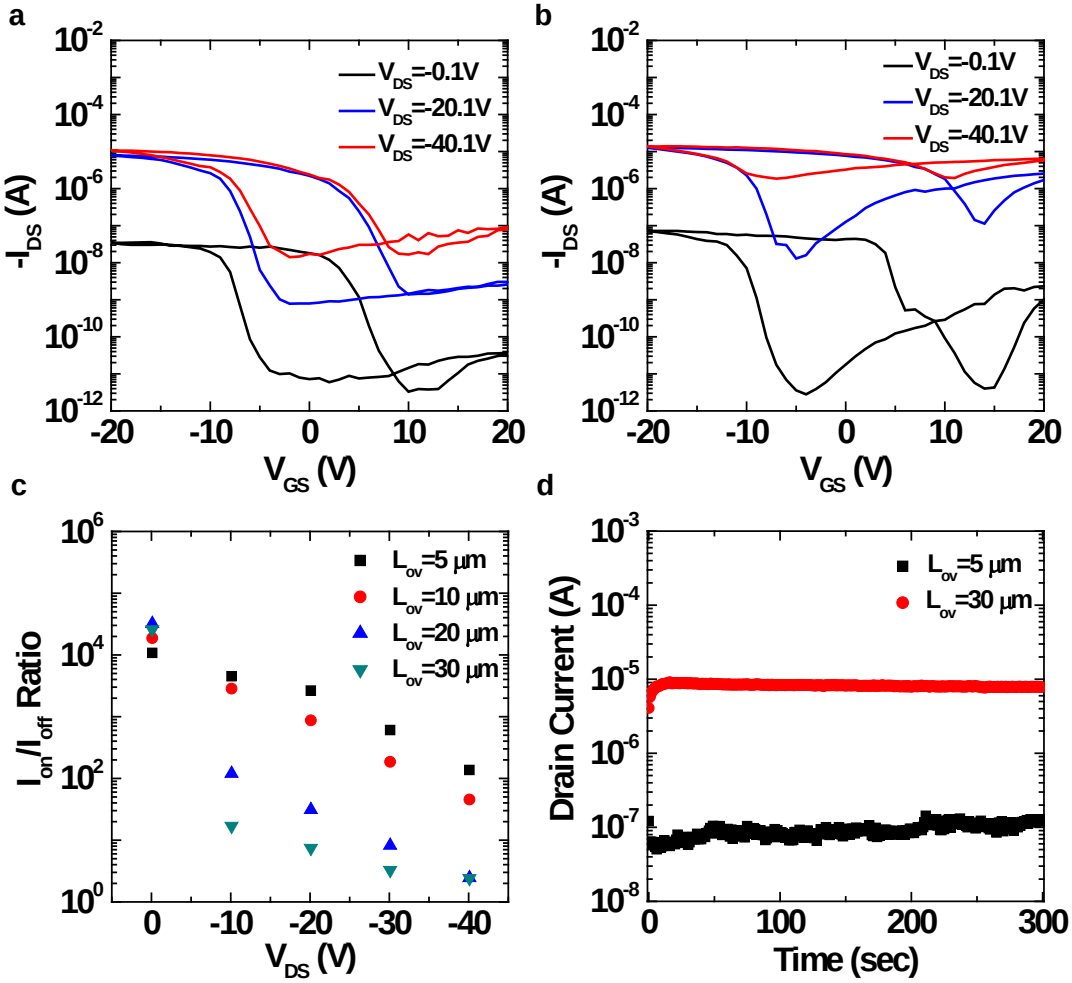

Figure S4. Effect of partial gate transistor geometry. Electrical characterization of an individual SWNT device with varying gate overlap. Transfer characteristics for different drain voltages (V_{DS}=-0.1, -20, -40 V) for the case of (a) partial gate and (b) full gate configurations. (c) I_{on}/I_{off} dependence on gate overlap (L_{ov}) ranging from 5 to 30 µm and (d) drain current associated with devices held in their off state (V_{GS}=+20 V, V_{DS}=-40V) for extended durations, for partial gate and full covered configurations.

Scanning Joule expansion microscopy

Figure S5a shows a scanning Joule expansion microscope (SJEM) image[4] of an array of SWNTs (two terminal device, SiO_2 (200 nm) / Si substrate) covered with a 120 nm thick film of PMMA, collected at the condition of $V(t) = V_{DS}\cos(2\pi ft)$ with V_{DS}=3 V and f=30 kHz and V_{GS}=0 V. Figure S5a shows the integrated expansion percentage (I.E.P.). To determine this quantity, we first located the maximum expansion along each measured cross-section perpendicular to the length of the SWNT. Next, we integrated these values along each SWNT, to get the integrated expansion (I.E.). The I.E.P. is the ratio of the I.E. to the sum of the I.E. for all three SWNTs, times 100%. Since the maximum expansion is proportional to the input power, the I.E.P. can be used to estimate the power input for each SWNT, from the measured total power into the device. Figure S5c shows a 3D rendering of the SJEM signal for the SWNT associated with Fig. 2b. Figure S5d shows a schematic of the SJEM measurement.

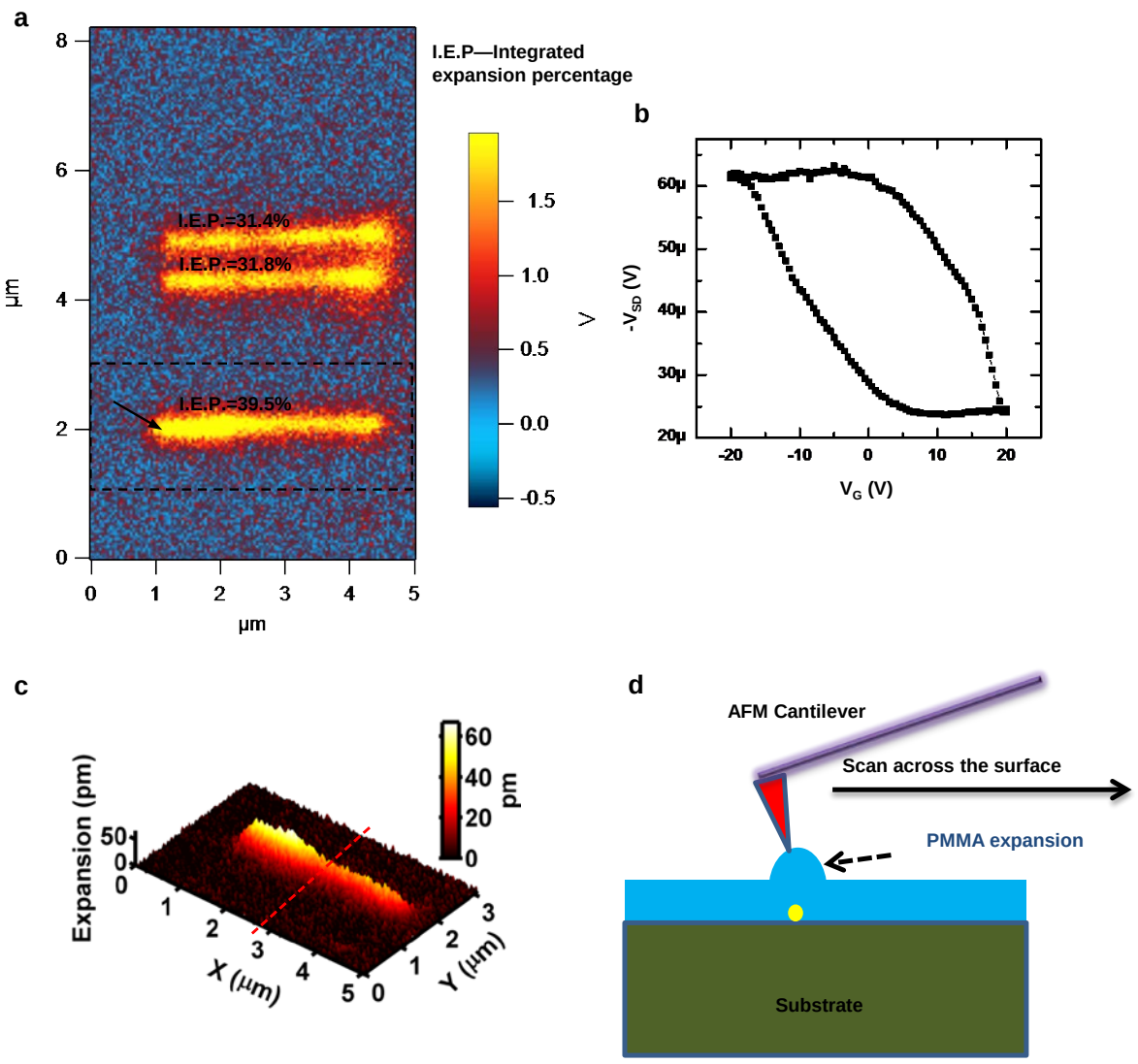

Figure S5. Summary of SJEM measurements. (a) Full SJEM image for an array of 3 SWNTs. The relative integrated intensity for each SWNT is indicated. This relative intensity is used to calculate the relative proportion of the total device power density associated with each SWNT. (b) Transfer characteristic of a device with an array of 3 SWNTs. (c) SJEM image for a SWNT used for validation of analytical temperature models (Fig. 2c). (d) Schematic illustration of SJEM measurements.

Computed temperature distributions associated with Joule heating in individual SWNTs

In this section, we describe procedures for determining the temperature distribution resulting from a SWNT embedded in a film of PMMA on SiO_2/Si substrate with power dissipation at the SWNT for an AC applied voltage. The temperature rise at the surface of the Tc-resist can be obtained by considering first the analytical solution for a disk heat source with radius r_0 at the interface between the Tc-resist and the SiO_2. Here, a cylindrical coordinate system is set such that the origin is coincident with the center of the heat source as shown in Fig. S6a,b. The heat transfer governing equation temperature in cylindrical coordinate is

$$\frac{\partial^2 T}{\partial r^2}+\frac{1}{r}\frac{\partial T}{\partial r}+\frac{\partial^2 T}{\partial z^2}-\alpha\frac{\partial T}{\partial t}=0 \qquad (1)$$

where $\alpha=\frac{k}{c\rho}$ is thermal diffusivity, k is thermal conductivity, ρ is density, and c is specific heat capacity. The subscripts 0, 1 and 2 denote Tc-resist, SiO_2 and Si, respectively. Setting $\theta=T-T_\infty$, where T_∞ is the remote temperature, the above equation is equivalent to

$$\frac{\partial^2 \theta}{\partial r^2}+\frac{1}{r}\frac{\partial \theta}{\partial r}+\frac{\partial^2 \theta}{\partial z^2}=\alpha\frac{\partial \theta}{\partial t} \qquad (2)$$

The boundary conditions are

(1) $z=-h_0$ (top surface)

$$-k_0\left.\frac{\partial \theta}{\partial z}\right|_{z=-h_0}=0 \qquad (3)$$

(2) $z=0$

$$\theta_{0^+} = \theta_{0^-},\ -k_0 \left.\frac{\partial \theta}{\partial z}\right|_{z=0^-} = \begin{cases} Q_1 & 0 \le r \le r_0 \\ Q_{c1} & r_0 < r < +\infty \end{cases},\ -k_1 \left.\frac{\partial \theta}{\partial z}\right|_{z=0^+} = \begin{cases} Q_2 & 0 \le r \le r_0 \\ Q_{c1} & r_0 < r < +\infty \end{cases} \tag{4}$$

where Q_1 and Q_2 satisfy $-Q_1 + Q_2 = \dfrac{P}{\pi r_0^2}$, P is the total power of the disk.

(3) $z = h_1$

$$\theta_{h_1^+} = \theta_{h_1^-} \text{ and } -k_1 \left.\frac{\partial \theta}{\partial z}\right|_{z=h_1} = -k_2 \left.\frac{\partial \theta}{\partial z}\right|_{z=h_1} \tag{5}$$

(4) $z = h_1 + h_2 \sim \infty$

$$\theta_{h_1+h_2} = 0 \tag{6}$$

For a voltage $V(t) = V_0 \cos(\omega t)$ with angular frequency $\omega = 2\pi f$, the Joule heating has angular frequency 2ω. The total power of the disk can then be obtained as $P(t) = P_0\left[1+\cos(2\omega t)\right]/2$, which yields a constant temperature rise (DC component) due to $P_0/2$ and a time oscillating temperature rise (AC component) due to $P_0 \cos(2\omega t)/2$. It should be noted that the DC component of temperature rise can be easily obtained by setting ω=0 in the solution of AC component.

The time oscillating temperature rise (AC component) has the same frequency as the power density, i.e. $\theta(r,z,t) = \theta(r,z)\exp(2\omega t i)$. Therefore, we have

$$\frac{\partial^2 \theta}{\partial r^2} + \frac{1}{r}\frac{\partial \theta}{\partial r} + \frac{\partial^2 \theta}{\partial z^2} - q^2\theta = 0 \tag{7}$$

where $q^2 = \frac{2\omega i}{\alpha}$ and $\theta = \theta(r, z)$.

Equation (7) can be solved via the Hankel transform, for which the following transform pair of the first kind is applicable,

$$\begin{aligned} \varphi(r,z) &= \int_0^\infty \overline{\varphi}(\xi,z) J_0(\xi r)\xi \mathrm{d}\xi \\ \overline{\varphi}(\xi,z) &= \int_0^\infty \varphi(r,z) J_0(\xi r) r \mathrm{d}r \end{aligned} \tag{8}$$

where $\varphi(r,z)$ is the original function, $\overline{\varphi}(\xi,z)$ is the transform, and J_0 is the 0^{th} order Bessel function of the first kind. Equation (7) then becomes

$$\frac{d^2\overline{\theta}}{dz^2} - (\xi^2 + q^2)\overline{\theta} = 0 \tag{9}$$

Solving the above equation gives

$$\overline{\theta} = A\exp(z\sqrt{\xi^2 + q^2}) + B\exp(-z\sqrt{\xi^2 + q^2}) \tag{10}$$

where A and B are two unknown functions to be determined according to boundary and continuity conditions. The temperature rise is then obtained by

$$\theta = \int_0^\infty \left(A\mathrm{e}^{-\xi z} + B\mathrm{e}^{\xi z}\right) J_0(\xi r)\xi \mathrm{d}\xi \tag{11}$$

Therefore, the temperature rise in Hankel space at each layer is obtained as

Tc-resist: $\overline{\theta}_0(\xi,z) = A_0\exp(z\sqrt{\xi^2 + q_0^2}) + B_0\exp(-z\sqrt{\xi^2 + q_0^2})$

SiO2 layer: $\overline{\theta}_1(\xi,z) = A_1\exp(z\sqrt{\xi^2 + q_1^2}) + B_1\exp(-z\sqrt{\xi^2 + q_1^2})$

Si layer: $\bar{\theta}_2(\xi, z) = A_2 \exp(z\sqrt{\xi^2 + q_2^2}) + B_2 \exp(-z\sqrt{\xi^2 + q_2^2})$

With BCs (3)-(6) in Hankel space, we can obtain the temperature at each layer. For example, A_0 and B_0 are given by

$$A_0 = \frac{\kappa + 1}{(1-\kappa)\left[1 + \exp(-2h_0\sqrt{\xi^2 + q_0^2})\right] + (\kappa + 1)\dfrac{k_0\sqrt{\xi^2 + q_0^2}}{k_1\sqrt{\xi^2 + q_1^2}}\left[1 - \exp(-2h_0\sqrt{\xi^2 + q_0^2})\right]} \frac{P_0}{k_1 \pi \xi \sqrt{\xi^2 + q_1^2}} \frac{J_1(\xi r_0)}{2r_0}$$

$$B_0 = A_0 \exp(-2h_0\sqrt{\xi^2 + q_0^2}) \tag{12}$$

where $\kappa = \dfrac{1 - \dfrac{k_2}{k_1}\dfrac{\sqrt{\xi^2 + q_2^2}}{\sqrt{\xi^2 + q_1^2}}}{1 + \dfrac{k_2}{k_1}\dfrac{\sqrt{\xi^2 + q_2^2}}{\sqrt{\xi^2 + q_1^2}}} \exp(-2h_1\sqrt{\xi^2 + q_1^2})$

The temperature rise due to the disk heat source can be obtained by Eq. (11). For example, the temperature rise in the Tc-resist is obtained as

$$\theta(r, z) = \int_0^{+\infty} A_0 \left[\exp(z\sqrt{\xi^2 + q_0^2}) + \exp(-z\sqrt{\xi^2 + q_0^2} - 2h_0\sqrt{\xi^2 + q_0^2})\right] \cdot J_0(\xi r)\, \xi d\xi \tag{13}$$

The surface temperature rise of the Tc-resist is then obtained by setting $z = -h_0$ as

$$\theta(r) = \int_0^{+\infty} 2A_0 \exp(-h_0\sqrt{\xi^2 + q_0^2}) \cdot J_0(\xi r)\, \xi d\xi \tag{14}$$

As $r_0 \to 0$, we obtain the temperature rise due to a point heat source as

$$\theta_P(r)=\frac{1}{4k_1\pi}\int_0^{+\infty}\frac{(\kappa+1)J_0(\xi r)\xi}{(1-\kappa)\cosh(h_0\sqrt{\xi^2+q_0^2})+(\kappa+1)\dfrac{k_0\sqrt{\xi^2+q_0^2}}{k_1\sqrt{\xi^2+q_1^2}}\sinh(h_0\sqrt{\xi^2+q_0^2})}\cdot\frac{P_0}{\sqrt{\xi^2+q_1^2}}d\xi \tag{15}$$

For a point heat source at $(0,\eta,0)$ with heat generation $P_0=Q_0\cdot d\eta$ and Q_0 as the power density, the integration of Eq. (15) with $r=\sqrt{(\eta-y)^2+x^2}$ gives the temperature rise at point (*x*, *y*) due to a line heat source as

$$\theta(x,y)=\frac{1}{4k_1\pi}\int_{-L/2}^{L/2}d\eta\int_0^{+\infty}\frac{(\kappa+1)J_0\left(\xi\sqrt{(\eta-y)^2+x^2}\right)\xi}{(1-\kappa)\cosh(h_0\sqrt{\xi^2+q_0^2})+(\kappa+1)\dfrac{k_0\sqrt{\xi^2+q_0^2}}{k_1\sqrt{\xi^2+q_1^2}}\sinh(h_0\sqrt{\xi^2+q_0^2})}\cdot\frac{Q_0}{\sqrt{\xi^2+q_1^2}}d\xi \tag{16}$$

It should be noted that Eq. (16) gives the magnitude of time oscillating temperature rise, i.e., θ_0 in the main text is equal to $2\theta(x,y)$. The total surface temperature rise can be obtained as $\theta(x,y,t)=\theta(x,y)\big|_{\omega=0}+\theta(x,y)\cos(4\pi ft)=\left[\theta_1+\theta_0\cos(4\pi ft)\right]/2$ due to a line heat source with power density $Q(t)=Q_0\left[1+\cos(2\omega t)\right]/2$.

Here, boundary conditions involve continuous temperature and heat flow at all material interfaces except those with the SWNT, negligible heat flow at the top surface and a constant temperature at the base of the substrate. For the SWNT interface, discontinuous heat flow, is assumed, as a means to introduce the Joule heat source. The results, together with materials constants taken from the literature (see Supplementary Information, Table S1) and analytical treatments of the resulting thermal expansion, yield expansion profiles that have both peak

magnitudes (E_0~50 pm) and spatial distributions (characteristic widths ~340 nm) that are remarkably consistent with the SJEM results (~40 pm and ~320 nm, respectively), when Q_0 ~ 13 μW/μm, the estimated experimental value.

Computed thermal expansion at the surface of a thin film coating on a heated SWNT on a substrate

Under the assumptions of (1) plane strain in *y* direction since the length of SWNT (~30μm) is much larger than its radius and (2) plane stress in *z* direction since the film is very thin (~25nm), the peak-peak value of AC surface thermal expansion (i.e., the out-of-plane displacement) of the Tc-resist can be obtained as

$$E_0 = \frac{1+\nu_0}{1-\nu_0}\beta_0 h_0 \theta(x, y=-h_0) \tag{17}$$

where ν_0 and β_0 are the Poisson's ratio and coefficient of thermal expansion of the PMMA, respectively.

Computed temperature distribution for a system consisting of a SWNT undergoing Joule heating with a constant bias, on a quartz substrate coated with Tc-resist

Setting $k_2 = k_1 = k_s$, $k_0 = k_f$, $h_0 = h_f$ and ω=0, Eq. (16) gives the surface temperature of Tc-resist for Tc-resist/quartz under DC voltage as

$$\theta(x,y) = \frac{1}{2k_s\pi}\int_{-L/2}^{L/2} d\eta \int_0^{\infty} \frac{Q_0 J_0\left(\xi\sqrt{(\eta-y)^2+x^2}\right)}{\cosh(\xi h_f)+\frac{k_f}{k_s}\sinh(\xi h_f)}\mathrm{d}\xi \tag{18}$$

where k_f and k_s are the thermal conductivity of Tc-resist and quartz, respectively and h_f is the thickness of Tc-resist

A 3D finite element model was established to study the temperature distribution in the system and validate the analytical model. Eight-node, hexahedral brick elements in the finite element software ABAQUS are used to discretize the geometry. A volume heat source was applied on the SWNT. The zero heat flux boundary was applied at the top surface of the Tc-resist, and a constant temperature T_∞ is applied at the bottom of the quartz substrate. The finite element simulations agree well with analytical modeling as shown in Fig. S6c for the surface temperature of the Tc-resist with with $k_0 = 0.2$W/m/K, $k_f = 6$W/m/K, $Q_0 = 16.7\mu$W/μm and L=30μm.

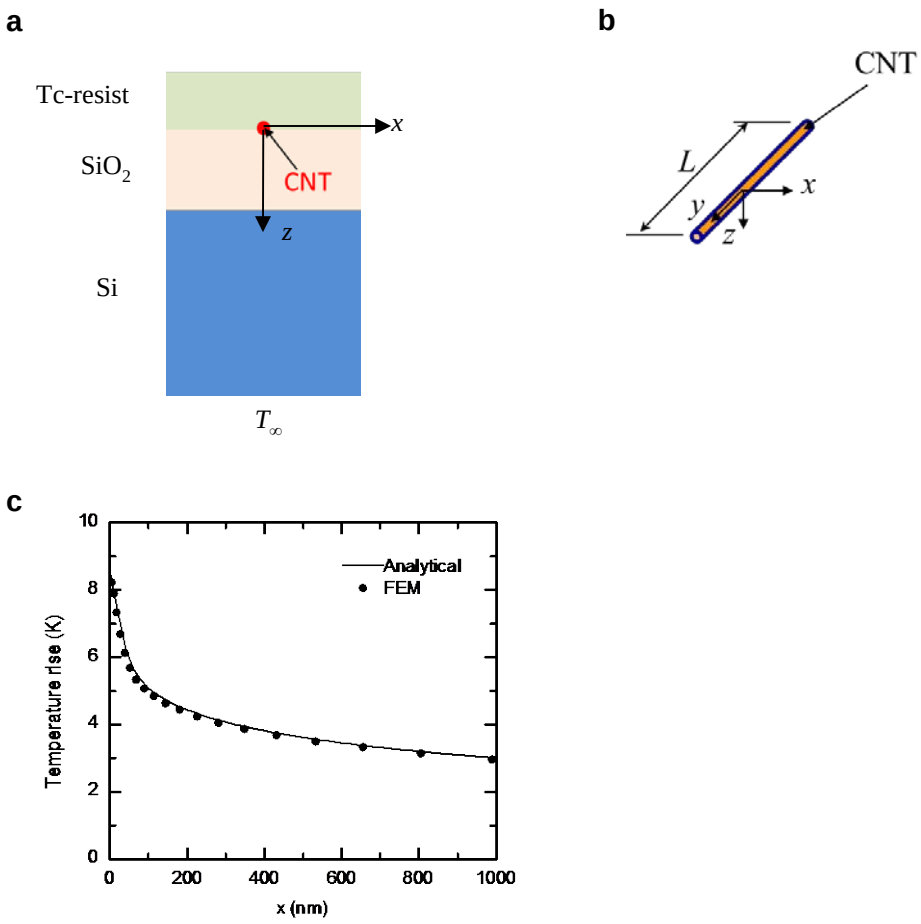

Figure S6. Thermal modeling geometry. (a) Cross-sectional schematic of the film and substrate geometry associated with thermal modeling, with axes defined. (b) Modeling axes defined relative to the position of the SWNT. (c) Tc-resist surface temperature distribution for the case of a heated SWNT on a quartz substrate (16.6 μW/μm)

Table S1. Thermal and Mechanical parameters used in analytical and FE models

Materials	Thermal Conductivity ($Wm^{-1}K^{-1}$)	Thermal Diffusivity $10^{-6}(m^2s^{-1})$	Coefficient of Thermal Expansion $10^{-6}(K^{-1})$	Yong's Modulus 10^9(Pa)	Poisson Ratio
Si	120(ref[5])	73	2.6(ref[6])	165(ref[7])	0.28(ref[8])
SiO2	1.3(ref[9])	0.84(ref[9])	0.50(ref[10])	64(ref[7])	0.17(ref[11])
Quartz	6.0(ref[12])	---	---	---	---
PMMA	0.19(ref[13])	0.11(ref[14])	50(ref[15])	3.0(ref[16])	0.35(ref[17])
Tc-resist	0.2 (meas)	---	---	---	---

Effects of thermal interface resistance

The models above do not consider the effect of thermal interface resistance, which can in some cases affect the resulting temperature distributions. For the case of AC heating for relatively thick films (~250 nm) for PMMA, the interface resistance has negligible effect (for ~100 MW/m^2/K for the SiO_2/PMMA interface, the result is a relatively small increase in peak temperature rise, ~1%). For the case of thinner films of Tc-resist (~25nm) with DC heating, the surface temperature rise incorporating interface resistance can be obtained using Hankel transform as

$$\theta(x,y)=\frac{1}{k_f\pi}\int_{-L/2}^{L/2}d\eta\int_0^{\infty}\frac{Q_0e^{-\xi h_f}\left(1+\frac{k_s\xi}{\zeta}\right)J_0\left(\xi\sqrt{(\eta-y)^2+x^2}\right)}{-\left(1+\frac{k_s\xi}{\zeta}-\frac{k_s}{k_f}\right)e^{-2\xi h_f}+\left(1+\frac{k_s\xi}{\zeta}+\frac{k_s}{k_f}\right)}d\xi \tag{19}$$

where ζ is the thermal interface conductance. As ζ approaches to infinity, Equation (19) denigrates to Eq. (18). For ~100 MW/m^2/K for the Tc-resist/quartz interface, the result shows a ~40% increase in peak temperature rise. However, this rise is not significant enough to affect any of the major conclusions associated with this study. Namely, that at the powers used to induce trenches by Tc-flow, temperature rises are small. Similarly, the qualitative aspects and scaling laws associated with the Tc-flow modeling are unaffected by these minor corrections.

Modeling of thermocapillary flow in TcEP

The viscous flow of Tc-resist is essentially unidirectional and the evolution of film thickness $h(x,t)$ can be obtained from a lubrication equation

$$\frac{\partial h}{\partial t}+\frac{\partial}{\partial x}\left[\frac{\tau h^2}{2\mu}+\frac{h^3}{3\mu}\frac{\partial}{\partial x}\left(\gamma\frac{\partial^2 h}{\partial x^2}\right)\right]=0\,. \tag{20}$$

where γ is the surface tension, which usually linearly depends on the temperature rise (i.e., $\gamma=\gamma_0-\gamma_1\theta$), $\tau=\frac{\partial\gamma}{\partial T}\frac{\partial T}{\partial x}$ is the thermocapillary stress with $T=T_\infty+\theta$, and μ is viscosity. By introducing the following non-dimensional terms $\bar{h}=h/h_f$, $\bar{x}=x/h_f$, $\bar{t}=\gamma_1 Q_0 t/\left(\mu_0 k_f h_f^2\right)$, $\bar{\mu}=\mu/\mu_0$, $\bar{\gamma}=k_f h_f\gamma/\left(Q_0\gamma_1\right)$, $\bar{\tau}=\partial\bar{\theta}/\partial\bar{x}$ and $\bar{\theta}=k_f h_f\theta/Q_0$, Eq. (20) can be written in non-dimensional form as

$$\frac{\partial\bar{h}}{\partial\bar{t}}+\frac{\partial}{\partial\bar{x}}\left[\frac{\bar{\tau}\bar{h}^2}{2\bar{\mu}}+\frac{\bar{h}^3}{3\bar{\mu}}\frac{\partial}{\partial\bar{x}}\left(\bar{\gamma}\frac{\partial^2\bar{h}}{\partial\bar{x}^2}\right)\right]=0\,. \tag{21}$$

The Fortran solver PDE_1D_MG can be used to solve for $\bar{h}$.

Experimental and theoretical time dependence of trench evolution in TcEP

The time dependence of trench evolution was studied for a small area (3×3 μm) within an array of SWNTs by collecting a sequence of AFM images (~30 s), for different durations of applied bias (V_{DS}=0.66 V/μm, L= 30 μm, 30 ˚C background heating) . During imaging no bias was applied, thereby leaving the trenches in fixed geometries for the duration of the measurement. In between images, biases were applied, driving trench formation for controlled durations (durations varied depending on accumulated duration ranging from 0.1 s for very short accumulated duration, <10 s, to 30 min for very long accumulated duration, 6-8 hrs). The total time of trench formation was taken to be the sum of the durations for all preceding experiments. Figure S7 shows representative images at various points in the evolution of trenches (Fig. 3c shows cropped images associated with the second trench from the left). Supplemental movie 1 is based on 3D rendering of representative AFM data with speeds that accelerate throughout the movie (indicated by time bar) to match the rate at which features evolve. At relatively short durations, trenches were shallow (< 1 nm deep) and characterized by slight ridges in the Tc-resist on each side of the SWNT, over time evolving into fully formed trenches, which grow and eventually (hours) began to interact with trenches from adjacent SWNTs, limiting further growth. Data associated with analysis of time dependence was restricted to durations where trenches were isolated from one another (<2 hr). For the purposes of establishing reliable measures of trench evolution, the trench width, W_{Tc}, was defined as the width between the peak of the pile-up on either side of the trench (actual minimum widths, evaluated at the base of the Tc-resist, were much narrower). Analysis to determine the left and right side of the trench was performed in MATLAB, and involved identifying the first location to the left and right side of the trench where the slope fell below a certain threshold, 5×10^{-11}. Figure S8a shows an AFM image for

t=600 s with the identified left and right sides of the trench highlighted for the three central trenches. Figure S8b shows cross-sectional profiles associated with the central trench at various points in the trench evolution and the identified left and right positions. Figures 3f and S9a show the resulting experimentally extracted W_{Tc}. Smaller trenches (W_{Tc}<150 nm, associated with t<10 min), were less distinct, and identifying the left and right positions was more difficult. While values of W_{Tc} were roughly accurate, there was significantly more error at shorter times than longer times. The short time values were not used for power law fitting (Fig S9a). Power law fitting was performed in data ranges where the standard deviation was <10% of W_{Tc}. (For data outside of this range, standard deviation was W_{Tc} ~20-50% of W_{Tc}). The data fit well to a power law with exponent 0.25 (The value for the constant of proportionality, A, are shown). Figure S9b shows the predicted W_{Tc} based on modeled trench profiles (peaks in $\bar{h}(\bar{x},\bar{t})$), which also fit well to a power law with exponent of 0.25 (The parameter A depends on various Tc-resist properties, several of which are unknown). Figures S9c,d show the predicted W_{Tc} for power densities varying from 8.3-33.3 μW/μm for long durations and for durations that yield trench widths associated with those typical for TcEP. (Comparison to model can be difficult given the uncertainty in materials properties for the Tc-resist. Because $\bar{t}$ is normalized with respect to μ and γ, which are unknown, it is not possible to compare directly to t. Nevertheless, the computed W_{Tc} is only normalized by h_0, so it is meaningful to compare modeled $\bar{t}$ to ranges of experimental t that yield trenches of similar size to those measured experimentally). For long times, W_{Tc} varies with power density. At durations associated with experimental conditions, however, almost no variation is predicted. This relative insensitivity to power is consistent with experimental observation (Fig. 2e,f), where only~20% variations in W_{Tc} are typically observed. Such variations likely result from local changes in film viscosity associated with heating, or

other effects not explicitly included in the model. In addition, besides capturing the underlying physics, these models also establish a set of guidelines for the selection of optimal materials for Tc-resists, i.e. large temperature coefficients of surface tension and low viscosities yield narrow trenches within reasonable experimental times. Furthermore, decreasing the thickness reduces the trench widths. Empirical studies of various materials for Tc-resists (see Supplementary Information, Fig. S12) led to the selection of the molecular glass reported here.

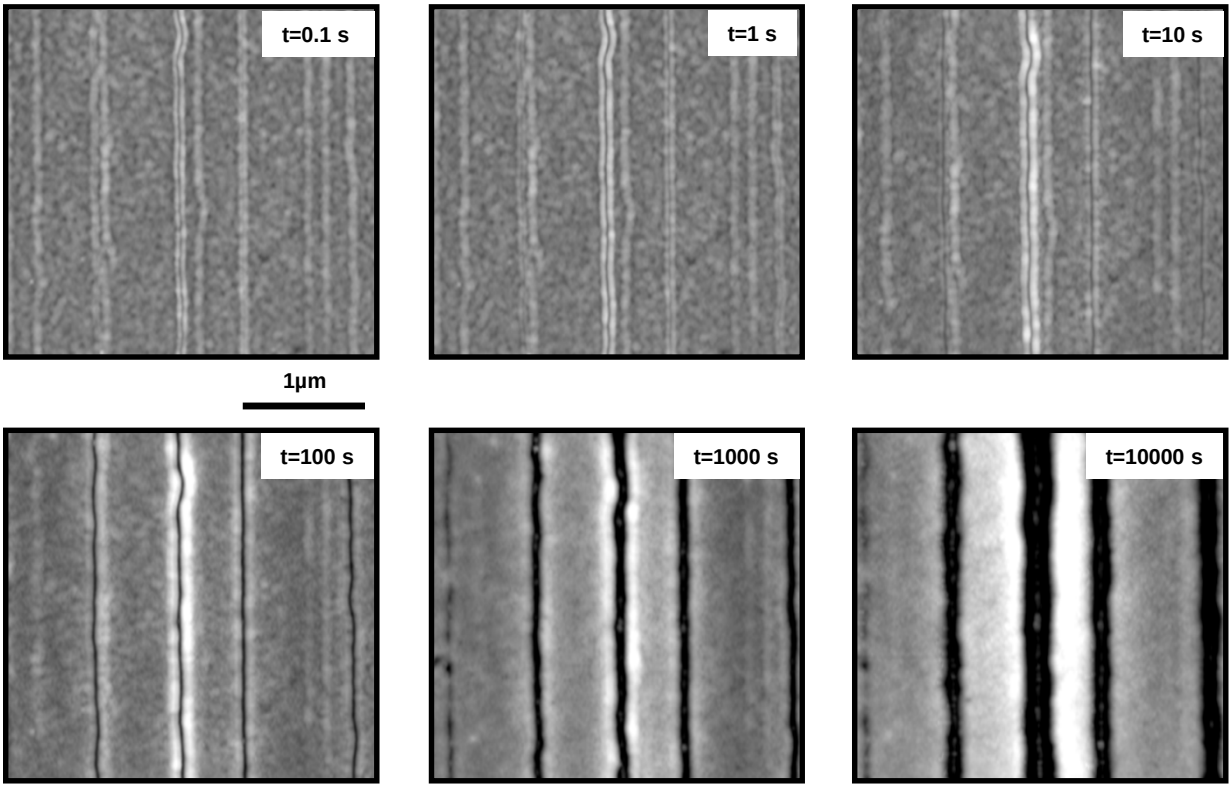

Figure S7. Time dependent trench formation study. 3×3 μm AFM images associated with in-situ measurement of trench formation. Brief intervals of bias were applied and the associated topography was measured (30 s scans) in between each interval. These images are associated with various total accumulated bias durations as trenches evolve.

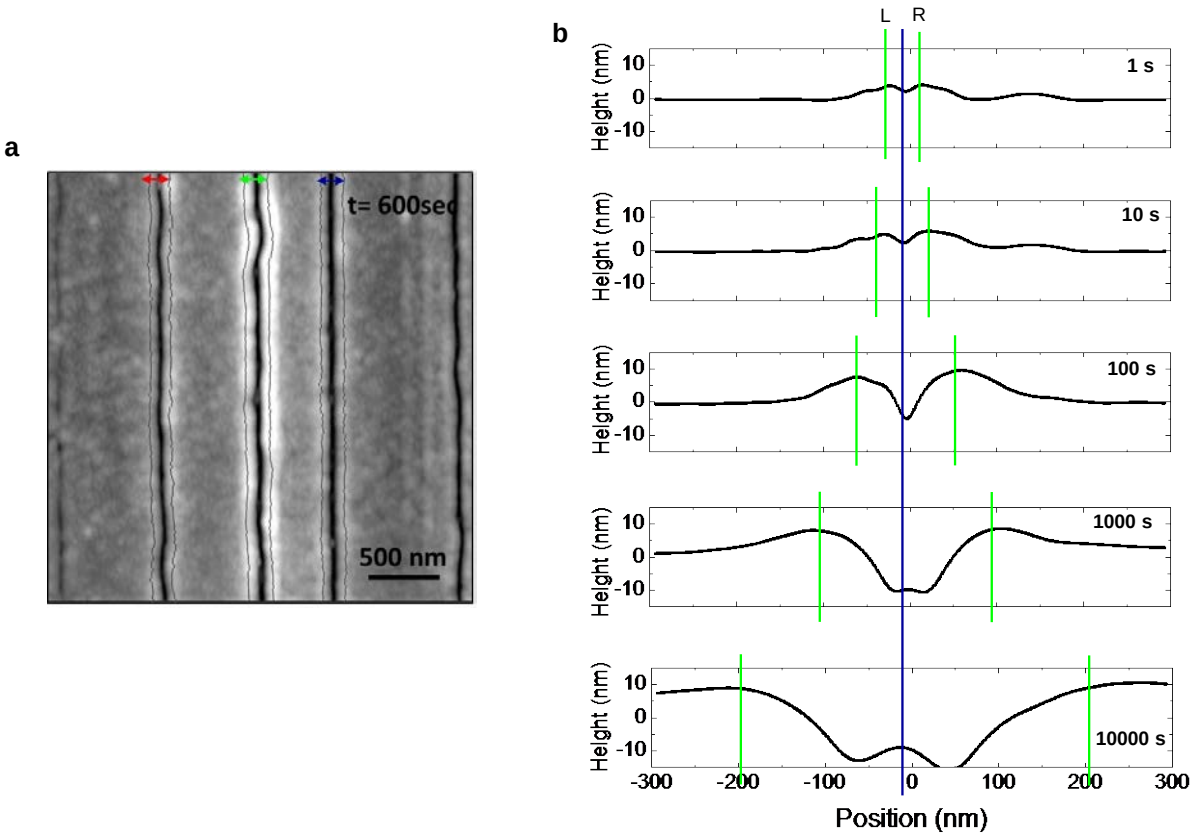

Figure S8. Details of trench width identification. (a) Representative image of trench formation. Lines showing the position identified as the right and left trench edge. (b) Representative cross-sectional height profiles at various points in trench evolution. For the purposes of establishing reliable methods of consistently identifying trench width that are independent of AFM tip condition and can yield comparison to features easily identified by thermocapillary flow modeling, the trench edges were associated with the peaks of the pileup on the trench edge. As is evident from the cross-section profiles, that width of the trench at the base is substantially narrower than these values. AFM tip artifacts make precise measurement of this inner width difficult.

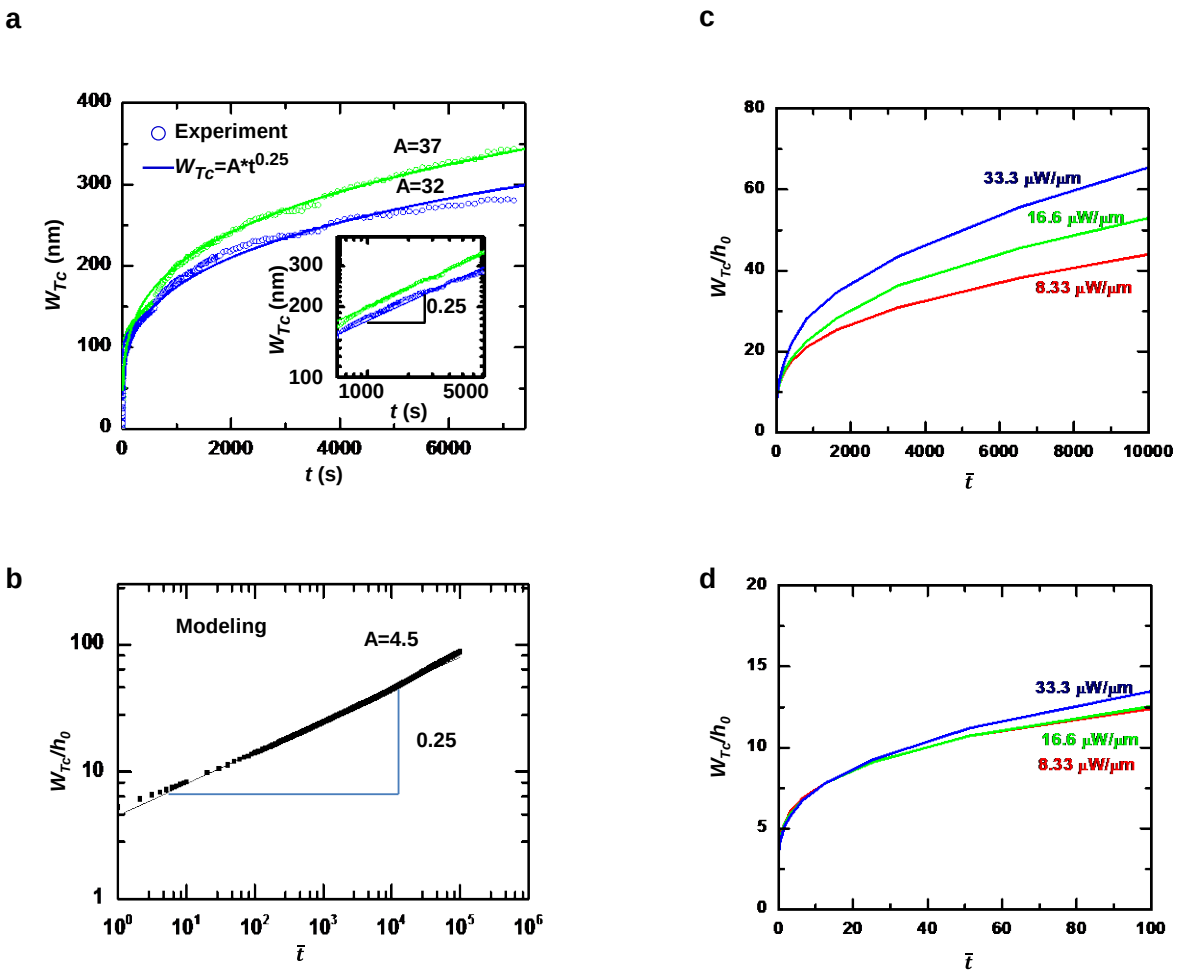

Figure S9. Time dependence of trench width. (a) Experimental results showing power law time dependence, with $t^{0.25}$ scaling, for th width. Trenches associated with different SWNTs have slightly different prefactors, most likely associated with slight differences in relative power densities. (b) Modeling showing similar $t^{0.25}$ dependence, thus indicating that the model for Tc-flow accurately captures the fundamental scaling of trench formation. (c,d) Time dependence of width for various powers over long and short time scales respectively. For short time scales, where trench widths are comparable to those in TcEP, the width only depends weakly on the power.

Thermocapillary flows in Tc-resist, studied by heated AFM tips with integrated temperature sensors

Heated atomic force microscope (AFM) tips with known temperatures contacted with the Tc-resist layer for various times, and with various applied powers, allow study of the effects of thermocapillary flow in a nanoscale system where temperature and other parameters are controlled (and known) more accurately than the case for SWNTs. The heated tip (radius <100 nm) was fabricated from doped single crystal silicon, and is capable of reaching temperatures of 1000 °C with a temperature calibration to within 5 °C for this entire range.[18] Previous studies of viscous mass flow from a heated tip to a substrate revealed thermocapillarity to be an important driver of flow[19]. Figure S10 shows Tc-resist layer deformation induced by tip heating for tip-substrate temperature differences between 5 – 45 °C and dwell times between 0.1 – 300 s on both an unheated Tc-resist layer and a Tc-resist layer heated to 50 °C. The tip dwelled on the surface with tip forces below 20 nN and did not deform the surface when unheated. The results show that significant material flows radially away from the heated tip for Tc-resist layer temperatures far below the sublimation temperature, consistent with thermocapillary stresses induced by the temperature gradient around the tip.

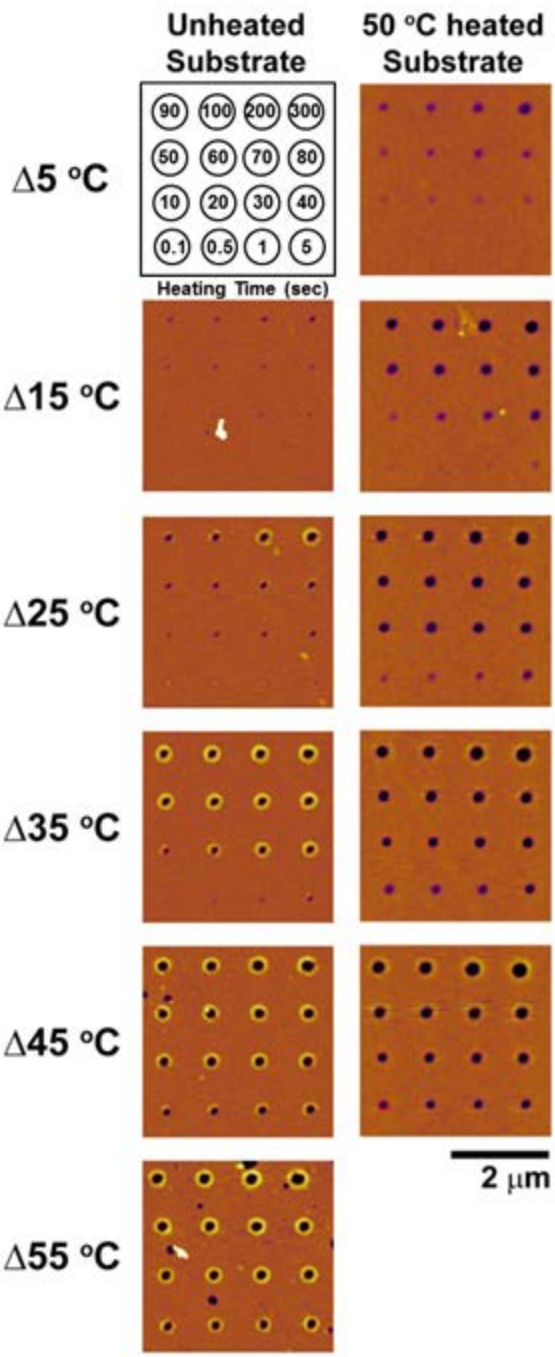

Figure S10. Thermocapillary flows in Tc-resist studied with calibrated, heated AFM tips. AFM images of a series of arrays of dots patterned in films of Tc-resist, created by contact of heated AFM tips for a variety of temperature differences (tip to substrate) and contact durations (indicated in first frame) at both room temperature and 60 ˚C. General behavior is consistent with that observed for SWNT Joule heating. In particular, features form in the Tc-resist even at low temperature rises. Feature sizes increase with time.

Pulsed heating in TcEP for large scale arrays of SWNTs

For arrays that contain large numbers of SWNTs (either at high densities or over large areas) the coupled heating of many SWNT leads to bulk, and sometimes large, increases in temperature. These effects can yield thermocapillary flow on larger length scales and in ways that are difficult to confine to the positions of the SWNTs (Fig. S11). Pulsed bias conditions (~1-10 μs) can avoid these cumulative effects, to yield localized heating and thereby preserve well-behaved trenches even with large arrays of SWNTs and/or relatively high densities (up to 3 SWNT/μm studied here). Figure S11, shows the resulting trenches for a localized region within a large area high density array (30 μm × 1 mm, 2-3 SWNT/μm) for increasing duty cycles (10 to 100%) with a fixed pulse duration (10 μs). These data clearly show the gradual transition from narrow, well defined trenches associated with individual SWNTs to uncontrolled flow not correlated to SWNTs. For optimized application of pulsed TcEP (large area, high density arrays), 1-3 μs pulses (40V) were applied with 10 μs pulse periods.

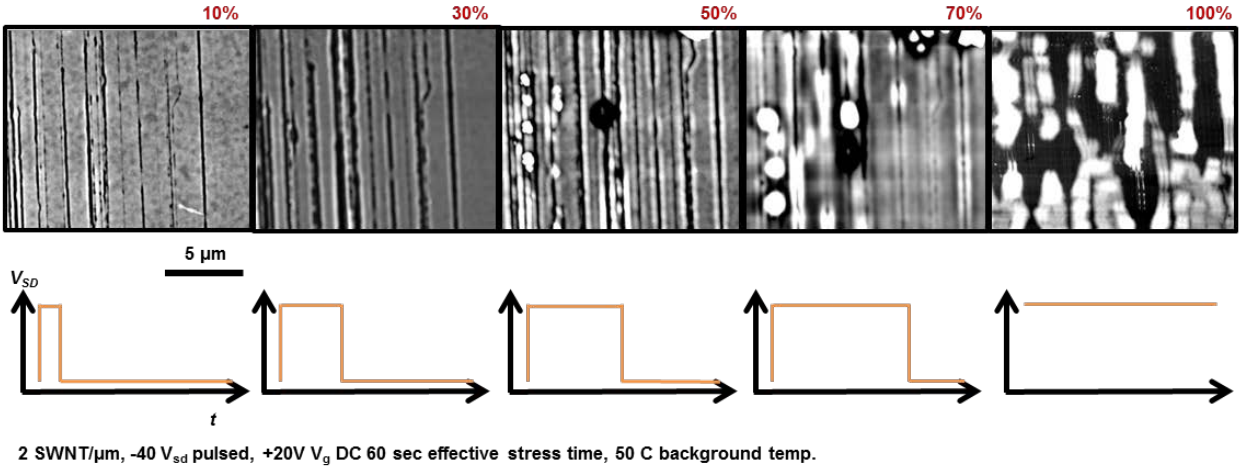

Figure S11. Pulsed biases for forming trenches in large and/or high density arrays of SWNTs. AFM trenches formed in Tc-resist for an array with 2-3 SWNT/μm associated with pulsed heating with increasing duty cycle (V_{DS}= -40V peak amplitude, period= 10 μs, duration= 1-10 μs, V_{GS}= +20V DC, 60 sec total stress duration, 50 ˚C background heating). For 10% duty cycle clearly defined trenches are observed. As the duty cycle increases, trenches become less clearly defined and flow is observed that does not correlate to the underlying SWNT positions. This result from delocalized heating associated with parallel operation in many SWNT. Pulsed heating aids in localizing the flows needed for proper operation in TcEP.

Tc-resist material selection

There are numerous characteristics that are critical for an effective Tc-resist material. Basic requirements are that the material can be easily deposited in thin film configurations, where vacuum deposition is preferable to spin coating, since it easily yields uniform film thickness even in regions near the partial gate electrode structures, where substrate topography is highly nonuniform. The films must afford good coverage and adhesion to both the SWNT and the quartz substrate, and at the same time be sufficiently impermeable to O_2/CF_4 plasma to act as an effective etch resist. The unique chemistry of the Tc-resist material studied here combines hydroxyl and phenyl moieties which provide compatibility with both SWNT and oxide substrates. It is critical for films to exist in an amorphous phase, to avoid spatial nonuniformities in thermal properties (thermal conductivity, k), viscous flow properties (temperature coefficient of surface tension, γ_1, and viscosity, μ) and thickness that can be associated with crystalline grains. Figure S12a,b,c shows AFM associated with trench formation experiments with arrays of SWNTs and Tc-resists consisting of thin films of paraffin, TCNQ, and pentacene (similar results were achieved for TCTA and F4-TCNQ). All of these materials show features that roughly correlate to underlying SWNT heaters, but showed massive variations in resulting trenches over the area of the film. Films of TAZ and anthracene (deposited at -80 ˚C) yielded amorphous films, but, over the time scales associated with experiments and characterization, exhibited spontaneous crystallization. Other materials, such as polystyrene (M_W=288,000, Fig. S12d) or Alq3 provided high quality amorphous films, but significantly higher power densities (and/or higher background heating, T_∞ >140 ˚C) were required to yield trenches. (In the case of Alq3, crystallization occurred at lower temperatures than those required for trenches to be observed, in reasonable experimental time scales). These power densities (or background heating) lead to

bias requirements and/or operating conditions in which non-ideal device behaviors (e.g. non-negligible current through the s-SWNTs) limit the selectivity of the TcEP process. Models of thermocapillary flow suggest that such behaviors are due to either low temperature coefficients of surface tension or high viscosities. While both parameters play an important role in the flow (and γ_1 also plays a role in the trench profile), most materials exhibit γ_1 between ~0.05 and ~0.15 $mJ/m^2/^{\circ}C$, while viscosities can vary by many orders of magnitude. It is likely, then, that viscosity is the most significant parameter that determines whether materials yield trenches in experimentally practical time scales and with low power levels, without significant background heating. While the Tc-resist demonstrated here meets all of these criteria, advances could be obtained through the development of materials with similar properties but also with the ability for use at smaller thicknesses (e.g. 5-10 nm, rather than 25 nm). Reductions in thickness enable decreases in W_{Tc} (linearly with h_f) which, in turn, could allow application to arrays of SWNTs with high densities.

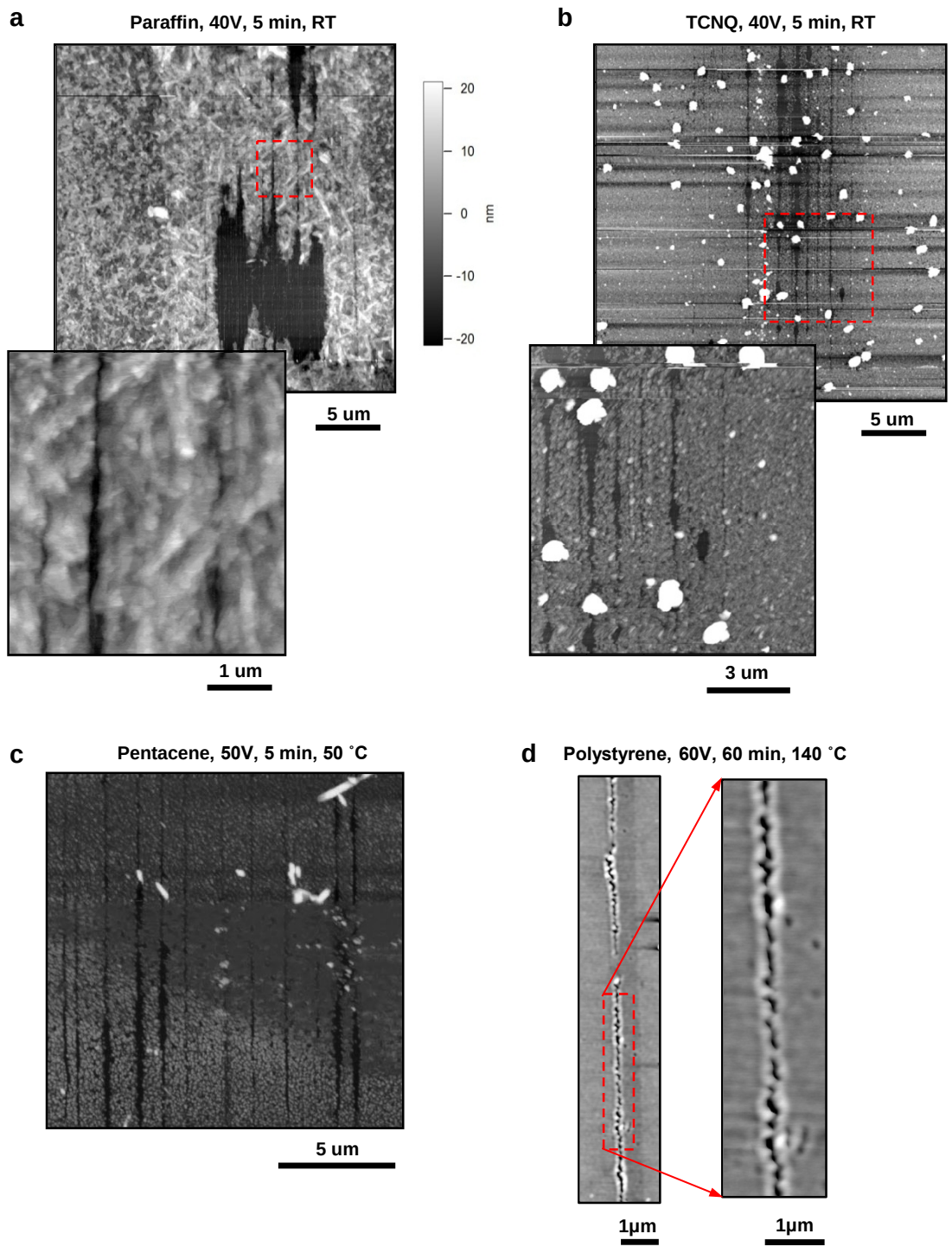

Figure S12. Behaviors in other candidate materials for Tc-resists. AFM images of trenches formed for (a) paraffin, (b) TCNQ, and (c) pentacene. Some trenches are observed, but with non-uniform widths. For these materials, such behaviors can be attributed to their morphology. Other materials explored, such as polystyrene (d) failed as Tc-resists due to inability to form trenches at sufficiently low powers (likely due to high viscosity or low temperature coefficient of surface tension) and/or insufficient etch resistance.

Processes defined by critical temperatures

The unique scaling (particularly power invariance) associated with thermocapillary flow is critical to the success of TcEP, because it allows uniform trenches in arrays of SWNT that incorporate significant variations in power densities among the various SWNTs. Although it is possible to envision approaches like TcEP but which rely on processes such as sublimation or ablation, their robust operation is limited by the existence of a critical temperature, T_C. In such cases, at temperatures below T_C, the resist will remain, while at temperatures above T_C, the film will be removed. Thermal models can provide key insights into the scaling of this type of process. Figure S13a,b show temperature profiles and thermal gradients for a range of power densities similar to those measured experimentally. Both peak power and peak gradient scale linearly with power. A width associated with a process that relies on a critical temperature, W_C, can be determined (Fig. S13a). Figures 13c,d show the predicted scaling for processes associated with critical temperatures of 2-10 ˚C. It reveals that these processes yield no trench until a certain power density is reached. Afterward, the width increases dramatically with increasing power, to widths that would expose other SWNT in arrays of densities >0.1 SWNT/μm. This type of scaling is incompatible with desired operation. For higher T_C the range of powers that yield practical trench widths (several hundred nm) becomes larger. Here, the required power density to initiate trenches grows dramatically, which is also highly undesirable.

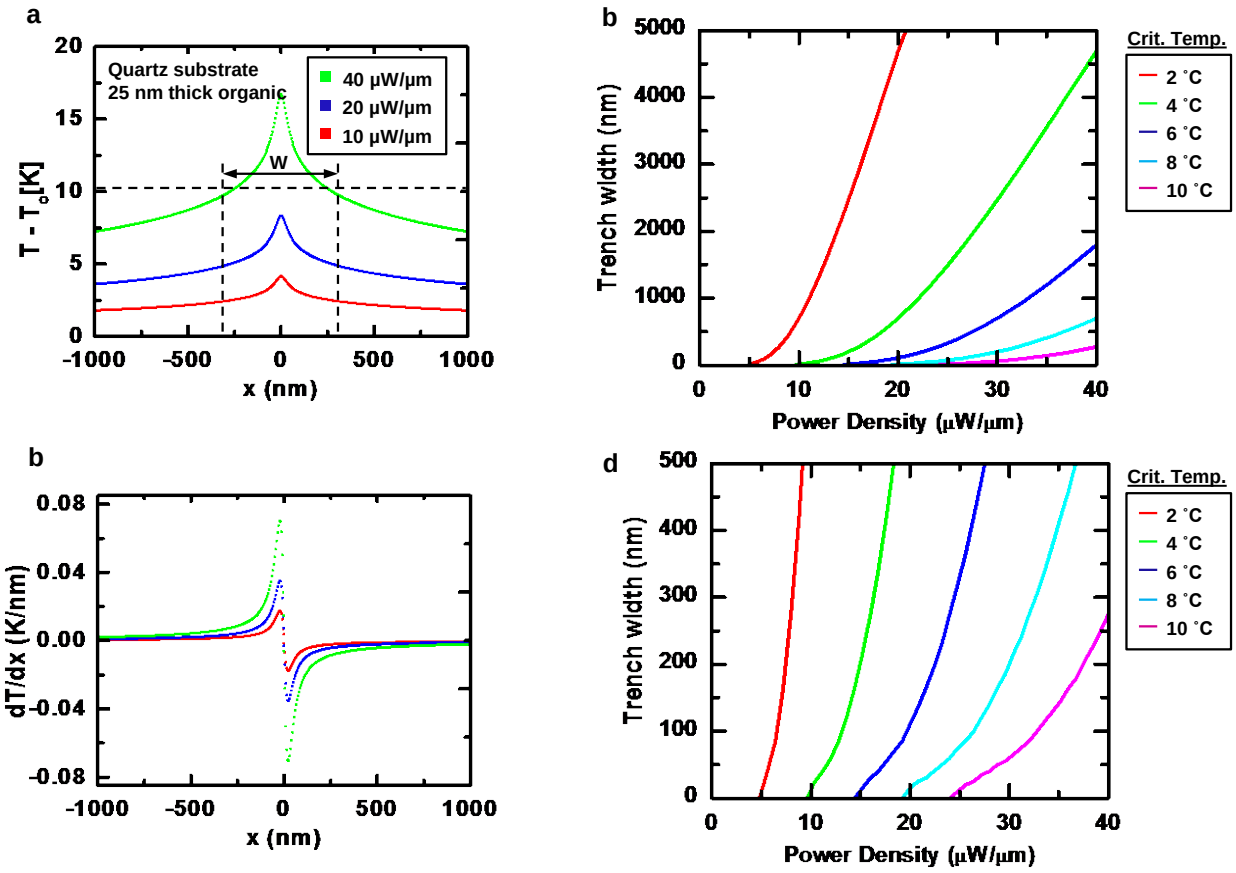

Figure S13. Theoretical trench width for processes based on critical temperatures. (a,b) Temperature profiles and gradients predicted by analytical thermal models for a variety of powers. Processes such as sublimation or ablation have a critical temperature associated with them such that all material at or above this temperature is removed and all below the critical temperature is preserved. (c,d) Power dependence of predicted trench width associated with processes with critical temperatures ranging from 2-10 ˚C. Processes with higher critical temperature should show similar scaling but with higher power density required to yield trenches (unsuitable for TcEP). This type of scaling is not ideal for TcEP, since at conditions sufficient to yield trenches in the least conductive m-SWNT, the most conductive SWNTs would exhibit very wide trenches (several μm), thereby exposing neighboring SWNTs.

Effects of trench formation in neighboring SWNTs

For very high SWNT densities, non-ideal behavior in TcEP can occur if a trench associated with an m-SWNT exposes an s-SWNT in close proximity. The trench width provides an indicator for the density at which this type of behavior can be expected. In particular, for an array of SWNTs with regular spacing, the maximum density is defined roughly by the average trench width (trench width measured at the base of the Tc-resist ~100 nm, where W_{Tc} is ~250 nm). We note, however, that thermocapillary flow can be altered as neighboring trenches approach one another. Certain effects can be seen in supplemental movie 1: At long times the pileup from two adjacent trenches coalesces, creating a narrow strip of Tc-resist in between them. It is unclear from the simple models here, which apply to isolated SWNT, how close the SWNTs can be before their trenches merge. As a result, the minimum spacing between trenches where Tc-resist remains in between them provides the best indicator of the maximum density that can be accommodated in TcEP, as implemented here. AFM measurements of trench formation in arrays with locally high densities suggest that neighboring trenches can be as close as 250 nm while still showing well-defined Tc-resist in between. Figure S14 shows an AFM, cross-sectional height profile, and associated 3D renderings of such trenches. Here, isolated trenches are observed along the entire lengths of the trenches (~8 μm).

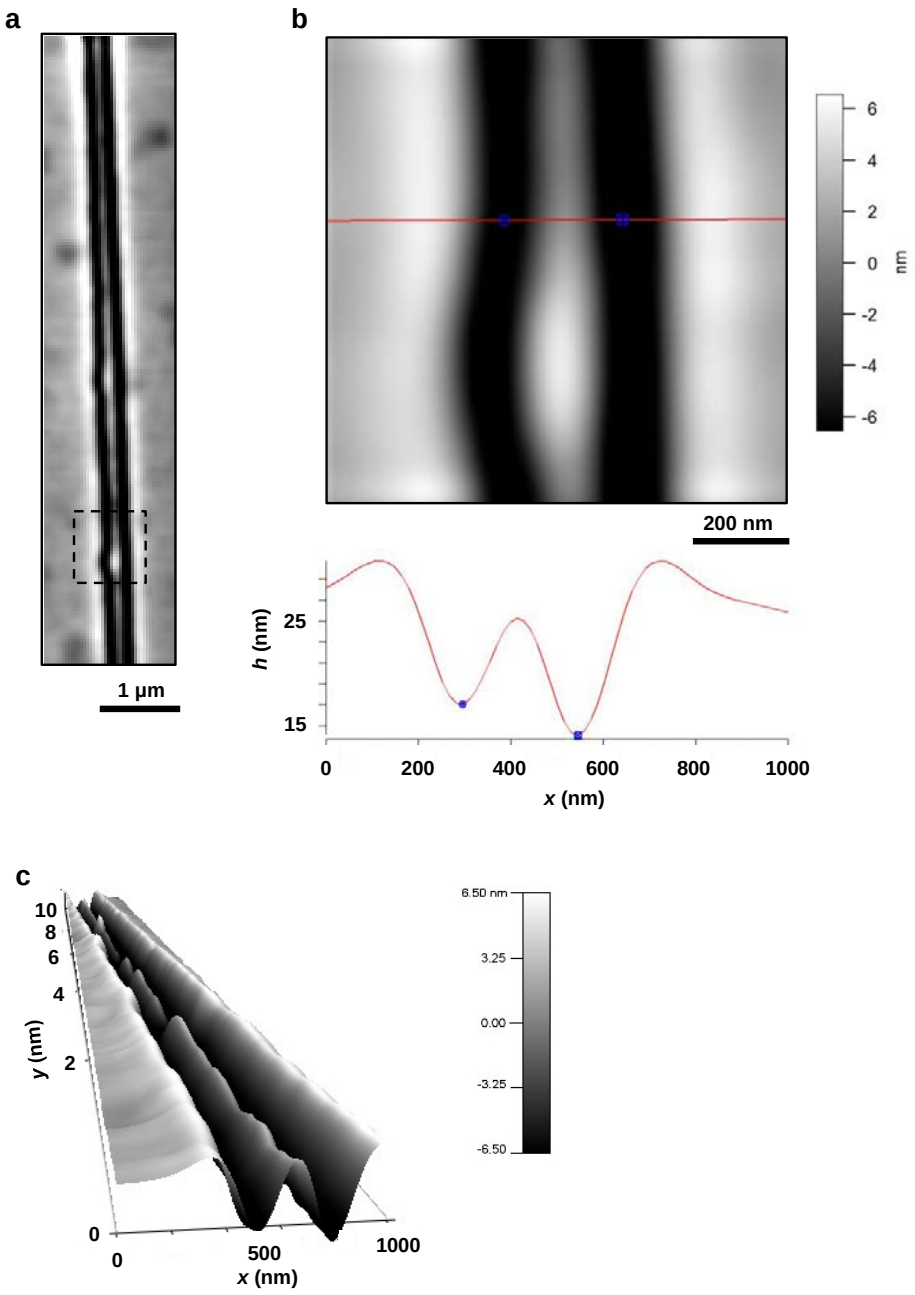

Figure S14. Trenches in cases with neighboring SWNTs. AFM images associated with two distinct trenches that form from heating in neighboring SWNTs. Despite their close proximity (250 nm) two distinct trenches form along the lengths of the SWNTs (~10 µm).

Interconnected arrays of SWNT for large area TcEP

For applications where the collections of devices in a target application are known roughly, then it is practical to perform TcEP in local patches, as part of an interconnected array of electrodes. Figure S15a shows five 1×5 sets of SWNT processed by TcEP in this manner. Figure S15b,c show the transfer characteristics for one of the arrays before and after TcEP and the characteristics for all five devices after TcEP. Table S2 summarizes the results for all five arrays. For each array, after removing interconnects (lithography and etching), all of the devices (25 total) showed high on/off ratio ($> 1 \times 10^3$). This result demonstrates the effectiveness of performing TcEP over large areas using this type of interconnection scheme.

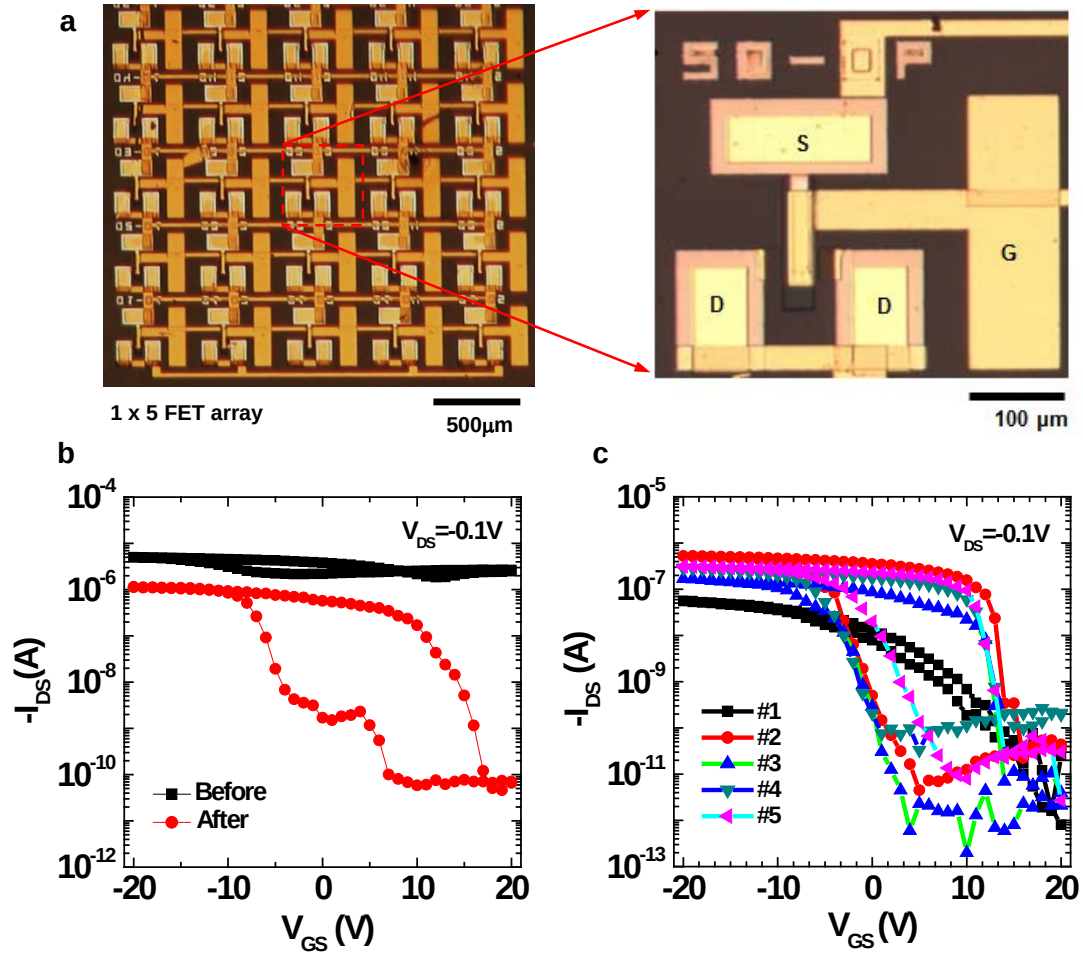

Figure S15. Details of TcEP in a parallel operational mode. (a) Optical images for a 1×5 array of SWNT arrays and associated electrodes for TcEP, with electrodes connected in parallel (b) transfer characteristics before and after TcEP in parallel and (c) transfer characteristics for disconnected individual arrays following TcEP. All arrays show high on/off ratio following TcEP.

Table S2. Summary of conductance of 1×5 arrays of devices before and after TcEP.

Array #	$I_{on,\ b}$ (A)	$I_{on,\ a}$ (A)	I_{on}/I_{off} ratio	$I_{on,\ a}/I_{on,\ b}$ (%)
#1	4.50E-06	1.02E-06	1.06E+03	22.6
#2	5.28E-06	1.03E-06	6.60E+03	19.5
#3	4.99E-06	1.13E-06	2.46E+04	22.7
#4	7.18E-06	1.21E-06	9.26E+03	16.9
#5	1.20E-05	1.16E-06	4.38E+03	9.7
AVG	6.80E-06	1.11E-06	9.18E+03	18.3

Inverter fabrication and load line analysis

A p-type inverter was fabricated from two devices based on arrays treated by TcEP. Figure S16a shows optical micrographs associated with this process. Here, a common source electrode is used to perform TcEP on two arrays with interconnected drain electrodes. Following TcEP, the gate and dielectric layers were removed. For one transistor (the load TFT), the associated source and drain electrodes for TcEP served as electrodes for the final device. For the other (the driver TFT) the source electrode was extended to yield a reduced channel length (~3.5 μm). Finally, new dielectric (SOG/HfO_2, 35/20 nm) and top gate (Ti, 70 nm) structures were defined, to complete the fabrication. The current level for the driver TFT increased roughly linearly with the reduction in channel length from 30 μm to 3.5 μm (expected ratio~8.5, measured ratio~9.5). This yielded for a current ratio between driver and load TFTs of ~10. Figure S16b,c shows the electrical properties of the driver and load TFTs. The measured voltage transfer curve (VTC) is consistent with that predicted from load line analysis (Fig. S17). Some variation between the measured and predicted VTC curves results from hysteresis in the load and driver TFTs. The measured voltage gain (~4) is near expectation based on conventional diode-load inverter circuit design equation (~3, $A_V=g_m/g_{m\_load}=(L_{load}/L_{driver})^{0.5}$)[20].

In addition, this demonstration hints that TcEP scheme can be important for short channel devices and their circuit demonstrations. In particular short channel devices, such as the one shown in Fig. 6c, would difficult or impossible to fabricate reliably using a traditional method to eliminate the role of m-SWNTs, such as electrical breakdown, for two reasons: (1) heat sinking at the electrode contacts[29] progressively drive required powers to levels that reduce selectivity and lead to biases that can cause electrical breakdown in the necessarily thin gate dielectrics and (2) arrays of SWNT processed by breakdown in large device geometries lead to small

discontinuities[34] in the m-SWNTs at positions that cannot be aligned, in determinate fashion, with the channels of subsequently fabricated devices.

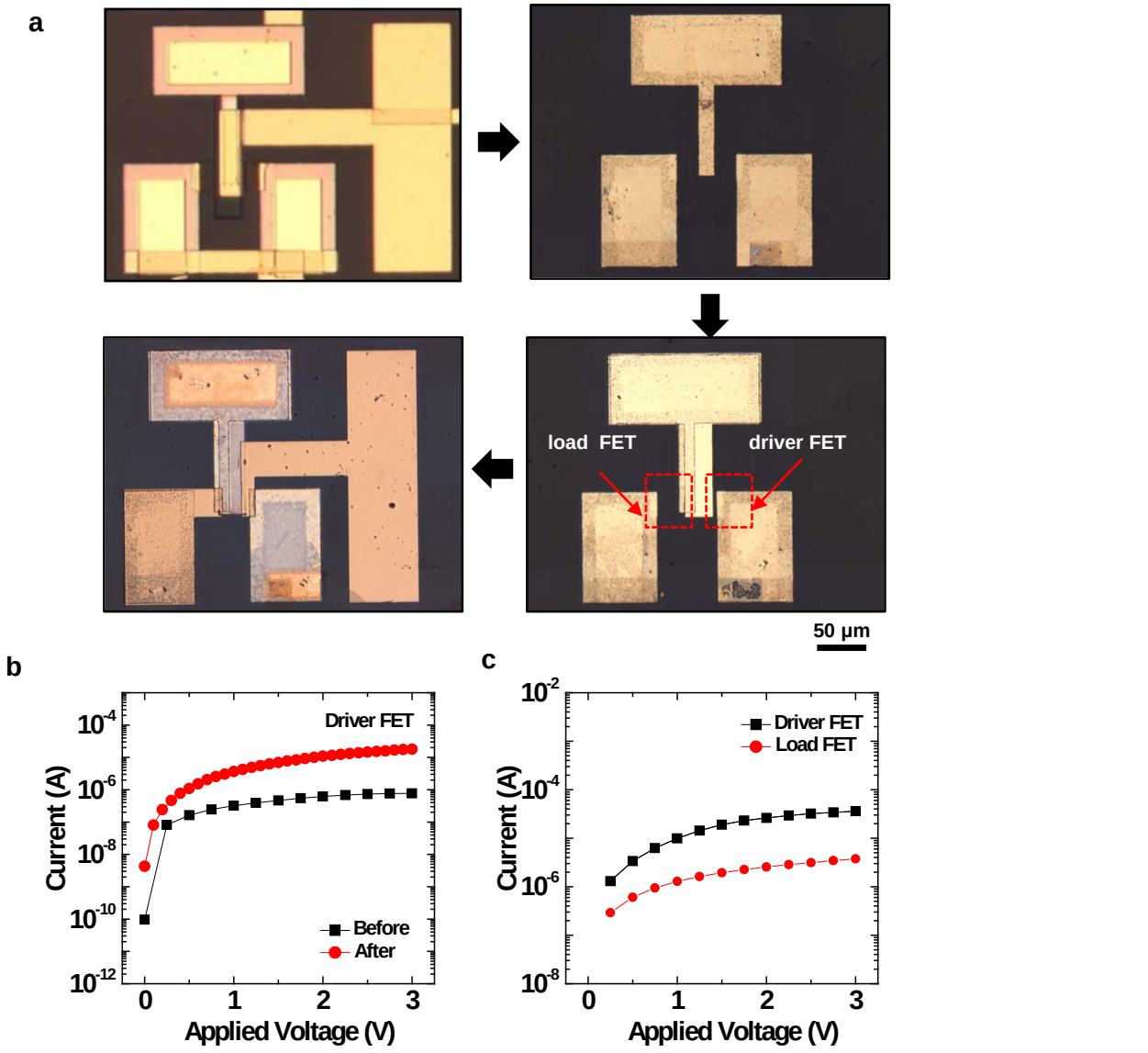

Figure S16. Details of inverter fabrication (a) Optical micrographs corresponding to process steps for inverter fabrication. TcEP was performed on two arrays in parallel, the gate electrode and dielectric layers were removed, and then new, top-gated TFTs were fabricated with appropriate channel lengths for optimal inverter performance. (b) I-V characteristics of driver FETs associated with electrodes used for TcEP (30 μm channel length) and final device configuration (3.5 μm channel length), respectively. (c) I-V characteristics of driver and load TFTs following inverter fabrication.

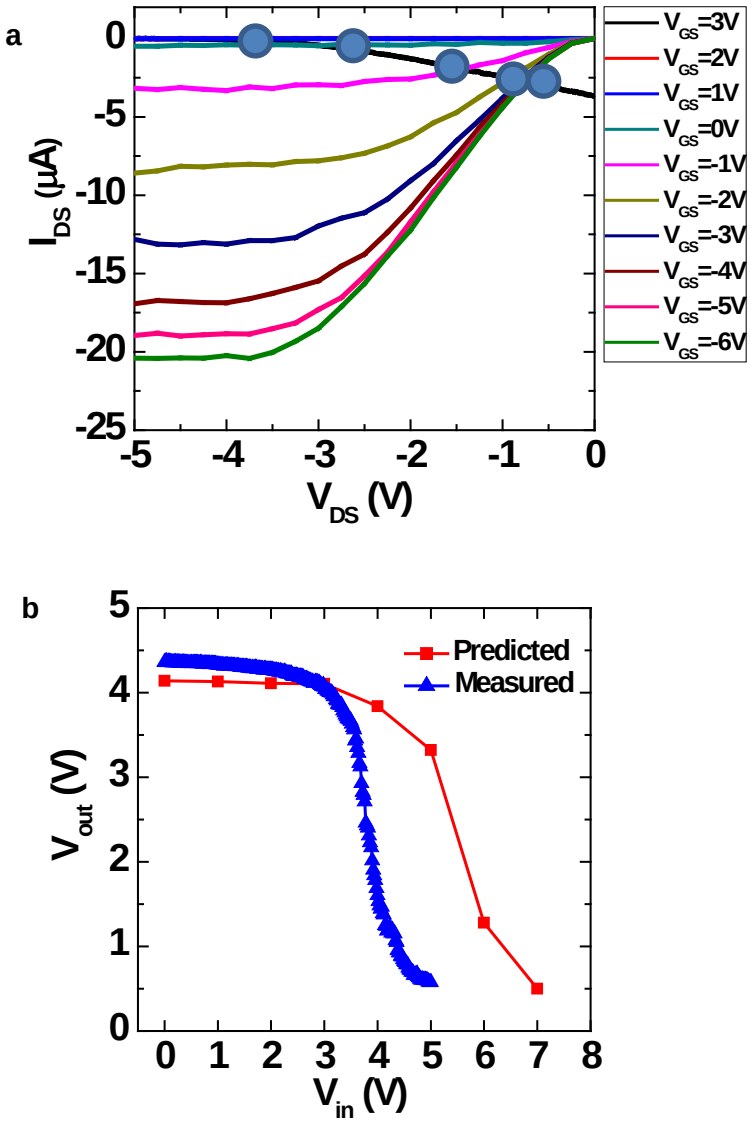

Figure S17. Inverter fabricated using arrays processed by TcEP. (a) load line analysis for the inverter and (b) voltage transfer characteristics measured and predicted from load line analysis

Modeling of Electrical Properties of SWNTs in partial gate configurations, after TcEP

To determine the mobility of s-SWNTs following TcEP, the transfer characteristics from the devices comprising ~200 s-SWNTs with similar operating voltages were averaged and used as the basis of fitting to simulation results. In particular, self-consistent solutions to the Poisson and drift-diffusion equations[21] were used to simulate a partial gate SWNT field effect transistors (PG-FET) with 1nm diameter (average diameter expected for populations grown by this technique[2]) s-SWNT as channel. Dimensions and other parameters are based on experiments and shown in Figure S18a. Solution of the three-dimensional Poisson equation captures the effect of contact dimensions on the electrostatics of PG-FETs; whereas solution of the drift-diffusion equation describes one-dimensional carrier transport along the s-SWNT. In addition to using analytical expressions for mobility and carrier densities, simulation also considers acceptor doping to capture the influence of (oxygen and water induced) negatively charged interface defects.

Figure S18b shows measured and simulated drain to source current (I_{DS}) vs. gate voltage (V_G) characteristics of the PG-FET at different source-drain bias (V_{DS}) for the averaged s-SWNT response. The simulation shows good agreement with the values measured under similar bias conditions. (Measured values represent average characteristics for ~30 PG-FETs with ~ 200 s-SWNTs). As shown in Fig. S18c, the percentage difference between experiment and simulation, defined as $(I_{DS\_exp} - I_{DS\_sim})/I_{DS\_exp} \times 100$ % from V_{GS} ~ 0 V (i.e., the voltage where transconductance, $g_m = dI_{DS}/dV_{GS}$, is maximum) to V_{GS} = -20 V, is within ± 5-7%. The variation reflects the uncertainty of device parameters used in the simulation. The average mobility throughout the devices, averaged over the quasi-Fermi level variation[22], i.e.,

$$\mu_{avg}\left(V_{DS},V_{GS}\right)=\frac{\int_0^L \mu(x)\left|\frac{dQ_{Fp}}{dx}\right|dx}{\int_0^L \left|\frac{dQ_{Fp}}{dx}\right|dx} \tag{22}$$

is summarized in Fig. S18d. We find that, μ_{avg} ~ 960-1050 cm^2/V-sec. Variation of mobility with V_{GS} and V_{DS} follows the classical trend, *i.e.*, decreases with both higher $|V_{GS}|$[22, 23] and higher $|V_{DS}|$ [22]. Such reduction of mobility at higher V_{GS} is routinely observed in s-SWNT's mobility measurements[23, 24] and is related to the increase of average electric field along the SWNT (considered in simulation) and also to the non-parabolicity in SWNTs' band-structure[25] (ignored in simulation). The effect of contact resistance (~ 28 kΩ) is observed to have negligible effect in extracted mobility for these long-channel length PG-FETs.

In addition, the average mobility (Eq. (22)) was extracted based on the following mobility equation (Eq. (23)). Mobility at position *x, μ(x),* along the nanotube is calculated using[22, 23, 25]

$$\mu(x)=\frac{\mu_{peak}}{1+\mu_{peak}\left|\frac{dQ_{Fp}}{dx}\right|\Big/ v_s} \tag{23}$$

where μ_{peak} is the peak mobility, V is the potential at x, v_s is the saturation velocity. This position dependent mobility (Eq. (23)) is later used for calculating average mobility (μ_{avg}) at a particular V_{GS}, V_{DS} using Eq. (22).

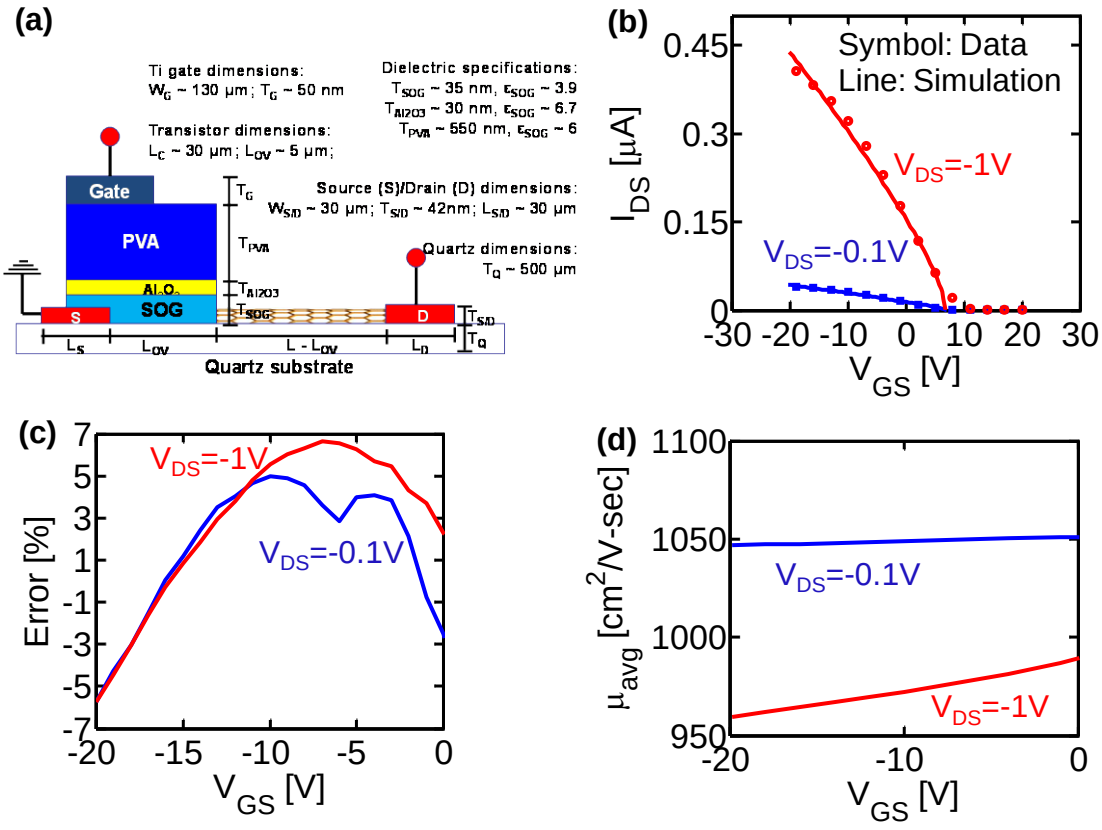

Figure S18. Modeling results used to extract mobilities from device characteristics. (a) Cross-sectional schematic illustration of a partial gate device consisting of source/drain (Ti/Pd), gate (Ti), and a gate dielectric of PVA/Al_2O_3/Spin-on-glass (SOG). Values for the width (W), length (L) and thickness (T) of different components of the device are also specified. (b) Measured drain to source current (I_{DS}) vs gate to source bias (V_{GS}) averaged over ~ 35 such devices having 200 semiconducting SWNTs (s-SWNTs) at two different drain to source bias (V_{DS}). Simulation of the device characteristics by considering the dimensions specified in (a) and using ~1 nm diameter (average value for these nanotubes[26]) s-SWNTs. The results match the measured data. (c) Calculated percentage difference between modeling results and data as a function of V_{GS} shows ±5-7 % uncertainty in mobility extraction. (d) The simulation yields an average mobility of ~ 960-1050 cm^2/V-sec at different bias conditions.

SEM and AFM images at each stage of the TcEP process, as implemented with a back split gate structure (BSGS)

As a simplified version of TcEP, we demonstrated the feasibility of a re-usable electrode/gate structure, to eliminate cycles of processing that would otherwise be necessary for repetitive fabrication of top split gate structures used in the original scheme.

Fig. S19a shows an AFM image of the channel region of the BSGS (bottom split gate structure) immediately after transfer of an array of SWNTs. The AFM image in Fig. S19b shows selective formation of trenches for the entire channel length of 30 μm, by thermocapillary flow in an overlying layer of Tc-resist. The bias conditions to initiate this flow were similar to those for the corresponding top gate geometry, i.e, V_{DS}=-40V, V_{GS}=20V for 5 min at 60^{o}C in vacuum (1×10^{-4} torr). After dry etching to remove m-SWNTs, the Tc-resist is removed with acetone. The resulting channel appears in Fig. S19c. The red arrow highlights a pair of s-SWNTs throughout this process. This BSGS has W/L=30/30 μm.

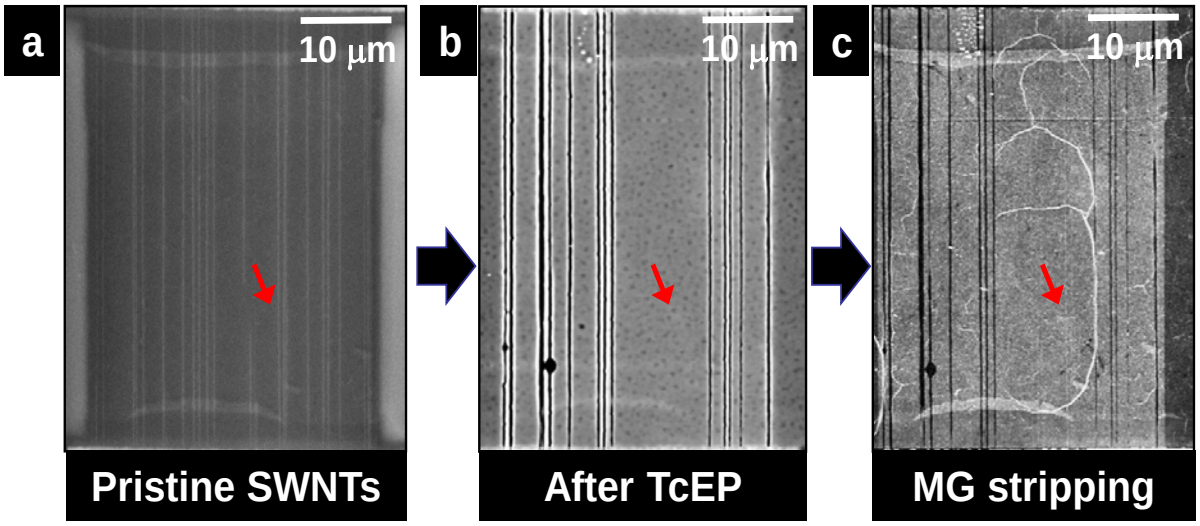

Figure S19 SEM and AFM images at each stage of the TcEP process, as implemented with a BSGS. (a) SEM image of an as-grown array of SWNTs after transfer onto the BSGS (source and drain electrodes out of the field of view, top and bottom) (b) AFM image after selective trench formation by thermocapillary flow, (c) AFM image after RIE etching and stripping of the Tc resist. The red arrow highlights a pair of s-SWNTs throughout this process. This BSGS has W/L=30/30 μm.

Demonstration of re-use of a BSGS

To demonstrate reusability, a BSGS was used for a first 1st TcEP cycle and then cleaned by O_2 plasma treatment (200 mTorr, O_2 20 SCCM, 100 W, 20 min, Plasma-Therm RIE). New, as-grown arrays of SWNTs were then transferred to the same BSGS using PVA/thermal tape. After a 2nd TcEP process, we observed expected operation, as shown in Fig. S20b. The behavior of the BSGS in this second cycle was the same as for the first. The successful multiple operation was confirmed by electrical measurements before and after TcEP for each of the two arrays of SWNTs, as summarized in main Fig. 5 b, c.

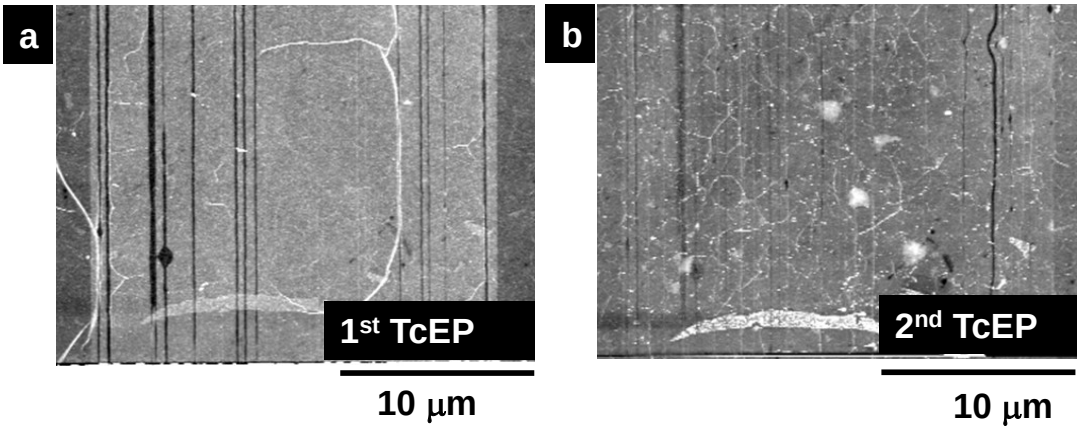

Figure S20. Demonstration of reusability of the BSGS. (a) AFM image after the first TcEP process, showing regions of selective etching of m-SWNTs (dark) and preserved s-SWNTs (light) (b) AFM image after a second TcEP process with the same BSGS, indicating new etched m-SWNTs and preserved s-SWNTs

Off-state stability of operation in top split gate structures

For the purpose of selective metallic nanotube removal by TcEP process, current stability in the 'off state' condition (i.e. large negative gate biases) for the s-SWNTs is particularly important. To verify this stability, we measured current outputs in devices with several s-SWNTs tubes at conditions corresponding to those used to induce thermocapillary flow (i.e, V_{GS}=20V, V_{DS}=-40V, T_{sub}=60^{o}C, 1×10^{-4} torr). Fig. S21(b) shows that the current remains less than several nA throughout the experiment.

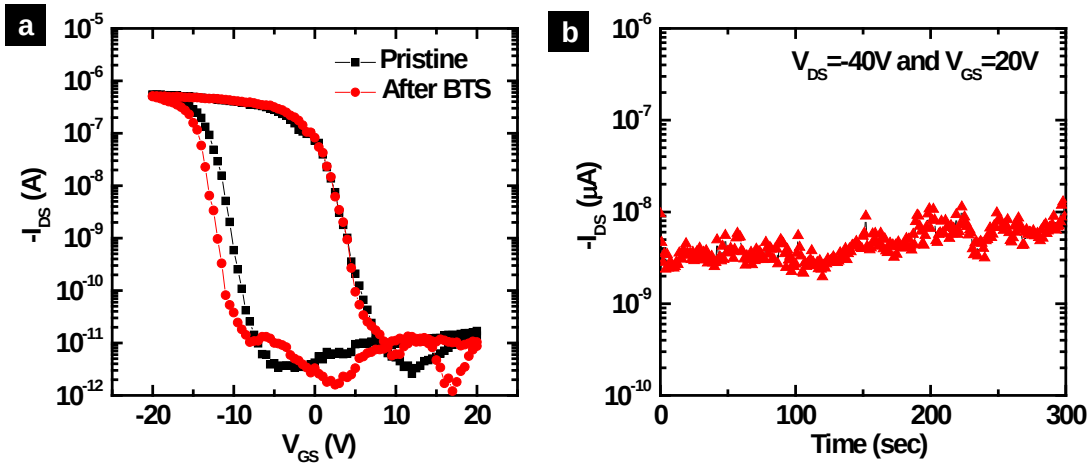

Figure S21. Off state stability for top split gate structures. (a) Transfer characteristics before and after application of bias stress in the off-state, i.e, V_{DS}=-40V and V_{GS}=20V for 5 min and (b) off-state current as a function of time during this test. All characterization was performed under vacuum (1×10^{-4} torr) at a substrate temperature of 60^{o}C.

Off-state stability of operation in top split gate structures

To evaluate on-state stability, we measured current output in the device of Fig. S22 at bias condition (V_{GS}=-20V and V_{DS}=-40V) for 5 min in vacuum (1 x 10^{-4} torr). The results of Fig. S22 indicate that the current in the on-state shows some variation in the first few tens of seconds, likely due to filling of charge traps near the SWNTs and in the gate dielectric, and then remains constant.

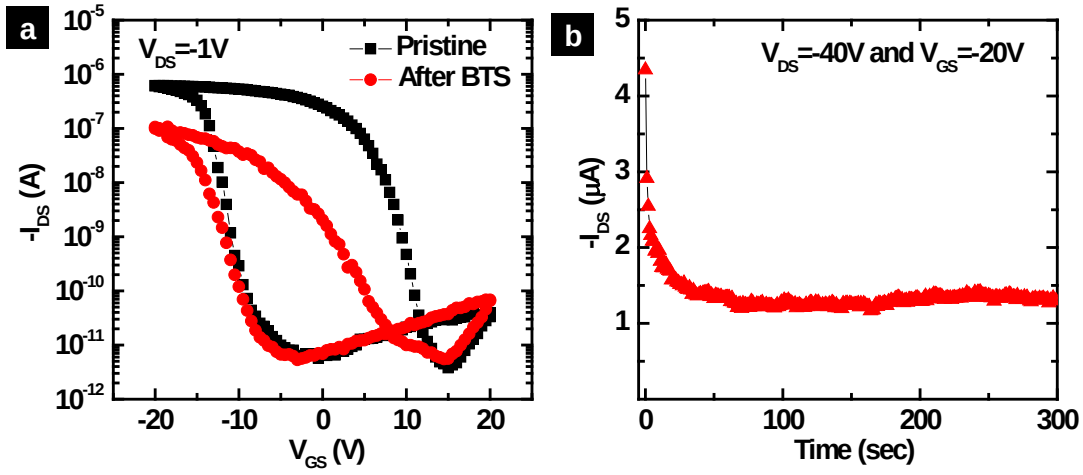

Figure S22 On-state stability of operation in top split gate structures (a) Transfer characteristics before and after application of bias stress in the on-state, i.e, V_{DS}=-40V and V_{GS}=-20V for 5 min and (b) on-state current as a function of time during this test. All characterization was performed under vacuum (1×10^{-4} torr) at a substrate temperature of 60^{o}C.

Full characterization of split gate devices with W/L(=1000/30 μm or 2000/30 μm) after TcEP

For devices with large widths (W/L=1000/30 μm), I-V characteristics after TcEP reveal the maximum achievable current levels, as well as any variations in device switching behavior at high drain biases. In particular, we measured the device of Fig. 4(c), for which W/L=1000/30 μm, at drain biases up to V_{DS}=-40.1 V. Here, Fig.S23b indicates that the maximum output current which can be extracted is ~1.5 mA. To further verify the width scalability of devices with purified arrays of s-SWNTs, we connected two devices with the same physical dimensions (W/L=1000/30 μm) to create an effective dimension of W/L=2000/30 μm, with current outputs of ~3 mA as shown in Fig.S 24b. These results correspond to the simultaneous operation of at least several hundred s-SWNTs. All characterization was performed in dry N_2 ambient.

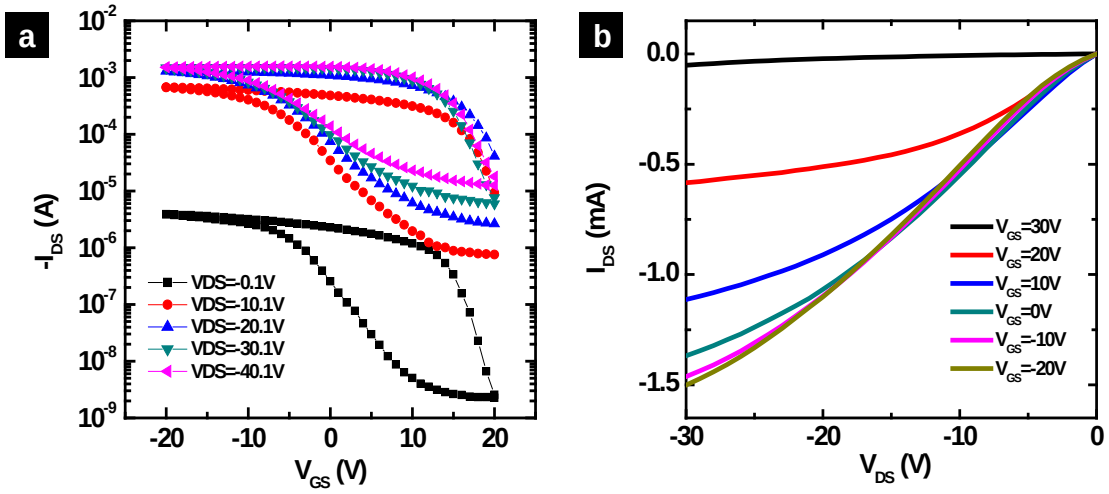

Figure S23 Full characterization of split gate devices. (a) Transfer characteristics for a device with W/L=1000/30 μm after TcEP, evaluated at various drain bias (V_{DS}) conditions (b) output characteristics for this same device. All measurements were performed in a dry N_2 environment.

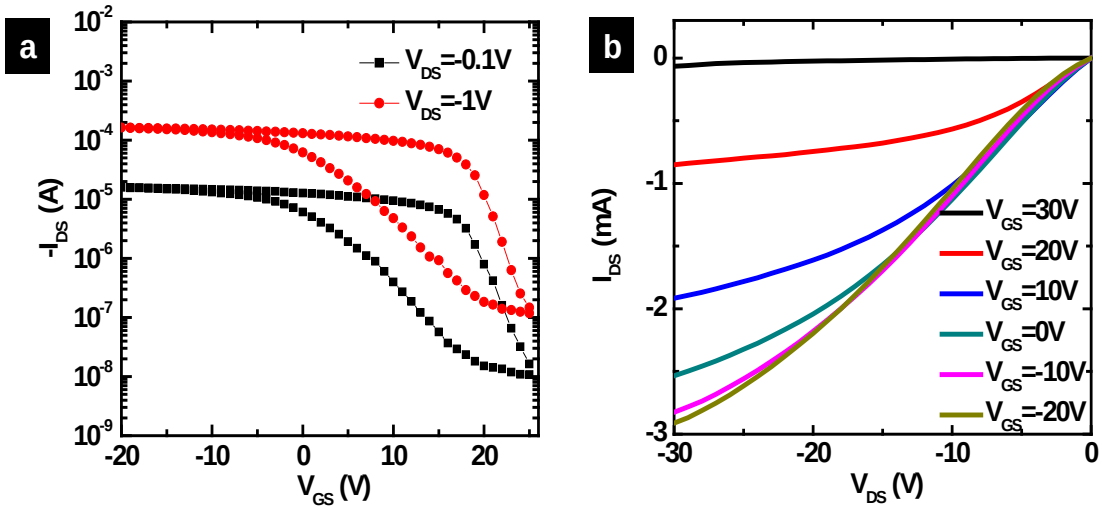

Figure S24 Full characterization of split gate devices. (a) Transfer characteristics for two interconnected, purified devices to form effective channel dimensions of W/L=2000/30 μm, at low drain bias. (b) Output characteristics from the same structure. All measurements were performed in a dry N_2 environment.

On/off ratio as a function of drain bias in split gate devices with large widths

The on/off ratios of devices shown in Fig. 4(a), (b), diminish somewhat at the most extreme bias conditions, due to effects that arise from band bending near the drain and associated band-to-band tunneling (see Supplementary Information, Figs. S26 and S27), but remains close to 100.

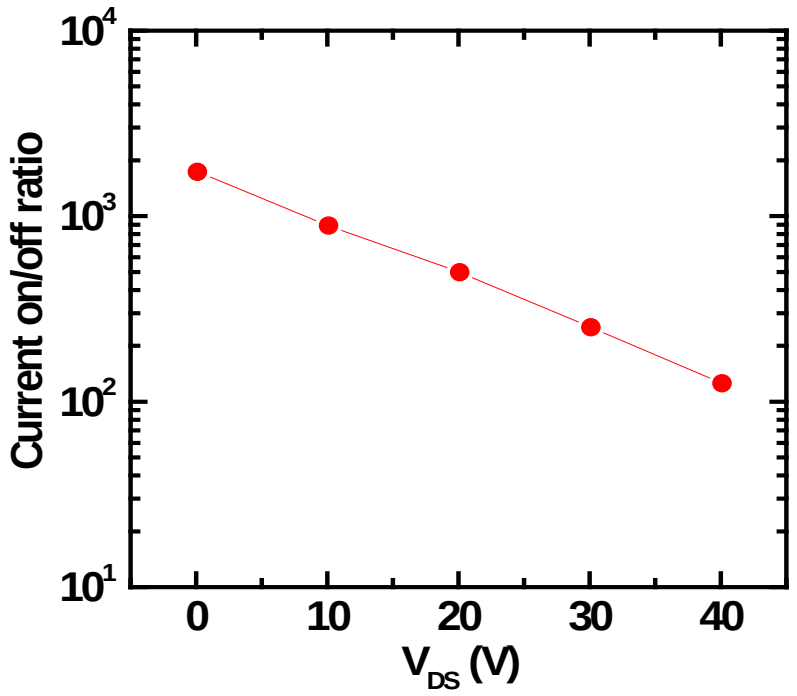

Figure S25 On/off ratio as a function of drain bias for split gate device. On/off ratio as a function of V_{DS} for a device with W/L=1000/30 μm, described in Fig. 4(c).

Electrostatic behavior associated with operation at high bias voltage

The values of on/off ratio (i.e., $I_{DS}@V_{GS}$ = -20 V/$I_{DS}@V_{GS}$ = 20 V) in Fig. S4 and Fig. 6(c) suggest the existence of small bandgap (large diameter) semiconducting CNTs after metallic CNT removal. Fig. S4 is measured for a device that has single semiconducting nanotube as channel. Simulation of I_{DS}-V_{GS} for this device is consistent with a diameter of 1.74 nm (directly estimated by analysis of Raman spectra) for the SWNT and matches the on/off ratio measured by varying overlap length (L_{OV}) and V_{DS} (Fig. S26c). Low on/off ratio for the full-gate device configuration (L_{OV} = L; Fig. S26b) is due to larger band bending near the drain end of the nanotube (Fig. S27a) that induces band-to-band tunneling (BTBT)[22] and high I_{DS} at V_{GS} = 20 V. Band bending near the drain end is relaxed due to the extension of electrostatic gate control in the overlap region (Fig. S27c) and, therefore, BTBT and I_{DS} at V_{GS} = 20 V is lower and on/off ratio is higher for the same nanotube in the partial-gate configuration (L_{OV} < L; Fig. S26a). For all L_{OV} values, band bending (Fig. S27a) and BTBT increases at larger $|V_{DS}|$, therefore, reduces the on/off ratio (Fig. S26c).

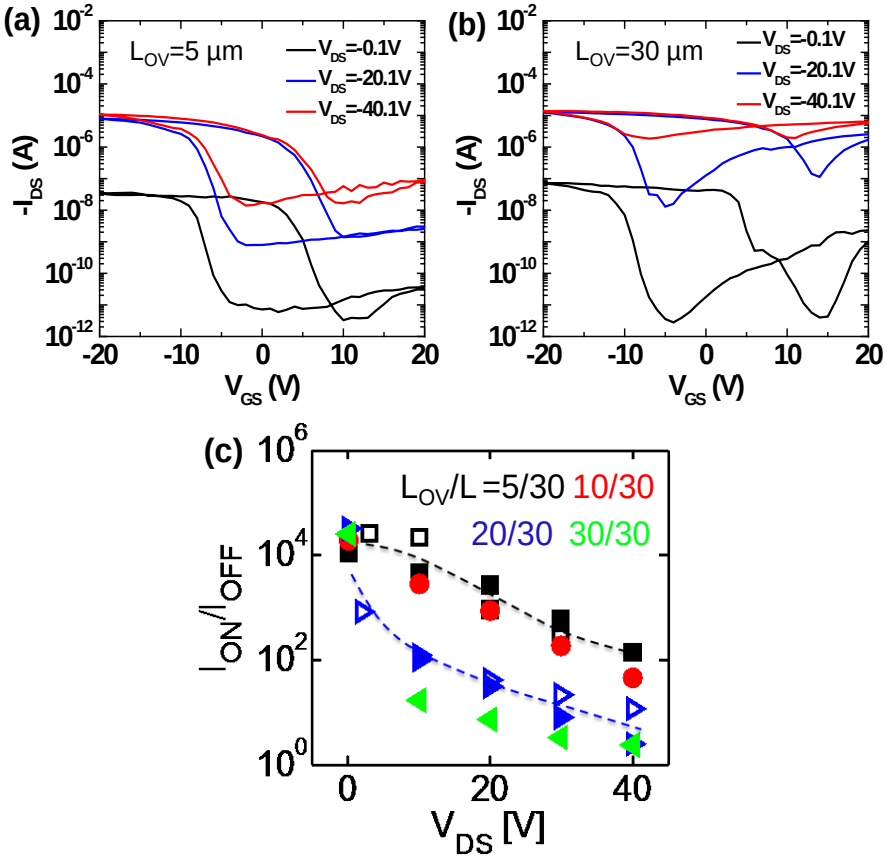

Figure S26 Simulation and experimental results on trends in on/off ratio with bias condition. (a): Experimental I_{DS}-V_{GS} characteristics for different drain bias at (a) L_{OV} = 5 µm and (b) 30 µm. (c) Experimental (solid symbol) on/off current ratio vs V_{DS} for different L_{OV} follows simulation (open symbols are simulated for L_{OV} = 5, 20 µm). Dotted lines are guide to eye only.

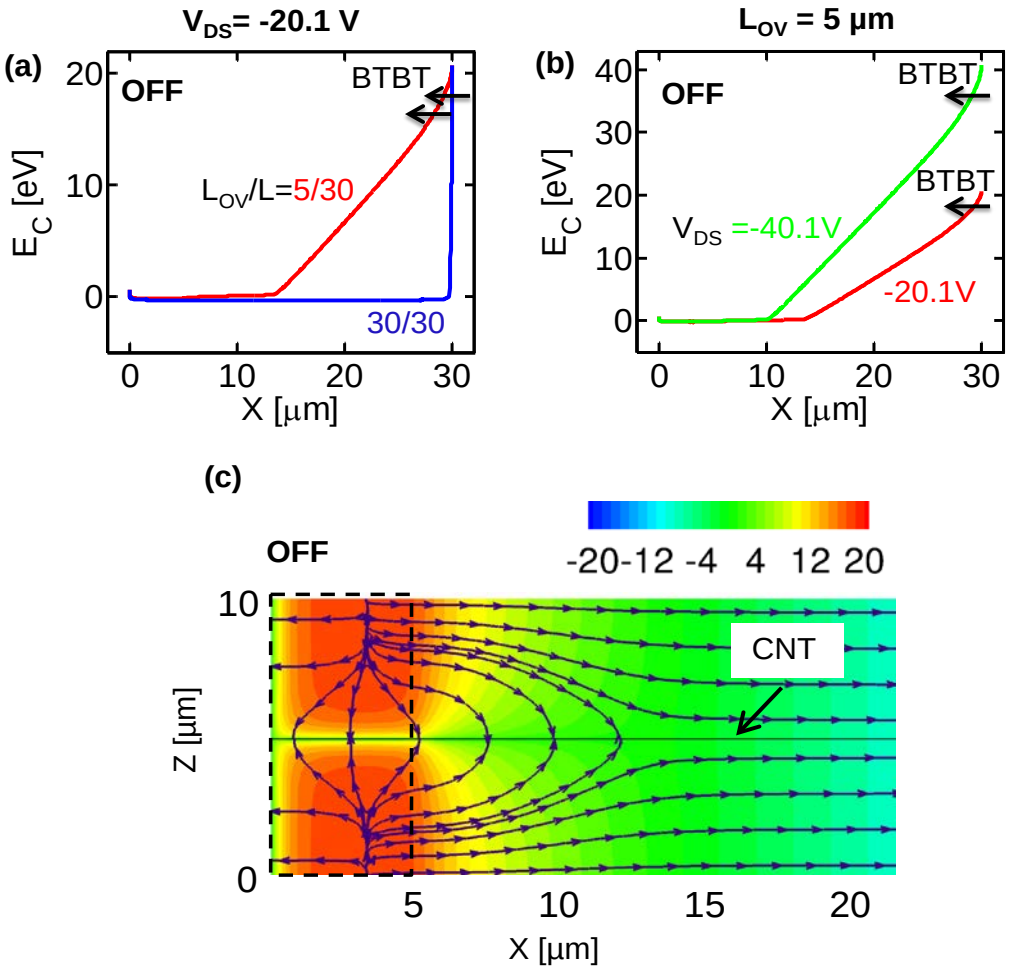

Figure S27: Conduction band profiles along a d = 1.74 nm semiconducting nanotube for different (a) overlap length and (b) drain bias. Regions with higher band bending near the drain end are prone to band-to-band tunneling (BTBT) that increases I_{DS} at V_{GS} = 20 V and, therefore, calculated on/off ratio (i.e., $I_{DS}@V_{GS}$ = -20 V/$I_{DS}@V_{GS}$ = 20 V goes down. (c) Two-dimensional potential profile (color contours) in off-state along the surface of a quartz wafer (directions X and Z are along and across the nanotube, respectively) containing the nanotube. The nanotube is biased in partial-gate FET configuration (Fig. S18a) with L_{OV}/L= 5/30 μm. Electrostatic control of gate extends beyond the gate region and results gradual change in potential along the nanotube and therefore, low BTBT for the partial-gate configuration.

Forming horizontally aligned arrays of SWNTs

Photolithography (AZ 5214 positive photoresist), electron beam evaporation (0.6 nm Fe; AJA), and subsequent liftoff defined regions of catalyst in the geometry of strips oriented perpendicular to the preferred growth direction on ST-cut quartz substrates (Hoffman). Annealing in air at 950 ˚C for 1 hr at the pressure (1 atm)(quartz tube furnace with ~1 inch outer diameter), cooling the furnace, purging it with hydrogen (300 sccm) at the pressure (1 atm), and then heating to 925 ˚C with ramping rate of 50^{o}C/min prepared the iron catalyst for chemical vapor deposition. Introduction of growth gases (20 sccm H_2, 20 sccm Ar, bubbled through ethanol ($T=0^{0}$C) at 925 ˚C for 20 min yielded well aligned arrays of SWNTs.

Fabricating devices that incorporate a single SWNT. The fabrication procedures followed those described above. The use of arrays of SWNT grown at low density (0.1-0.2 SWNT/μm), and subsequently etched in patterns that removed all of the SWNTs except those in narrow strips (~3 μm widths) yielded devices with small numbers of SWNTs. Electrical and AFM analyses identified a subset of such devices that incorporated only a single SWNT bridging the source and drain electrodes.

Removing the gate electrode and dielectric. Following TcEP, the purified SWNTs (i.e. consisting only of s-SWNTs) were protected by a patterned layer of photoresist (AZ 5214) prior to removal of the gate metal (for Ti, Transene, Inc; titanium etchant TFTN; for Cr, Transene, Inc; chrome mask ethant-CE-5M 9). Wet etching (H_2SO_4:H_2O_2=2:1, 60 ˚C, 5 ~10 s) removed the crosslinked PVA. Etching in buffered hydrofluoric acid (BOE 6:1, 30 s) removed the SOG/Al_2O_3 bilayer. Stripping the photoresist completed the process.

Fabricating short channel devices. Following removal of the partial gate transistor structure, phase shift lithography[27], electron beam evaporation (2 nm Ti, 25 nm Pd), and lift-off (facilitated by brief ultrasonication, ~1 min) defined a narrow gap separating new source and drain electrodes on a purified array of s-SWNTs. PDMS stamps for phase shift lithography were cast and molded (Dow Corning, Sylgard) from a Si master, fabricated by photolithography (AZ 5214) and Bosch etching (etch/passivation, cycle time: 5 sec/5 sec, RIE power: 20 W/0 W, 35 sccm SF_6, 110 sccm C_4F_8, for constant ICP power of 600 W, etch rate: 1 μm/80 s) in SF_6 to a depth of ~1 μm. Following liftoff, the dimensions of source and drain electrodes were further defined by photolithography (AZ 5214) and a combination of wet and dry chemical etching (Transene Pd etchant, 50 sec, followed by RIE, 40 sccm CF_4, 1.2 sccm O_2, 150 W, 30 sec; Plasma-Therm). Gate dielectric layer (~30 nm) of HfO_2 was deposited by electron-beam evaporation followed by atomic-layer deposition of HfO_2(10 nm). Photolithography (AZ 2070), and sputtering (70 nm Ti, 150 W, 3 mTorr Ar; AJA International), followed by lift-off defined gate electrodes, to complete the devices.

Fabricating inverters. First, TcEP yielded two purified arrays of s-SWNTs. Photolithography (AZ 5214), electron beam evaporation (2 nm Ti, 48 nm Pd) and lift-off then patterned source and drain electrodes for the driver transistor (L= 3.5 μm, W=30 μm). The electrodes associated with the TcEP processes were used for the load transistor (L=30 μm, W=30 μm). Previously described procedures[28] yielded SOG/HfO_2 (35 nm/20 nm) dielectrics for both transistors. Photolithography (AZ 5214), electron beam evaporation (100 nm Ti) and lift-off defined the gate electrodes.

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