

Quantum Confinement Effects in Transferrable Silicon Nanomembranes and Their Applications on Unusual Substrates

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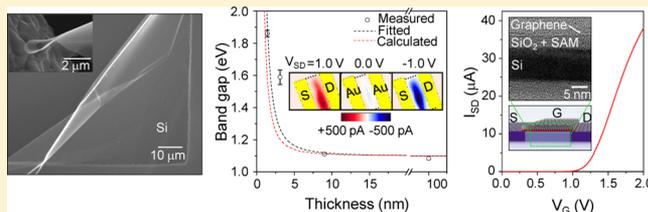
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Supporting Information

ABSTRACT: Two dimensional (2D) semiconductors have attracted attention for a range of electronic applications, such as transparent, flexible field effect transistors and sensors owing to their good optical transparency and mechanical flexibility. Efforts to exploit 2D semiconductors in electronics are hampered, however, by the lack of efficient methods for their synthesis at levels of quality, uniformity, and reliability needed for practical applications. Here, as an alternative 2D semiconductor, we study single crystal Si nanomembranes (NMs), formed in large area sheets with precisely defined thicknesses ranging from 1.4 to 10 nm. These Si NMs exhibit electronic properties of two-dimensional quantum wells and offer exceptionally high optical transparency and low flexural rigidity. Deterministic assembly techniques allow integration of these materials into unusual device architectures, including field effect transistors with total thicknesses of less than 12 nm, for potential use in transparent, flexible, and stretchable forms of electronics.

KEYWORDS: Two-dimensional material, single-crystal silicon, graphene, quantum confinement, transparent transistor, flexible electronics



A dominant path in the development of advanced electronics involves the continued reduction in the critical dimensions of transistors for increased operating speed and density of integration in circuits.¹ At the same time, improved electrostatic control demands decreases in the thicknesses of the gate dielectrics and in many cases the semiconductor itself.² For emerging, unusual forms of electronics, reductions in thicknesses offer other important benefits, including (i) exceptionally low bending stiffnesses and degrees of bendability, (ii) minimal optical absorption through the visible range, (iii) low energy release rates associated with fracture at interfaces with unconventional substrates, and (iv) confinement effects that can alter significantly the electronic properties. These resulting characteristics create many opportunities in

unusual devices, including flexible, stretchable, and transparent classes of electronics for systems such as smart glasses, see-through displays, and wearable electronics. Here, we demonstrate techniques for forming and manipulating large, uniform silicon nanomembranes (Si NMs) with thicknesses that approach those of 2D materials.^{3–9} This class of material offers important advantages over other emerging 2D semiconductors, including (i) compatibility with established semiconductor techniques such as well-developed doping techniques, (ii) exceptional materials quality and compositional purity, and (iii) straightforward paths for integration into existing Si-based

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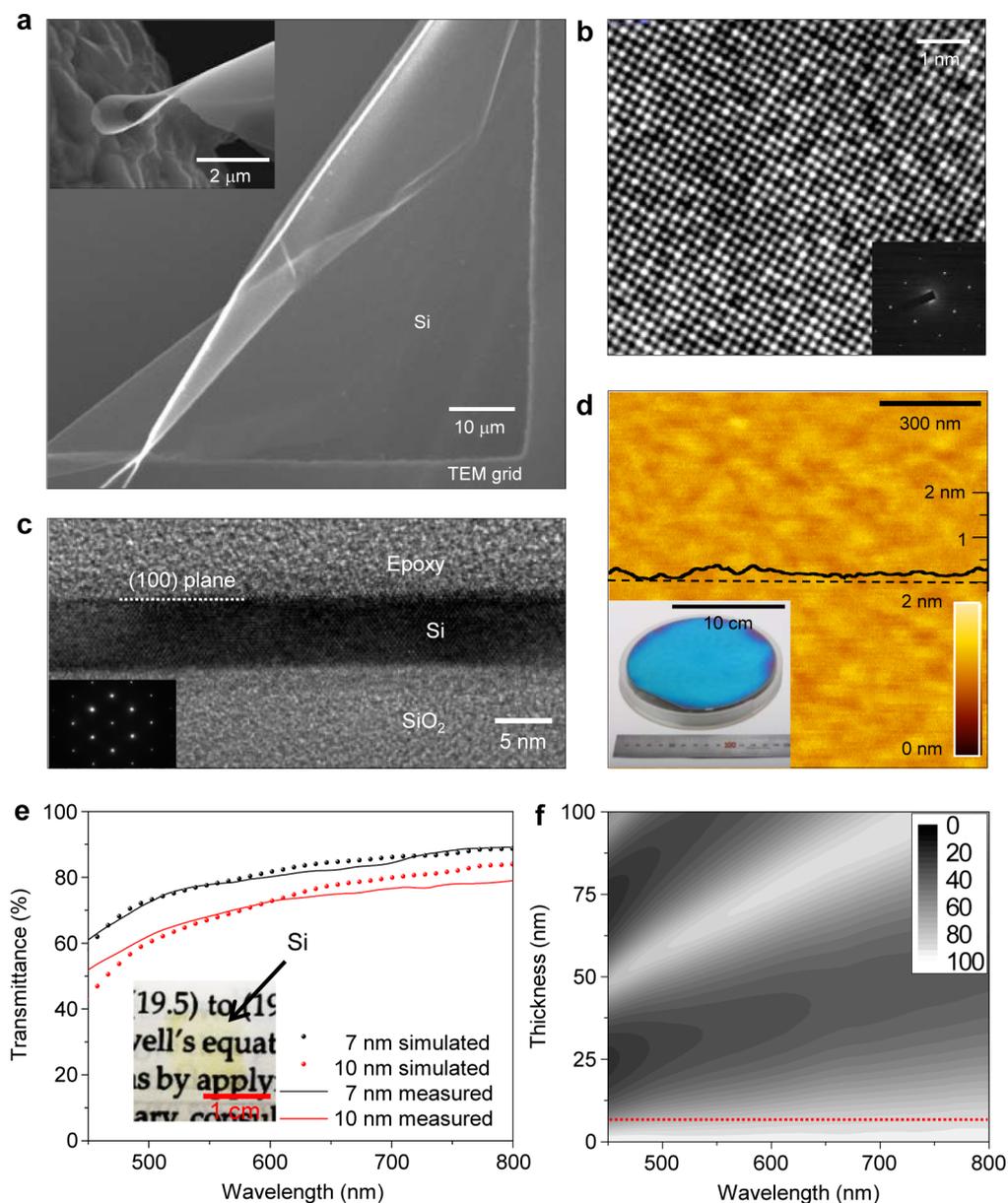


Figure 1. Observing Si NMs and their optical property (a) A SEM image of an ultrathin Si NM on a TEM grid. The inset provides an SEM image of such a Si NM bent to a curvature radius of ~ 500 nm. (b) HR-TEM image of the Si NM (top view). The inset shows (100) zone axis diffraction pattern. (c) TEM image of a Si NM with thickness of 7 nm (side view). The inset shows (110) zone axis diffraction pattern. (d) AFM topographical image of an ultrathin top Si layer on an SOI wafer, showing an RMS roughness of 0.067 nm. The inset shows 6 in. SOI wafer. (e) Simulated and measured transmittance of a structure of native oxide/Si NM/epoxy/PET. The thickness of the Si NM is 10 nm (black) and 7 nm (red), measured by ellipsometry. The inset shows an optical image of the Si NM transferred onto a sheet of PET. (f) Simulated transmittance of a structure of native oxide/Si NM/epoxy/PET as a function of wavelength and thickness of the Si NM. The red dot indicates the case of 7 nm.

electronic platforms. In addition, we present materials and fabrication schemes for transferrable silicon transistors that use these materials, in which the electrodes have atomic-scale thicknesses, via the use of monolayer graphene, the dielectrics have molecular-scale thicknesses, via the use of organic self-assembled monolayers (SAMs), and the semiconductors have nanoscale thicknesses, via the use of Si NMs. The electrical characteristics of these devices, which we refer to as ultrathin film transistors (U-TFTs), include low subthreshold swing, high mobility, and on/off ratio. When combined with plastic or rubber substrates, this technology offers important advantages over alternatives that use polymer, oxide, or carbon-based semiconductors.^{10–12}

The U-TFTs involve a multilayer stack of materials formed by a combination of growth and physical transfer. The electrodes consist of monolayer sheets of graphene, selected for their high transmittance, low sheet resistance, and excellent mechanical stretchability.¹³ The gate dielectric consists of an ultrashallow oxide layer and a densely packed SAM, selected for its outstanding electrical properties, as previously demonstrated in organic transistors.¹⁴ The semiconductor consists of a Si NM, chosen both for its established role in advanced, silicon-on-insulator electronics, and its ability to offer optical transparency in NM form. When synthesized and combined together into transistor configurations like that shown in Figure 3a, these materials offer unique, device-level characteristics.

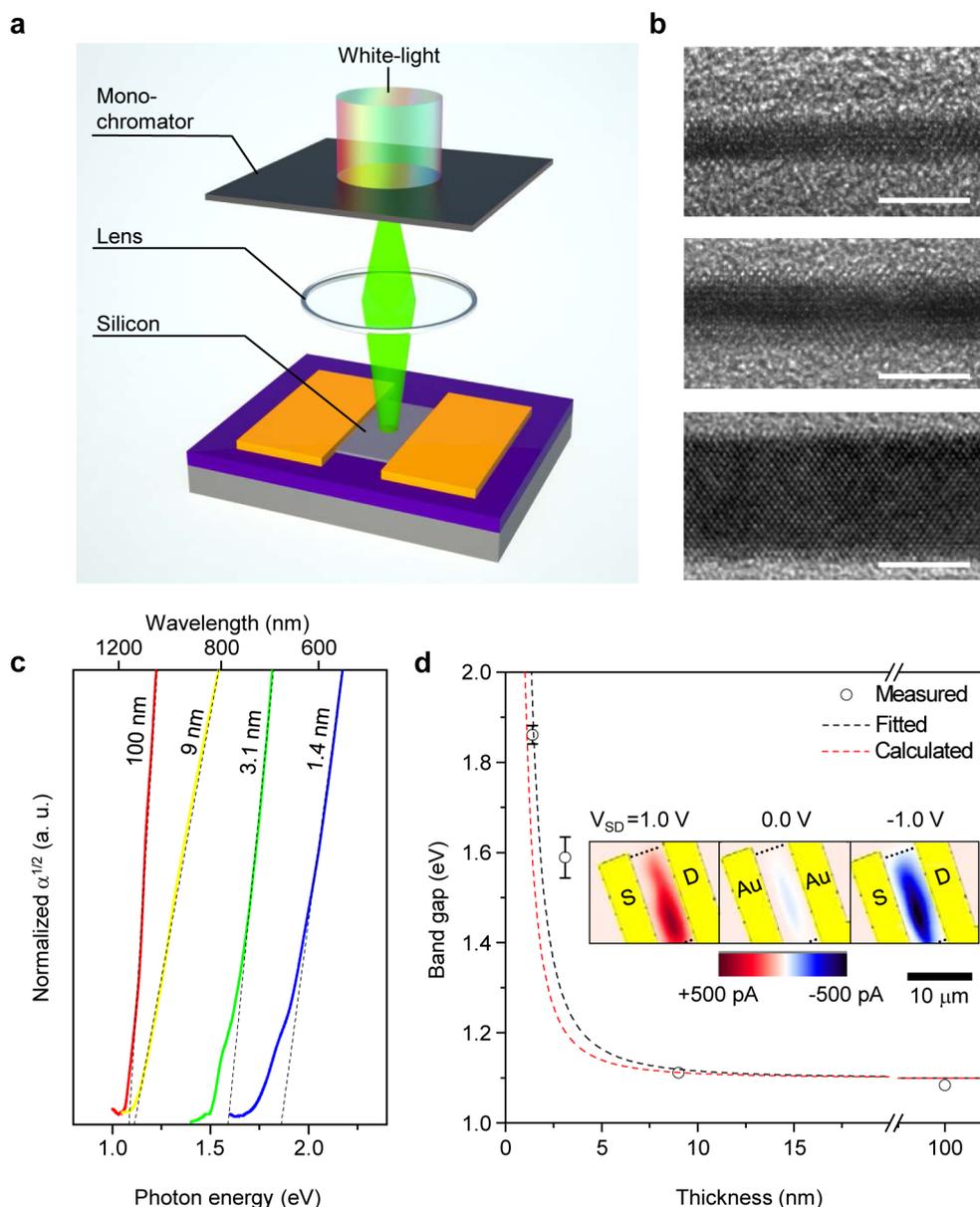


Figure 2. Bandgap change of the ultrathin Si NMs (a) A schematic illustration of the photocurrent measurement system consist of phonon injection with various phonon energy and electrical conductivity measurement system. (b) The TEM images of the silicon with various thicknesses of 1.4, 3.4, and 9 nm from top to bottom, respectively (scale bar: 5 nm). (c) The normalized $\alpha^{1/2}$ as a function of photon energy to show absorption edges of the ultrathin Si NMs with various thicknesses. (d) The measured (circle), fitted curve (black dash), and theoretically calculated (red dash) bandgap of the silicon as a function of the thickness of the silicon. The inset shows I_{ph} images of the ultrathin Si NMs with various drain voltage, which show the photocurrent generated mainly on silicon itself.

Results and Discussion. We begin by describing the fabrication and characteristics of free-standing, Si NMs and their key properties. The process involves two stage oxidation sequences using a silicon-on-insulator (SOI) wafer, that is, Si (100 nm)/SiO₂ (300 nm)/Si (wafer) as previously reported.^{15,16} Thermal oxidation followed by etching of the resultant SiO₂ with hydrofluoric acid (HF) reduces the thickness from 100 to \sim 16 nm, as the first stage. In the second stage, a repetitive process of ultraviolet (UV) oxidation and oxide removal eliminates \sim 0.74 nm of Si per cycle, as shown in Supporting Information, Figure S1. This level of control exceeds that possible with thermal oxidation. Inspection of the resulting ultrathin Si NMs using a scanning electron microscope (SEM), transmission electron microscope (TEM),

and atomic force microscope (AFM) reveals the key properties. Figure 1a shows an image of a representative NM released from the SOI wafer by removal of the SiO₂ with HF, and then transferred onto a TEM grid. Images of the folded geometry (bending radius \sim 500 nm) illustrate clearly the outstanding mechanical compliance and flexibility, both of which result from the ultrathin NM geometry (inset of Figure 1a; Supporting Information, Figure S2 and S3). A Si NM with thickness of 7 nm has a bending stiffness of 8.86 MPa $\cdot\mu$ m⁴, which, by comparison, is 7 orders of magnitude lower than that of otherwise similar structure with thickness of 1.5 μ m (Supporting Information, Figure S3). A magnified image and diffraction pattern collected using a high-resolution TEM (HR-TEM) indicate an unperturbed lattice of the (100) plane

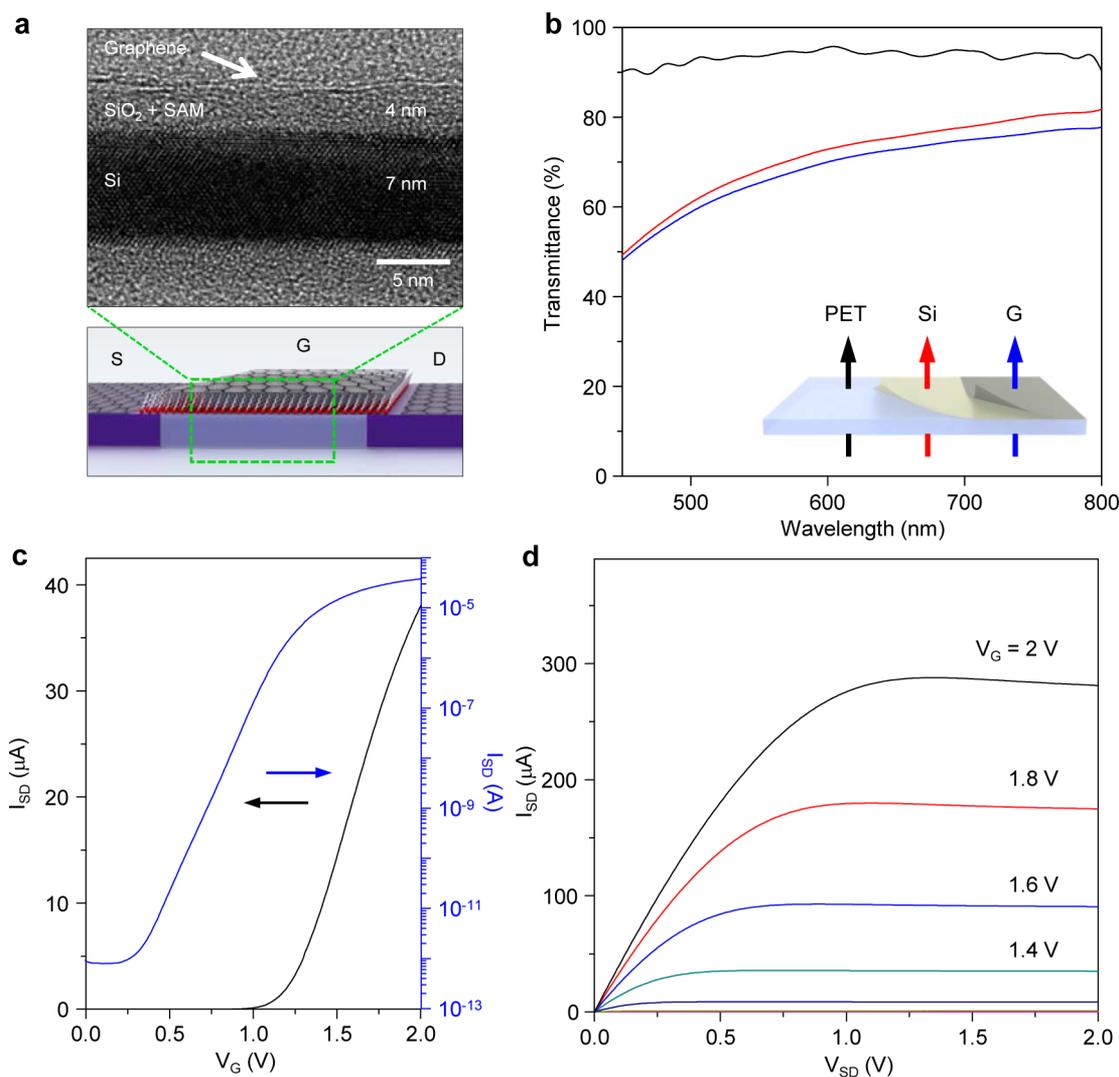


Figure 3. Optical and electrical characterizations of the U-TFTs (a) TEM image and schematic illustration of an U-TFT device with a MOS structure using a Si NM semiconductor, a SAM gate dielectric, and graphene electrodes. The total thickness of the device is less than 12 nm, in its thickest regions. (b) Optical transmittance as a function of wavelength for PET (black), Si NM/epoxy/PET (red), and graphene/Si NM/epoxy/PET (blue). (c) Transfer characteristic of the device in linear (left y -axis) and log (right y -axis) scales, for a channel width of $200\ \mu\text{m}$ and length of $25\ \mu\text{m}$ at a drain voltage of $0.1\ \text{V}$. (d) Full current–voltage characteristics at gate voltages from 0 (bottom) to $2\ \text{V}$ (top) in $0.2\ \text{V}$ steps.

(Figure 1b). A cross-sectional TEM image shows the thickness ($\sim 7\ \text{nm}$) (Figure 1c). (Cross-sectional TEM images of the SOI wafer before and after UV oxidation process appear in Supporting Information, Figure S4) An AFM image of the film surface indicates a roughness (root-mean-square, RMS) of $0.67\ \text{\AA}$ over the full $6\ \text{in.}$ SOI wafer (Figure 1d).

A key feature of ultrathin Si NMs is their high optical transparency throughout the visible range. Figure 1e shows the calculated and measured transmittance spectra for Si NMs with thicknesses of 7 and $10\ \text{nm}$ on a polyethylene terephthalate (PET) substrate coated with a thin layer of epoxy. The results show transmittance values of 78 and 68% at a wavelength of $550\ \text{nm}$ for the 7 and $10\ \text{nm}$ Si NMs, respectively. The results match calculations that use optical constants for bulk silicon. The high transmission follows directly from the nanoscale thickness and indirect bandgap of silicon. The result is simultaneous suppression of Fabry–Perot (F–P) resonances and optical absorption. To highlight these aspects, Figure 1f shows the calculated transmittance as a function of thickness from 0 to $100\ \text{nm}$ across wavelengths from 450 to $800\ \text{nm}$, for a

structure of native oxide ($\sim 1\ \text{nm}$)/Si NM (various thickness)/epoxy ($500\ \text{nm}$)/PET ($200\ \mu\text{m}$). An important effect is that the F–P fringes gradually disappear significantly as the thickness of the Si NM becomes smaller than $40\ \text{nm}$ (Supporting Information, Figure S5). The results show, in particular, dramatic increases in transmission for thicknesses less than $10\ \text{nm}$ (Supporting Information, Figure S6)).

We expect to observe strong optical confinement effects, particularly when Si NM thickness is below $10\ \text{nm}$, considering that the exciton-Borh radius of Si is $\sim 5\ \text{nm}$.¹⁷ In order to investigate the thickness-dependent optical absorption without ensemble-average, as shown in Figure 2a, we performed spatially and spectrally resolved photocurrent (I_{ph}) measurements on individual Si NMs of their thickness of 1.4 , 3.1 , 9 , and $100\ \text{nm}$ (see also Figure 2b) with a white-light supercontinuum laser source coupled to a monochromator as a wavelength tunable excitation system in the range of the incident photon energy from 0.9 to $2.3\ \text{eV}$.¹⁸ The insets of Figure 2d, the scanning I_{ph} images of Si NM channels ohmic-contacted to Ni/Au electrodes, show that the I_{ph} magnitude is mainly arising

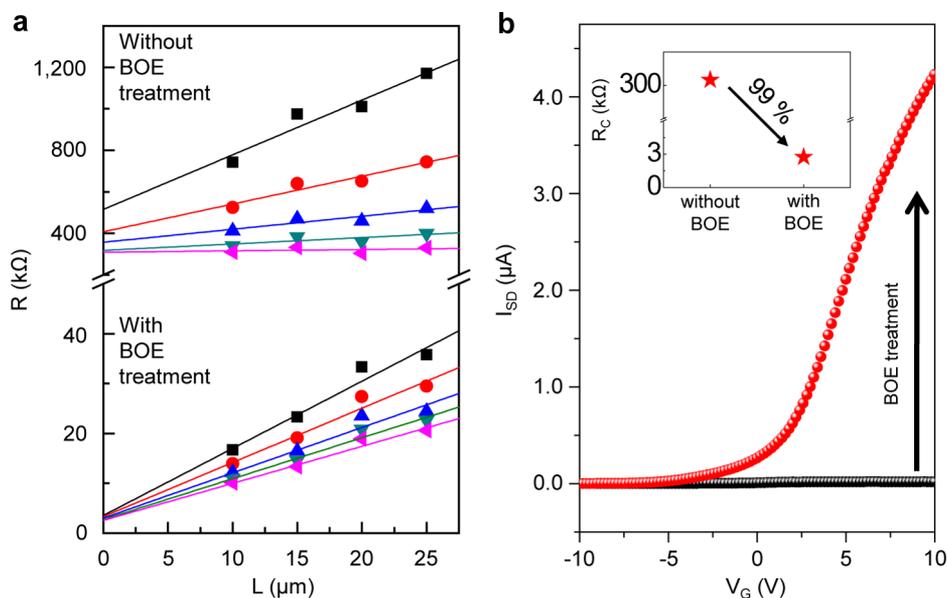


Figure 4. Improving electrical contact property between graphene and silicon (a) On-current resistance at a drain voltage of 0.1 V before and after BOE treatment as a function of channel length at different gate voltages from 10 V (black) to 18 V (pink) in 2 V steps. The intercept of each fitted line shows that the series resistances between graphene and the Si NM before and after BOE treatment are 310 k Ω and 2.7 k Ω , respectively. (b) Transfer characteristic of a Si NM transistor with graphene electrodes. The on-current of the device dramatically increases just after BOE treatment. The inset shows the relative decrease of series resistance after BOE treatment.

from the NM channels, not from the contacts, confirming the spectral I_{ph} information from this measurement, discussed below, indeed pertains to the intrinsic properties of our Si NMs, not from the contact band-bending. The spectrally measured I_{ph} is converted into the effective absorption coefficient, α , according to

$$\alpha = -\frac{1}{t} \ln \left(1 - \frac{I_{ph}}{(1-R)} \frac{h\nu}{G\eta P} \right)$$

where t is the thickness of the NM, R is the reflectance, G is the photoconductive gain, η is the photon-to-carrier conversion efficiency, which is assumed as unity, and P is the incident optical power. Figure 2c is the square root of the α as a function of incident photon energy upon varying the NM thickness, from the relation of $I_{ph} \sim \exp(\alpha) \sim \exp(h\nu - E_g)^2$ for the indirect gap transition near the absorption edge.¹⁹ We then estimate the effective absorption edge by extrapolating the linear portion of the square root of α above the lower limit of the measurable I_{ph} . We find that the on-set of the I_{ph} at around 1.08 eV from the 100 nm thick Si NM, which corresponds to the indirect band gap edge of bulk Si, and it systematically shifts to the higher values with decreasing t below 10 nm. The intercept of the linear fit in Figure 2c, that is an effective measure of the optical band gap of the Si NMs shows reasonable agreement with the calculated ones, as shown in Figure 2d, based on an effective mass theory for a one-dimensional quantum confinement effect.^{20–22} Although the precise assignment of the optical E_g of our Si NMs requires more rigorous model calculations incorporating the surface states, terminations and geometries, this observation principally demonstrates a strong thickness effect in light absorption in our Si NMs to a lowest order, presumable due to quantum size effects.

U-TFTs that incorporate these Si NMs exploit a SAM formed on a UV-ozone treated silicon surface, by vapor-phase assembly for the gate dielectric,²³ and graphene layers

synthesized by chemical vapor deposition for the source, drain and gate electrodes.²⁴ Figure 3a shows a cross sectional TEM image and schematic illustration of this multilayer stack. The thickness of the electrodes (graphene) is 0.3 nm, the gate dielectric (UV-ozone generated oxide plus SAM) is 4 nm, and the semiconductor (Si NM) is 7 nm. The total thickness of the resulting device is therefore less than 12 nm, even in its thickest regions (Detailed fabrication processes are explained in Supporting Information, Table S1 and Figure S7–S12). The optical transmittance in areas with and without graphene electrodes at a wavelength of 550 nm are 65.8% and 68%, respectively (Figure 3b). The difference in these two values is 2.2%, corresponding to the transmittance of a single layer of graphene.²⁵ The set of curves in Figure 3c shows the electrical properties of a U-TFT with a channel width and length of 200 and 25 μm , respectively. Measurements on 88 devices indicate a yield of $\sim 89\%$, an average mobility of $110 \pm 27 \text{ cm}^2/\text{V}\cdot\text{s}$ and an average subthreshold voltage of $135 \pm 9 \text{ mV}/\text{decade}$ (Supporting Information, Figure S13–S15). The mobility, while high compared to those of transparent oxide semiconductors, are lower than those observed in conventional state-of-the-art silicon transistors, likely due to the poor interface with the SAM dielectric layer.²⁶ The charge trap density of the interface was evaluated as $5.6 \times 10^{11}/\text{cm}^2$ from hysteresis of the device, which is relatively higher than that between Si and SiO₂ interface (Supporting Information, Figure S16).²⁷ Current–voltage characteristics at different gate voltages show expected current saturation behavior, with no significant adverse effects of the Schottky contacts at the source and drain (Figure 3d). A notable feature of the device structure is that the physical integrity of the graphene layer and the associated transfer process for its integration, lead to exceptionally low leakage currents, i.e. six orders of magnitude lower than that achieved with evaporated metal electrodes in the same device structure (Supporting Information, Figure S17).

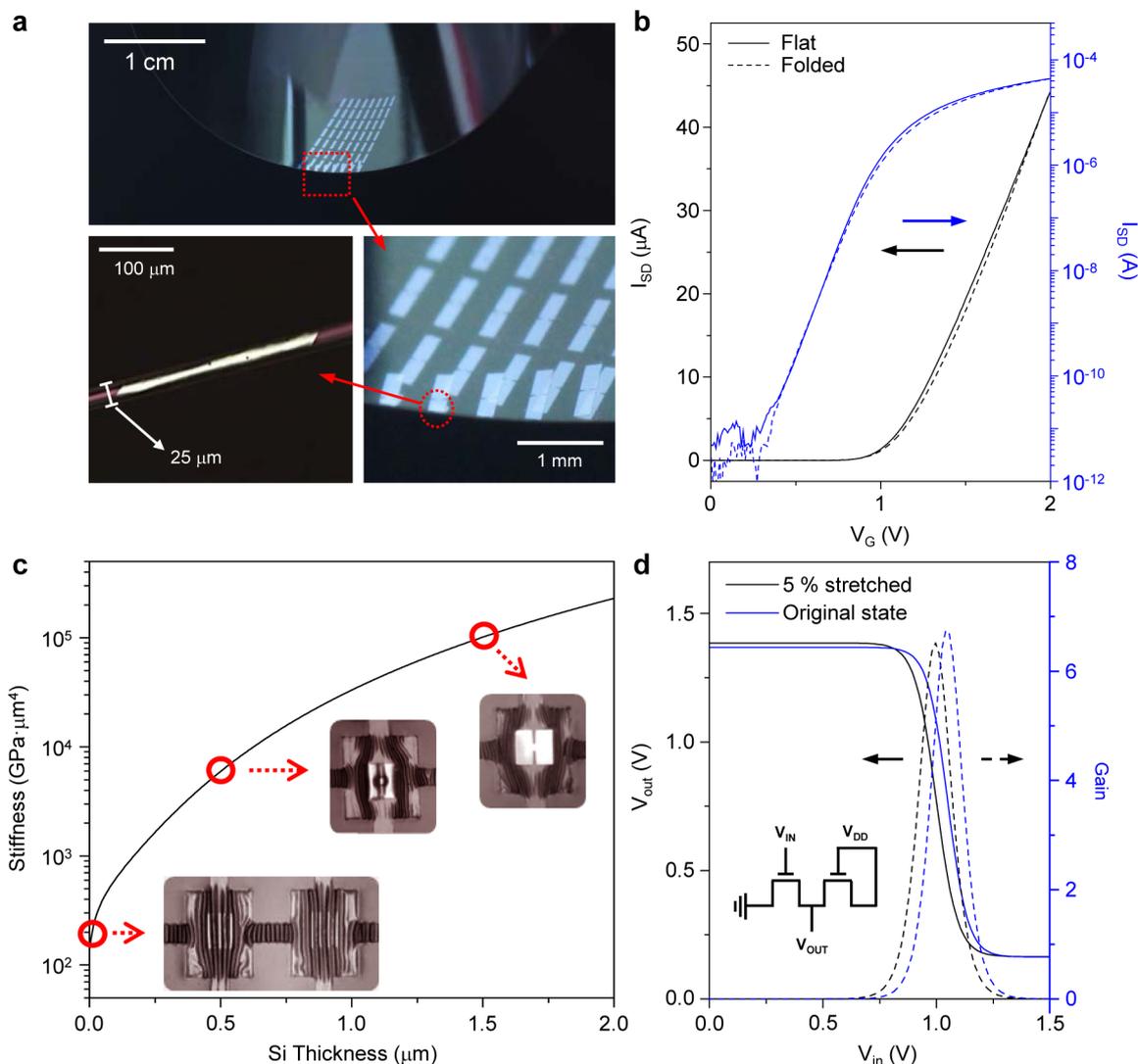


Figure 5. Extremely low stiffness of the U-TFTs (a) Arrays of U-TFTs fabricated on an epoxy sheet with a thickness of 300 nm, folded around the edge of a piece of PET with a thickness of 25 μm (bending radius <12.5 μm) and magnified images showing folded U-TFTs at the edge without cracks. (b) Transfer characteristics of a U-TFT with a channel width of 200 μm and length of 20 μm at a drain voltage of 0.1 V in linear (left axis) and log scale (right axis) before (line) and after folding (dash). (c) Calculated stiffness of the U-TFT based inverters with various thicknesses of Si NMs. A thin encapsulation layer (~150 nm) of epoxy on the top of inverters on PDMS places the devices at the neutral mechanical plane. The inset optical images show devices with various thicknesses. (d) V_{out} – V_{in} characteristics and gain measured at $V_{DD} = 1.5$ V in the wavy configuration and stretched by 5%. The inset shows the corresponding n-mos inverter circuit. The channel width of the load and drive devices are 30 and 240 μm, and the values for channel length of those are 15 and 10 μm, respectively.

The properties of the contacts between graphene and silicon are important to the operation. Figure 4a shows the device resistance (R_{on}) at a drain voltage of 0.1 V, for gate voltages from 10 to 18 V as a function of channel length (L_c). This resistance includes contributions from the silicon/graphene contacts, the graphene itself and the channel of the device. The series resistance, corresponding to the first two of these contributions, can be determined from the intercept of a linear fit of R_{on} versus L_c and y -axis. This value, extracted from devices processed in a way that does not involve removal of the native oxide between graphene electrode and heavily doped Si prior to transfer of the graphene, is ~300 kΩ; with removal of this oxide, the value diminishes by nearly 2 orders of magnitude, to ~2.7 kΩ. The resistance of the graphene itself corresponds to ~1.3 kΩ, suggesting a contact resistance of ~1.4 kΩ. Because of the dramatically decreased contact resistance, the on-current of the device was increased (Figure 4b and for detail studies on

the contact, including transfer length and contact resistivity, see Supporting Information and Figure S18–S20). To maintain good properties at the contact, packaging schemes must prevent penetration of oxygen and resultant formation of oxide layers on the silicon after the fabrication process. We note that other reports indicate that graphene on silicon forms a schottky contact.²⁸ (The energy band diagram appears in Supporting Information, Figure S21, where the work function of graphene was measured by ultraviolet-photoelectron spectroscopy (UPS, ~4.57 eV, Supporting Information, Figure S22) and that of doped Si was calculated from the doping concentration (>10²⁰/cm³) measured by secondary ion mass spectroscopy.) Although the contact potential (V_0), defined by the difference between the work function of graphene and Si, is ~0.6 eV, the high doping concentration used in the Si NMs creates depletion regions narrower than 3 nm. As a result,

tunneling based ohmic contact between graphene and Si NM is possible.²⁹

In addition to the optical and electrical properties, U-TFTs offer exceptional mechanical flexibility when deployed on thin polymer substrates (Supporting Information, Figure S23).³⁰ As it is demonstrated in Figure 5a, arrays of U-TFT integrated onto thin (300 nm) epoxy sheets provide flexibility sufficient to allow folding around the edge of a PET with thickness of 25 μm . (The corresponding bending radius is 12.5 μm , and bending strain at the surface is 0.5%.) The red dashed mark and arrow show a magnified region and corresponding image, respectively. The U-TFT arrays fold without mechanical failure or significant change in electrical performance (Figure 5b). These devices can be incorporated into integrated circuits, even on rubber substrates, as demonstrated with simple logic gates. The example with a 7 nm thick Si NM shows wrinkling (Figure 5c) without noticeable effects on the output characteristics or gain profiles (Figure 5d). Here, the voltage gain was as high as 6.7; the threshold voltage (V_M) was 1.06 V. This highly wrinkled structure, which is impossible to achieve in thick devices, is a qualitative consequence of the U-TFT geometry. The result enables stable operation without degradation even after repeated stretching of the substrate to strains of 5% or more.

Conclusions. This paper presents ultrathin Si NMs as an alternative to other 2D semiconductors, along with synthesis and assembly techniques for ultrathin transistors based on Si NMs, SAMs, and graphene. The combined optical, mechanical, and electrical properties of Si NM enable devices with regimes of operation that would be difficult to achieve using other approaches. Similar architectures and film-stacking based approaches to fabrication have potential for use with other classes of electronic/optoelectronic materials, semiconductor components and integrated systems.

■ ASSOCIATED CONTENT

Supporting Information

Detailed materials and methods and supplementary figures. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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Notes

The authors declare no competing financial interest.

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■ ABBREVIATIONS

2D, two dimensional; NMs, nanomembranes; SAMs, self-assembled monolayers; Si NMs, silicon nanomembranes; U-TFTs, ultrathin film transistors; SOI, silicon-on-insulator; HF,

hydrofluoric acid; UV, ultraviolet; SEM, scanning electron microscope; TEM, transmission electron microscope; AFM, atomic force microscope; HR-TEM, high-resolution TEM; RMS, root-mean-square; PET, polyethylene terephthalate; F-P, Fabry-Perot; UPS, ultraviolet-photoelectron spectroscopy

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