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# Sources of Hysteresis in Carbon Nanotube Field-Effect Transistors and Their Elimination Via Methylsiloxane Encapsulants and Optimized Growth Procedures

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**The origins of gate-induced hysteresis in carbon nanotube field-effect transistors are explained and techniques to eliminate this hysteresis with encapsulating layers of methylsiloxane and modified processes for nanotube growth are reported. A combined experimental and theoretical analysis of the dependence of hysteresis on the gate voltage sweep-rate reveals the locations, types, and densities of defects that contribute to hysteresis. Devices with designs that eliminate these defects exhibit more than ten times reduction in hysteresis compared to conventional layouts. Demonstrations in individual transistors that use both networks and arrays of nanotubes, and in simple logic gates built with these devices, illustrate the utility of the proposed approaches.**

## 1. Introduction

Single-walled carbon nanotubes (SWNTs) have excellent electronic,[1,2] thermal,[3] and mechanical[4] properties that make them attractive for potential use in radio-frequency electronics,[5] macroelectronic systems,[6,7] and in various types of chemical and biological sensors.[8] Device architectures that incorporate random networks or aligned arrays of individual SWNTs in sub-monolayer coverages provide practical, realistic routes to these and other applications.[9] A significant and persistent challenge in transistors, however, is in the large gate-induced hysteresis that is typically observed, and the associated temporal instabilities in current–voltage characteristics.[10–12] Strategies ranging from the use of surface treatments[12–16] to pulsed-mode operation[17] can be useful in reducing hysteresis for certain cases. Nevertheless, a broadly applicable approach based on new materials and grounded in quantitative theoretical understanding of the underlying causes is missing. Here, we provide detailed experimental and theoretical studies of the sources of hysteresis in top and bottom-gated carbon nanotube field-effect transistors (CNTFETs) that use both random networks and aligned arrays of SWNTs. We demonstrate that encapsulation with methylsiloxanes can reliably suppress hysteresis, when other aspects of the device processing are also optimized.

**Figure 1**a schematically shows the configuration for a typical CNTFET that uses a bottom-gate geometry and a random network of SWNTs, at a density of approximately ≈36 SWNTs per μm$^2$, as channel. This architecture leads to current-voltage characteristics that exhibit large hysteresis (Figure 1b) during forward (positive to negative) and reverse (negative to positive) sweeps in gate voltage ($V_{GS}$). The channel width, $W$, and length, $L$, for the CNTFETs are 30 and 5 μm, respectively. These same dimensions and SWNT configurations are used for all devices except those indicated otherwise. The magnitude of the hysteresis (i.e., $V_{HYST}$) can be defined as the difference between gate voltages needed to induce an average of the maximum and minimum drain current, i.e., $(I_{DS,max} + I_{DS,min})/2$, for the forward and reverse sweep directions.

Fundamentally, hysteresis in CNTFETs arises from defects (shown in Figure 1a) that occur either a) at the interface between the SWNTs and the gate dielectric (interface defects) or b) at some position within the gate dielectric (bulk defects). Hydroxyl groups (–OH), commonly present on oxide surfaces act as interface defects and are considered to be significant contributors to hysteresis.[12,15,16] Charging and discharging of these –OH groups by carriers in the channel region electrostatically modulate the SWNTs, thereby changing their conductivity. With a positive bias on the gate, –OH groups can trap electrons. The result is to shift the threshold voltage ($V_T$) of a p-type CNTFET in the positive direction and to facilitate hole conduction during the forward sweep in gate voltage. A negative gate bias

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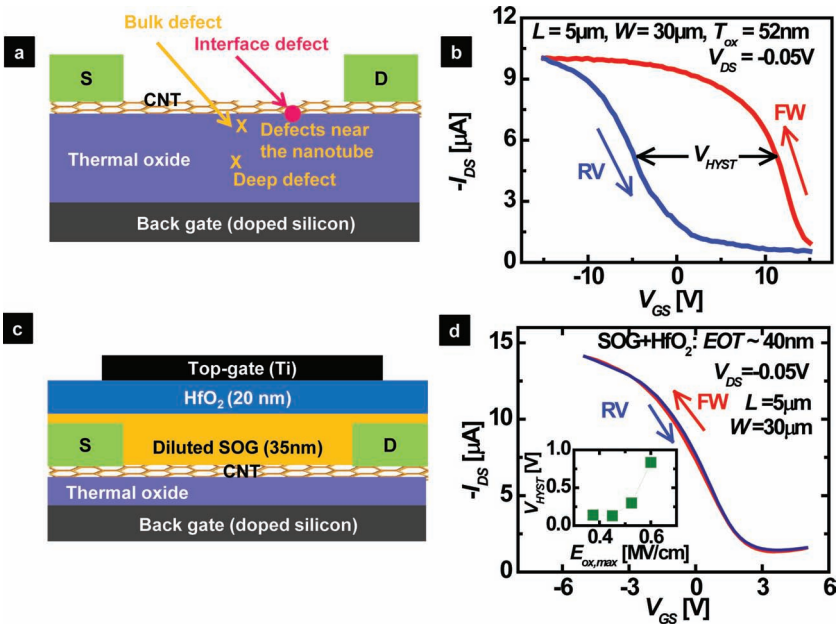


**Figure 1.** a) Cross-sectional schematic illustration of a bottom-gated CNTFET (S,D: source, drain) with cartoon depictions of the two classes of defects responsible for hysteresis: bulk (near the nanotube and deep within the oxide) and interface defects. b) Typical $I_{DS}$–$V_{GS}$ characteristics for such a device, showing extremely large hysteresis ($V_{HYST}$), measured at $(I_{DS,max} + I_{DS,min})/2$ between the forward (FW) and reverse (RV) sweeps. c) Cross-sectional schematic illustration of an optimized dual-gate CNTFET (SOG: Spin-on glass; $HfO_2$: Hafnium oxide). d) $I_{DS}$–$V_{GS}$ characteristics in this case show negligible $V_{HYST}$ (*EOT*: equivalent oxide thickness) at a maximum gate-induced electric field ($E_{ox,max}$) ≈ 0.38 MV cm$^{-1}$ (inset shows the $E_{ox,max}$ dependence of $V_{HYST}$).

discharges –OH groups into their neutral state, thereby reducing $V_T$ and the conductivity for hole transport during the reverse sweep. Physisorbed water molecules at the interface influence the density of these –OH groups,[18–20] and therefore the magnitudes of these behaviors. High temperature annealing under vacuum can reduce this form of hysteresis,[12] by eliminating the water (at >190 °C in vacuum[20]) and, in principle, the –OH groups (at >1000 °C, for $SiO_2$).[20] Other means to address such defects include encapsulation with poly(methyl methacrylate) (PMMA) after thermal annealing,[12] and incorporation of hydrophobic surfaces such as octadecyltrichlorosilanated-$SiO_2$[14,15] or octachlorotrisiloxane-capped organic dielectrics.[13]

The second class of defect (bulk defects) is also important to hysteresis[10,11,17,21] and can arise within the gate dielectric itself, either near the nanotube or into the depth. These bulk defects involve broken bonds within the amorphous oxide network and have been extensively studied magnetically,[22] electrically,[23] and optically.[24] Bulk defects either act as electron traps (i.e., those that switch between negative and neutral charged states) or hole traps (i.e., those that switch between positive and neutral charged states)[25] and can be annealed, for example, in hydrogen ambient.[26]

Here, we use experiments and computational models to explain the physical origin of hysteresis in CNTFETs such as those in Figure 1b. Two distinct classes of hysteresis dominate the observed behaviors that can be traced to two types of defects— bulk and interface— discussed above. Hysteresis arising predominantly from bulk defects cannot be addressed using surface passivation techniques, but instead must be eliminated by optimized fabrication and processing methods. On the other hand, hysteresis associated with interface defects can be suppressed by layers of methylsiloxanes (i.e., spin-on-glass, SOG). When both these approaches are implemented in optimized device architectures (Figure 1c), the two classes of defects are suppressed, thereby yielding significant improvement in the hysteresis behavior at maximum gate-induced electric field ($E_{ox,max}$) of up to ≈0.45 MV cm$^{-1}$ (Figure 1d). (Supporting Information Section 1 provides information on the calculation of $E_{ox,max}$ for all of our devices.) Measurements on dual-gate CNTFETs and other control devices, coupled with theoretical modeling, elucidate the underlying physics and materials aspects, and provide explicit links between the defects and corresponding hysteresis. Use of these methods in forming low-hysteresis inverters based on top-gated CNTFETs with aligned arrays of SWNTs suggests their potential for application in high performance nanotube circuits.

## 2. CNTFET Fabrication

Fabrication of bottom-gated CNTFETs starts with thermal oxidation of heavily doped silicon wafers (which serve as the bottom-gate), followed by deposition of catalyst (ferritin), growth of networks of SWNTs by chemical vapor deposition (CVD), and definition of Pd source and drain electrodes by electron beam deposition and photolithography. Removal of SWNTs from regions outside the channel completes the process. Some of these bottom-gate CNTFETs are transformed into dual-gate configurations by forming a top dielectric structure (spin-coated SOG and atomic layer deposited hafnium oxide $HfO_2$) and a top gate (electron beam deposition and photolithographic patterning of Ti). Removing selected regions of the top dielectric with HF provides access points for probing the source/drain contacts. Fabrication of top-gated CNTFETs with aligned arrays of SWNTs starts with the deposition of parallel stripes of iron as the catalyst on quartz substrates, followed by CVD growth of SWNTs, lithographic definition of Pd source and drain electrodes, removal of SWNTs outside the channel, and, finally, formation of a gate dielectric of SOG/$HfO_2$ and a top-gate of Ti. Details appear in Section 9.

## 3. Characterization and Suppression of Hysteresis

To examine the materials origins of hysteresis, we measure the dependence of $V_{HYST}$ on rate of sweep in $V_{GS}$ (*SR*). By definition,

$SR = V_{step}/t_{step}$, where $V_{step}$ is the magnitude of the step change in gate voltage and $t_{step}$ is the time between such step changes. *SR*-dependent $V_{HYST}$ measurements enable characterization of defects based on their capture/emission time constants.[27] Specifically, the computational model described in Section 4 suggests that: a) interface defects are characterized by short charge capture and emission times (relative to $1/t_{step}$, for the range of $t_{step}$ values studied here), such that $V_{HYST}$ is insensitive to *SR*; b) bulk defects close to the nanotube have small capture but comparatively large emission times, such that $V_{HYST}$ increases with *SR*; and c) deep bulk defects have large capture and emission times, such that $V_{HYST}$ decreases with *SR*.

**Figure 2**a shows the normalized value of $V_{HYST}$, i.e., $V_{HYST}/(qE_{ox,max}/C_{ox})$, measured at different *SR*, for CNTFETs whose hysteresis behavior is dominated by bulk defects close to the nanotube (i.e., $V_{HYST}$ increases with *SR*). The plot of $V_{HYST}C_{ox}/qE_{ox,max}$ in Figure 2 represents the total number of defects ($N_{total} = V_{HYST}C_{ox}/q$) normalized to $E_{ox,max}$; where $E_{ox,max}$ is proportional to the maximum carrier density within the nanotube, $q$ is the electron charge, $C_{ox} = \Xi\varepsilon_{SiO2}/T_{ox}$ or $\Xi\varepsilon_{SiO2}/EOT$ is the capacitance coupling of the nanotubes to the gate, $\varepsilon_{SiO2}$ is the dielectric constant of $SiO_2$, $T_{ox}$ is the oxide thickness, *EOT* is the equivalent oxide thickness for a dielectric other than $SiO_2$,[28] and $\Xi$ is the capacitance ratio that considers the effect of fringing fields.[29] Since the dependence of $V_{HYST}$ on *SR* (Figure 2a) persists at even small values of *SR*, at least 60% of the total defects (which is the ratio of change in $V_{HYST}$ with *SR* to the maximum $V_{HYST}$, as obtained from Figure 2a) must arise from bulk defects located near the nanotube. Therefore, coating these devices with SOG alone (see Section 9.5 for details) and/or employing other means to manipulate the properties of the interface have little effect on these devices, where bulk defects dominate, as confirmed in Figure 2b.

To find an approach that can passivate the bulk defects close to the nanotube, we must understand their physical origin. Detailed study suggests that these defects occur due to oxidation of the surface of the gate dielectric as the catalyst is annealed in air ambient, at temperatures ranging from 27 °C to 950 °C (see Section 9.3 for process details),[30–32] as confirmed by oxide thickness measurements using a Gaertner L116C Ellipsometer (**Table 1**) before and after annealing. This additional oxide has defects at densities that are considerably higher than those in the bulk. Annealing in argon ambient (see Section 9.4 for process details) eliminates this parasitic oxidation (Table 1) and consequently removes the bulk defects near the nanotube. Figure 2c shows a very weak dependence of $V_{HYST}$ on *SR* for devices fabricated using this single process modification, thereby suggesting a reduction of bulk defects near the nanotube. (Similar improvement in terms of bulk defects may be possible by using nanotube growth procedures that do not require air annealing.)[33] The measurements on these devices, which are prepared using argon annealing of catalyst, indicate the possible presence of bulk defects (≈3–20% of total defects) deep within the oxide, as indicated by a weak decreasing trend in $V_{HYST}$ with increasing *SR* (most noticeable for the case of 14 and 31 nm thicknesses), and interface defects. Therefore, Figure 2a,c suggests one order of magnitude improvement in terms of bulk defect density by argon annealing. Most of the defects for devices made with argon annealing are *SR* independent interface defects. These defects can be passivated by SOG to reduce $V_{HYST}$ to only 9–20% of its original value (Figure 2d). The beneficial effects of using SOG arise mainly due to the cross-linking of the linear chains of the SOG with the surface of the $SiO_2$ to form a 3D structure that also eliminates –OH groups, originally at the surface of the $SiO_2$, as confirmed using Fourier transform infrared (FTIR) analysis in other, unrelated studies.[34,35] Measurements on top-gated CNTFETs with SOG/$HfO_2$ gate dielectric (schematic in Figure 1c) show low $V_{HYST}$ at $E_{ox,max} < 0.45$ MV cm$^{-1}$ (Figure 1d) and also indicate a reduction of normalized $V_{HYST}$ at higher *SR* (**Figure 3**). This behavior suggests the presence of bulk defects as the origin of the remaining hysteresis. Supporting Information Figure 1 shows that although SOG reduces $V_{HYST}$ that arises from interface defects, it does not influence bulk defects. In addition, Supporting Information Figure 2

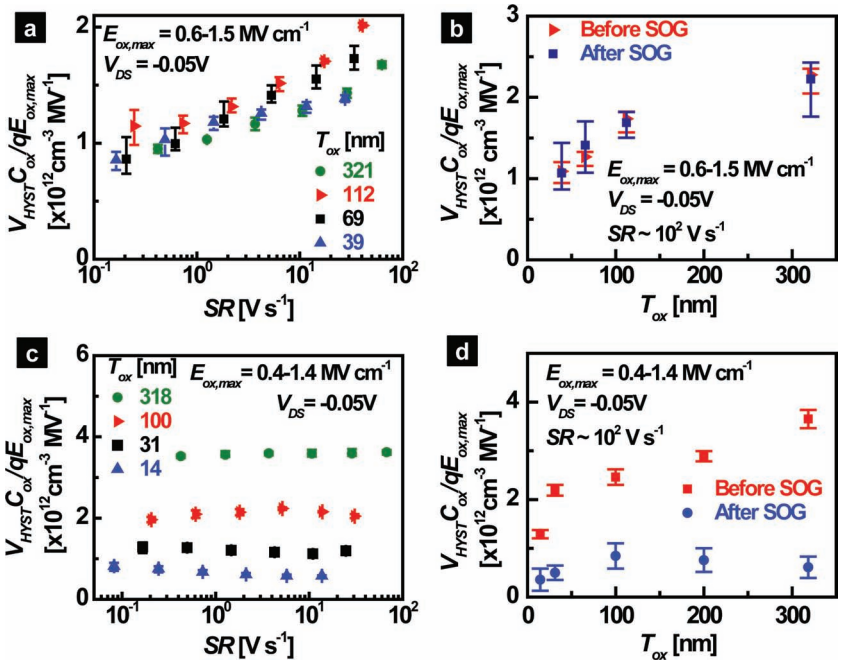


**Figure 2.** Plot of $V_{HYST}$, normalized using the oxide capacitance $C_{ox}$ and the maximum gate-induced electric field $E_{ox,max}$, as a function of a) sweep rate (*SR*) and b) oxide thickness ($T_{ox}$) for bottom-gated CNTFETs, fabricated with catalyst annealed in air (Section 9.3). Increases in $V_{HYST}$ with *SR* suggest the presence of near-interface bulk defects (see Figure 4 and Section 4.1) and, therefore, negligible effect of interface defect passivation techniques like SOG. Plot of normalized $V_{HYST}$ as a function of c) *SR* and d) $T_{ox}$ for bottom-gated CNTFETs, fabricated with catalyst annealed in argon (Section 9.4). Negligible *SR* dependence for these CNTFETs suggests the dominance of interface defects (see Supporting Information Figure 3a,c and Section 4.2), with small contributions from deep bulk defects (see Figure 5 and Section 4.3). Here, significant reduction of $V_{HYST}$ occurs with SOG passivation layers.

**Table 1.** Oxide thickness measured for bottom-gated CNTFETs before (pristine oxide) and after annealing in air and argon using Gaertner L116C Ellipsometer. Annealing in air (27 °C → 950 °C for ≈10 min, 950 °C for ≈1 h, and 950 °C → 27 °C for ≈20 min; process details are given in Section 9.3) increases the oxide thickness significantly. Performing the same annealing step in argon ambient (process details are given in Section 9.4) avoids this increase.

| Before annealing [nm] | After annealing in air [nm] | After annealing in argon [nm] |
|---|---|---|
| 13.6 ± 0.1 | 38.8 ± 0.4 | 14.4 ± 0.1 |
| 30.8 ± 0.2 | 52.5 ± 0.7 | 31.2 ± 0.2 |
| 95.9 ± 0.1 | 112.2 ± 1.7 | 99.8 ± 0.2 |
| 316.0 ± 0.8 | 321.2 ± 0.7 | 318.3 ± 0.8 |

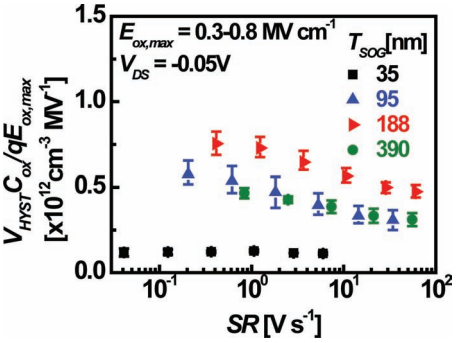


**Figure 3.** Plot of normalized $V_{HYST}$ as a function of *SR* for top-gated CNTFETs (Figure 1c) with different SOG thicknesses ($T_{SOG}$). Decreases in $V_{HYST}$ with *SR* suggest the presence of bulk defects (more for thicker SOG) within the SOG/$HfO_2$ dielectric.

compares hysteresis for the optimized CNTFET having 35 nm SOG/20 nm $HfO_2$ with hysteresis for CNTFET having 20 nm $HfO_2$ alone. These results confirm the beneficial role of SOG in reducing hysteresis.

## 4. Sweep Rate Dependence of Hysteresis

The preceding section summarized experimental observations of ways to change process conditions that can reduce hysteresis. We have explained qualitatively how these improvements can be attributed to suppression of various types of defects. In this section, we explain the experimental observations of Figure 2 and the associated inferences on materials-level sources of hysteresis using a simulation framework. More specifically, we compare the measured and simulated *SR* dependence of $V_{HYST}$ that only depends on the nature of contributing defects, irrespective of the types of nanotubes (see Supporting Information Figure 3). Supporting Information Figure 4 and Supporting Information Section 3 summarize the algorithm for calculating $I_{DS}$–$V_{GS}$ characteristics in a device structure that includes a single semiconducting SWNT (1 nm diameter), with both bulk and interface defects. To calculate $I_{DS}$ during the forward and reverse sweeps, we solve the Poisson equation for different gate biases, $V_{GS}$. Converged potential profiles at a given $V_{GS}$ enable calculation of electron and hole densities (using equations from ref. [36]) and total trapped charge associated with different defects (using equations from Section 5.5 of ref. [37]). These results allow calculation of $I_{DS}$ (using an equation from ref. [1]) by considering hole conduction for Pd source/drain contacts.[38] The sequence of discussions below follows observations in Figure 2 for different types of defects.

### 4.1. Bulk Defects Near the Nanotube

**Figure 4**a shows measured $I_{DS}$–$V_{GS}$ at two different values of *SR* for a CNTFET with $T_{ox} \approx 112$ nm, prepared by annealing the ferritin catalyst in air ambient (Section 9.3). As *SR* increases, $I_{DS}$ increases during the forward sweep and decreases during the reverse sweep, thereby increasing the hysteresis (inset of Figure 4a). Similar trends occur in simulation when electron traps and hole traps both at a density of ≈3.2 × 10$^{19}$ cm$^{-3}$ (≈0.14% of molecular density of $SiO_2$[39]) reside near the nanotube within the oxide (Figure 4b). The electron traps placed near the conduction band of nanotube have small capture times and large release times (Supporting Information Figure 5b,d,f). As the forward sweep proceeds, increasing numbers of trapped electrons electrostatically dope the SWNT in a way that leads to more rapid increases in $I_{DS}$ during the forward sweep than the reverse sweep. For higher *SR*, the electrons have less time to release during the forward sweep (Supporting Information Figure 5f), thereby increasing the hysteresis (inset of Figure 4b).

### 4.2. Interface Defects

Simulations of CNTFETs with only interface defects show negligible variation of hysteresis with sweep rate (Supporting

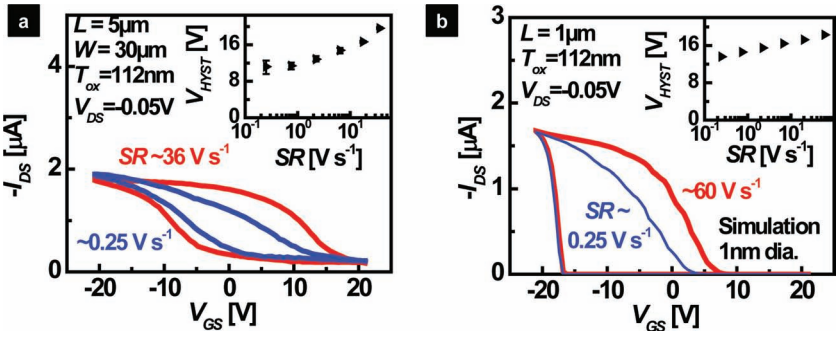


**Figure 4.** a) $I_{DS}$–$V_{GS}$ characteristics measured at two representative *SR* for a bottom-gated CNTFET that shows increasing $V_{HYST}$ with increasing *SR* (inset). b) *SR* dependent $I_{DS}$–$V_{GS}$ characteristics for a simulated CNTFET that incorporates a single semiconducting SWNT (1 nm diameter) with near-interface bulk defects (3.2 × 10$^{19}$ cm$^{-3}$). This type of defect leads to higher $V_{HYST}$ for higher *SR* (inset).

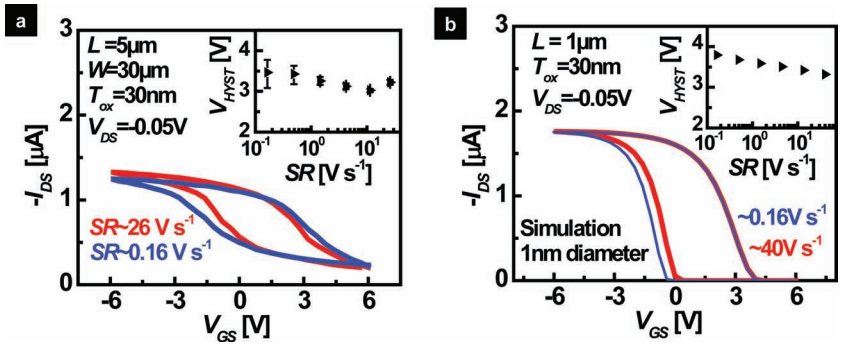


**Figure 5.** a) $I_{DS}$–$V_{GS}$ characteristics measured at two representative *SR* for bottom-gated CNTFETs that show decreasing $V_{HYST}$ with increasing *SR* (inset). b) *SR* dependent $I_{DS}$–$V_{GS}$ characteristics for a simulated CNTFET that incorporates a single SWNT (1 nm diameter) with interface defects ($1.6 \times 10^{14}$ cm$^{-2}$) and deep bulk defects ($8 \times 10^{18}$ cm$^{-3}$). The latter type of defects leads to decreasing $V_{HYST}$ with increasing *SR* (inset).

Information Figure 5c). The Marcus–Gerischer (MG) theory[40] provides a means to account for these defects, which likely arise from –OH groups in the device structures reported here, as discussed previously and elsewhere.[19,41] These –OH groups have separate energy levels for discharged (neutral) and negatively charged states (Supporting Information Figure 5a). We assume the separation between the discharged and charged states, called the reorganization energy,[41] to be similar to the bandgap of the simulated SWNT. Negligible *SR* dependence in simulated $I_{DS}$–$V_{GS}$ characteristics (Supporting Information Figure 5c) suggests fast charging and discharging of –OH groups, located at the CNTFET interface. We note that the choice for reorganization energy affects only the magnitude of $V_{HYST}$, but not the *SR* dependence.

### 4.3. Interface Defects and Deep Bulk Defects

**Figure 5**a plots $I_{DS}$–$V_{GS}$ at two different values of *SR* for a CNTFET with $T_{ox} \approx 30$ nm, prepared by annealing the ferritin catalyst in argon ambient (Section 9.4). With increasing *SR*, $I_{DS}$ decreases during the initial phases of the forward sweep and increases during the reverse sweep. Consequently, $V_{HYST}$ decreases with increasing *SR* (inset of Figure 5a). Similar trends occur in simulations (Figure 5b) that involve hole traps with density of $8 \times 10^{18}$ cm$^{-3}$ (≈0.04% of molecular density of $SiO_2$)[39] within the oxide bulk, along with interface defects with density of $1.6 \times 10^{14}$ cm$^{-2}$ (comparable to the -OH density at the surface of $SiO_2$ in air).[20] The inset of Figure 5b clearly suggests a decrease in hysteresis with increasing *SR*. Bulk defects have both large capture and release times. As a result, increasing *SR* reduces the number of such defects that contribute to hysteresis (Supporting Information Figure 5g) and thus reduces $V_{HYST}$.

## 5. Materials for Passivating Interface Defects

CNTFETs with hysteresis behaviors dominated by interface defects are of interest because surface passivation techniques can have beneficial effects. To examine the possibilities, we studied various treatments of devices formed using argon ambient annealing conditions (to minimize bulk defects). To evaluate the influence of thermal annealing, we measured $I_{DS}$–$V_{GS}$ at three stages: first in air ambient; second after holding the device in vacuum ($10^{-5}$ Torr in Lake Shore/Desert Cryo probe station) for 10 hours; and third after heating the device at 200 °C (in vacuum) for 10 h and then cooling down to room temperature (also in vacuum). **Figure 6**a shows the results for a bottom-gated CNTFET with $T_{ox} \approx 30$ nm. The vacuum treatment results in mild reduction of the hysteresis to ≈70% of its original value measured in air ambient (see

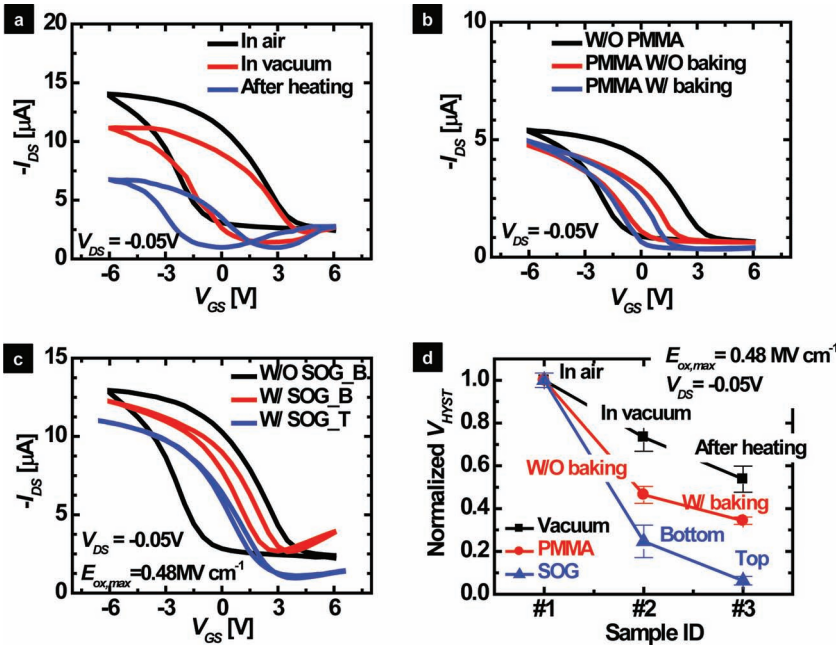


**Figure 6.** Effects of processing approaches and materials designed to reduce hydroxyl groups at the interfaces of bottom-gated CNTFETs ($T_{ox} \approx 30$ nm), whose hysteresis behavior is dominated by interface defects. a) Results from heating in vacuum: $I_{DS}$–$V_{GS}$ characteristics measured in air at room temperature, then after 10 h in vacuum ($10^{-5}$ Torr), and finally after 10 h of heating at 200 °C followed by cooling to room temperature in vacuum. b) Results from PMMA passivation (with: W/and without: W/O): $I_{DS}$–$V_{GS}$ characteristics measured before PMMA coating, after coating and heating for 1 min at 110 °C, and after an additional 15 h annealing at 150 °C. c) Results from SOG encapsulation: $I_{DS}$–$V_{GS}$ characteristics measured at similar $E_{ox,max}$ in bottom-gate configuration (SOG_B) with (W/) and without (W/O) SOG and in top-gate configuration (SOG_T; *EOT* ≈ 40 nm) with SOG. d) Normalized $V_{HYST}$ (with respect to the one measured in air ambient and for bottom-gate configuration) shows that SOG offers the most effective means to reduce hysteresis at $E_{ox,max} \approx 0.48$ MV cm$^{-1}$.

Figure 6d), potentially through partial desorption of phyisorbed water.[12,18,20] Heating reduces the hysteresis further, to 55% of its original value (see Figure 6d). The remaining hysteresis is likely due, predominantly, to residual –OH groups.[20]

We also examined the influence of coatings of PMMA[12] by measuring $I_{DS}$–$V_{GS}$ in three stages: first in air ambient; second after baking the device for 3 h at 300 °C in argon ambient (MBRAUN glove box; $H_2O$ < 0.1 ppm, $O_2$ < 5 ppm) then cooling down to room temperature, followed by coating PMMA (mol. wt. of 950 k, 5 wt%; 3000 rpm for 30 s) and baking at 110 °C for 1 min; and third after 15 h annealing at 150 °C in argon ambient. Figure 6b shows the results for a bottom-gate device ($T_{ox}$ ≈ 30 nm). Baking at 300 °C before PMMA coating removes water and partially removes the –OH groups.[20] Subsequent encapsulation by hydrophobic PMMA[12] and 1 min, 110 °C baking (to remove the solvent) blocks reappearance of the removed –OH groups and reduces hysteresis to ≈45% of the original value (see Figure 6d). Long duration annealing at 150 °C enables reaction between ester groups of the PMMA and surface –OH groups,[12,42] thereby further reducing hysteresis to ≈35% of the original value.

Finally we explored the use of SOG, introduced here as a materials system that is well suited for reducing hysteresis in a form spin-cast directly over the channel region, and subsequently baked in three steps (at 85 °C, 155 °C, and 255 °C), cooled (at 72 °C) to enhance planarization, then cured at high temperature (375 °C), all in an argon ambient (details in Section 9.5). Figure 6c shows the measured $I_{DS}$–$V_{GS}$ characteristics for a bottom-gated device ($T_{ox}$ ≈ 30 nm) before and after application of SOG. Also shown is a top-gated device ($EOT$ ≈ 40 nm) in an otherwise similar geometry, also with SOG. At comparable $E_{ox,max}$, application of SOG reduces hysteresis to ≈20%, compared to its original value, for the bottom-gated CNTFET and ≈5% for the top-gated CNTFET, compared to its value for the bottom-gated CNTFET without SOG (see Figure 6d). The effectiveness of SOG results from the cross-linking process mentioned previously, which effectively removes interfacial –OH groups.[34,35] As discussed earlier, the residual hysteresis is likely due to the presence of deep bulk defects within the dielectric (see Figure 2c and 3); the value reduces to a negligible magnitude as $E_{ox,max}$ reaches below 0.45 MV cm$^{-1}$ (inset of Figure 1d and Supporting Information Figure 6). The effectiveness of reducing interface defect induced hysteresis with optimized (SOG-based) CNTFET presents a significant improvement compared to other reported approaches incorporating PMMA,[12] $HfO_2$,[6] $Al_2O_3$,[43] and hydrophobic surfaces,[13–15,44] where low hysteresis is reported at $E_{ox,max}$ < 0.45 MV cm$^{-1}$. Supporting Information Section 2 provides information on the calculation of $E_{ox,max}$ for these cases.

## 6. Time Dependent Drift in Operation

Operational stability in CNTFETs is a requirement for nearly any application.[45] The hysteresis behaviors, and their dependence on $SR$, enable a clear understanding of the time dynamics associated with different types of defects. The results, in particular, explain the temporal degradation of performance parameters such as $I_{DS}$. Theory and experiment suggest that interface defects

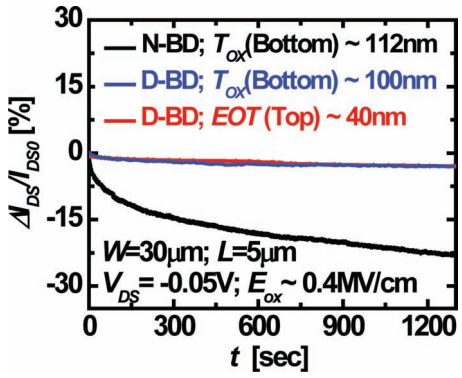


**Figure 7.** Percentage change in drain current ($I_{DS}$) relative to the initial value ($I_{DS0}$) as a function of time ($t$), for three different CNTFETs. The bottom-gated CNTFET with significant levels of bulk defects near the nanotube (N-BD: black line) shows large degradation in $I_{DS}$. Devices with small bulk defects deep within the oxide (D-BD), both in bottom-gate (blue line) and top-gate configurations (red line), show comparatively small degradation in $I_{DS}$.

have capture times less than milliseconds (Section 4.2). As a consequence, temporal variations in $I_{DS}$ (**Figure 7**), measured with approximately second resolution at a gate-induced electric field $E_{ox}$ ≈ 0.4 MV cm$^{-1}$ (with small drain bias to ensure uniform charge injection across the channel), arise mainly due to contributions from bulk defects. Bottom-gated CNTFETs with large bulk defects near the nanotube have large degradation in $I_{DS}$, while devices with negligible bulk defects in the depth show small degradation, on the measured timescales. Degradation can be characterized empirically with stretched exponential forms according to $I_{DS} = I_{DS0}[1 - \exp(-t/\tau)^{\beta}]$, where $I_{DS0}$ is the magnitude of drain current at $t = 0$, $t$ is the time at which degradation is measured, and $\tau$, $\beta$ are fitting parameters.[46] Fitted values yield $\tau \approx 7 \times 10^4$ s for CNTFETs with bulk defects near the nanotube and $\tau \approx 2 \times 10^7$ s for CNTFETs with deep bulk defects, both with $\beta \approx 0.35$. Such analysis confirms that the optimized CNTFETs of Figure 1c exhibit charge trapping only into bulk defects, with small degradation in $I_{DS}$.

## 7. Hysteresis Reduction in CNTFETs with Aligned Arrays of SWNTs

Although the focus of previous sections is on CNTFETs with random networks of SWNTs, similar considerations apply to devices formed with aligned arrays of SWNTs, as well. This aligned geometry is of interest for its potential to yield high performance operation.[47] Similar fabrication procedures and use of SOG yield low-hysteresis top-gated SOG/$HfO_2$ CNTFETs with aligned arrays of SWNTs (see Sections 9.2 and 9.6 for fabrication details and inset of **Figure 8**a for a cross-sectional schematic illustration). Figure 8a,b shows the $I_{DS}$ – $V_{GS}$ and $I_{DS}$– $V_{DS}$ characteristics for a device with approximately 1–2 aligned semiconducting SWNTs within the channel, and negligible hysteresis ($V_{HYST}$ ≈ 0.26 V). Two such CNTFETs can form an inverter, as shown in Figure 8c, with expected transfer characteristics. The gain of the inverter (≈9) is set by the width and length ratio ($W/L$) of load and drive transistors.[48] These results illustrate that low

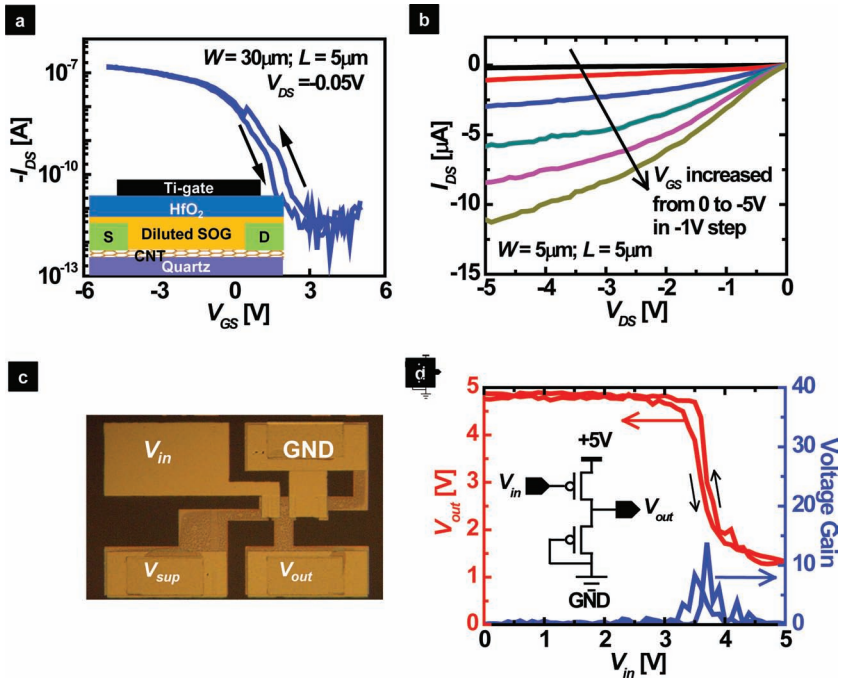


**Figure 8.** a) $I_{DS}$–$V_{GS}$ characteristics measured at $V_{DS}$ = –0.05 V and b) $I_{DS}$–$V_{DS}$ characteristics measured at different $V_{GS}$ for a top-gated CNTFET (inset of (a) shows cross-sectional schematic) with $EOT \approx 40$ nm and aligned semiconducting SWNTs in the channel. c) Optical image of an inverter consisting of two such CNTFETs; the right transistor acts as load ($W/L$ = 5 μm/45 μm) and the left one acts as drive ($W/L$ = 5 μm/5 μm). d) Voltage transfer ($V_{in}$–$V_{out}$) characteristics and voltage gain as a function of input voltage ($V_{in}$) for the inverter in (c). The inset shows the circuit configuration.

hysteresis in individual CNTFETs translates to low hysteresis in simple logic gates and, by extension, more complex circuits.

## 8. Summary

Current–voltage hysteresis in conventional CNTFETs arises from both interface and bulk defects. Measurements as a function of gate-voltage sweep rates, supplemented with computational models, reveal the relative contributions of various sources of defects in individual devices. As applied here, these studies help to guide the selection of optimized materials, growth and processing procedures for minimized hysteresis. Similar strategies to isolate and then eliminate defects can be used with other classes of gate dielectrics and SWNTs formed and processed in other ways. In this sense, the results presented here are useful not only for their identification of a set of specific optimized materials and fabrication approaches, but also for their potential utility in assessing alternatives.

## 9. Fabrication of CNTFETs

### 9.1. Thermal Oxidation for Bottom-Gated CNTFETs

Etching with 10:1 diluted HF solution removed the native oxide from heavily doped (with boron; $\rho < 0.01$ Ω cm) Si wafers. Immersion in piranha solution (3:1 mixture of $H_2SO_4$ and 30% $H_2O_2$) for 10 min eliminated adventitious organic contamination. Dry oxidation in $O_2$ ambient at 1100 °C for different times yielded thermal oxides with thicknesses ranging from 13.6 ± 0.1 nm to 316 ± 0.8 nm (Table 1).

### 9.2. Catalyst Deposition

For growing nanotube networks, wafers with thermal oxide (thickness 13.6 ± 0.1 nm to 316 ± 0.8 nm) were immersed in piranha solution to remove organic contaminants and hydroxylate the $SiO_2$. The resulting surface enabled uniform deposition of 20:1 diluted ferritin (Aldrich) as a catalyst.[6] For growing aligned nanotube arrays, ST (stable temperature) cut quartz wafers served as substrates, with thin films (≈0.8 nm) of iron (as catalyst) via electron beam evaporation (Temescal FC-1500) in parallel stripes patterned by photolithography and lift-off.[47]

### 9.3. Bottom-Gated CNTFETs With Random Networks of SWNTs, and Air Annealing

Annealing ferritin (coated on a $Si/SiO_2$ substrate) in a quartz tube (27 °C → 950 °C for ≈10 min, 950 °C for ≈1 h, 950 °C → 27 °C for ≈20 min), and heating to 925 °C in a hydrogen ambient formed iron nanoparticles (catalyst). Nanotube networks were then grown at 925 °C under a mixed flow of hydrogen (20 sccm), argon (80 sccm), and ethanol vapor (bubbled at 0 °C using $H_2$+Ar) for 20 min. Electron beam evaporation of metal (48 nm Pd, 2 nm Ti) formed source/drain electrodes in regions defined by photolithography. Removal of nanotubes outside the channel region (defined by photolithography) using an oxygen plasma (100 mTorr, 20 sccm, 100 W RF power in a plasma-therm reactive ion etching system) completed the fabrication.

### 9.4. Bottom-Gated CNTFETs With Random Networks of SWNTs, and Argon Annealing

The fabrication followed the procedures described above, except that the initial annealing occurred in argon, rather than in air.

### 9.5. Top-Gated CNTFETs With Random Networks of SWNTs

Substrates with bottom-gated CNTFETs fabricated according to procedures described above were heated at 300 °C for 3 h in argon ambient (MBRAUN glove box; $H_2O$ < 0.1 ppm, $O_2$ < 5 ppm). SOG dielectric was then formed (according to procedures in ref. [49]) by spin-coating (4000 rpm; 60 s) a 15:1

solution of isopropyl alcohol (IPA) and SOG (Filmtronics; siloxanes 215F) at room temperature, and then baking (85 °C for 1 min, 155 °C for 1 min and 255 °C for 1 min) and gradual cooling (30 min) to 72 °C for planarization and defect reduction. Subsequent curing at 375 °C for 1 h in argon ambient facilitated removal of –OH groups.[34,35] The final SOG thickness ($T_{SOG}$) was ≈35 nm. Varying the IPA: SOG dilution ratio changed the SOG thickness (e.g., 5:1, 2:1, and 0:1 dilution ratios yield $T_{SOG}$ ≈ 95 nm, 188 nm, and 390 nm respectively). On top of the SOG layer, 20 nm thick $HfO_2$ was deposited at 120 °C using atomic layer deposition (Savannah 100, Cambridge Nanto Tech Inc.; $H_2O$ + 99.99% $Hf(NM_2)_4$). The fabrication was completed by patterning top gate metal (50 nm Ti) using photolithography and lift-off, and then opening contacts to the source/drain electrodes using concentrated HF solution in regions defined by photolithography. The equivalent oxide thickness (*EOT*)[28] of a top-gated SOG(35 nm)/$HfO_2$(20 nm) CNTFET was ≈40 nm (calculated using the dielectric constant of 3.7 for SOG[49] and 25 for $HfO_2$[28]).

### 9.6. Top-Gated CNTFETs and Inverters With Aligned Arrays of SWNTs

Annealing parallel-stripes of iron (deposited on ST-cut quartz substrate) at 950 °C in a quartz tube, cooling down to room temperature, and heating to 925 °C in hydrogen ambient formed iron nanoparticle catalyst. Aligned SWNTs grew at 925 °C under a mixed flow of hydrogen (20 sccm), argon (20 sccm), and ethanol vapor for 20 min. Definition of source/drain electrodes and removal of SWNTs outside the channel occured according to procedures described for devices with random networks of SWNTs. Top-gated devices used SOG/$HfO_2$ as the gate dielectric and Ti as the top-gate (Section 9.5). CNTFETs with purely semiconducting behavior (yield ≈ 15%) were identified and used for inverter fabrication. The resulting CNTFETs ($L/W$ = 5/5 μm) had 1–2 semiconducting SWNTs connecting the source and drain.

### 9.7. Electrical Measurements

All SR dependent hysteresis measurements (Figure 2, 3, 4a, 5a) were performed using a Keithley 4200 semiconductor characterization system in Birck Nanotechnology Center at Purdue University. The remaining measurements were performed using an Agilient 4155C semiconductor parameter analyzer (in air ambient) and Lake Shore/Desert Cryo probe station (in vacuum) in Materials Research Laboratory at the University of Illinois. Gate leakage for the devices was at least two orders of magnitude less than the level of the drain current. As a result, measured $I_{DS}$–$V_{GS}$ characteristics were suitable for hysteresis analysis.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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