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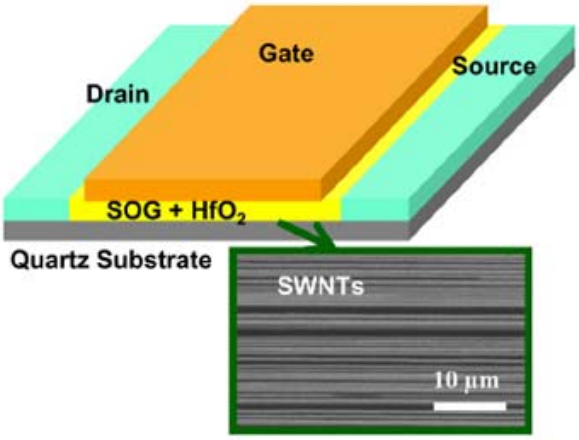
TECHNOLOGY UPDATE

Mar 30, 2012

Nanotube variations affect transistor performance

Researchers at the University of Illinois at Urbana-Champaign in the US have undertaken the first comprehensive study on how variations in the diameters and local densities of as-produced single-walled carbon nanotubes (SWCNTs) affect the performance of transistors made from arrays of these tubes. The results of the study show that the performance of the devices depends largely on how SWCNTs with varying diameters are spread throughout an array – a characteristic that could be improved on with better processes to grow and purify the nanotubes.



Aligned array of tubes

The best, and probably only, way to integrate carbon nanotubes into high-quality transistors is to use horizontal, aligned arrays of tubes, says team leader John Rogers. "Although it is now possible to grow nanotubes in exactly such configurations, nearly ideal in their layouts, there is no known way to control their diameters and local densities precisely," he told *nanotechweb.org*. "Our work describes a systematic study of how variations in diameter and local density affect the performance of transistors built from such arrays."

A single-walled carbon nanotube (SWCNT) is a sheet of carbon just one atom thick rolled up into a tube that has a diameter of about 1 nm. The atoms in the sheet are arranged in a hexagonal lattice. The relative orientation of the lattice to the axis of the tube determines whether the tube is a metal or a semiconductor and so what type of electronic properties it has.

Aligned arrays of SWCNTs are ideal for use in a variety of applications, such as high-performance sensors and transistors, thanks to their extremely high surface area and excellent charge transport properties, such as charge carrier mobilities as high as 10^4 cm^2/Vs^{-1}. However, in spite of these excellent properties, as-produced aligned arrays of SWCNTs contain a mixture of metallic and semiconducting nanotube with varying diameters and local densities (measured as the number of nanotubes per unit length perpendicular to the direction in which they are aligned). This fact leads to variations in the electronic properties across the arrays that are difficult to control.

Understanding such variations means that researchers need to make detailed measurements on the structures to locate where the non-uniformities actually lie, which is no easy task.

Experiment and theory

The work undertaken by Rogers' team combines both experiment and theory. “The experiments involve making measurements on single-tube devices as well as those built with arrays that have various numbers of tubes in different regions across a substrate, made of quartz, for example,” explained Rogers. “Then, theoretical models calibrated against the single-tube measurements are used to produce predictive tools to understand the behaviours of the array devices.”

The team measured how various performance parameters, such as drain current, transconductance and threshold voltage, varied across the devices. Deviations from theoretical values for these parameters suggested significant variations in

the SWNT density and/or diameters across the substrate. Extensive atomic force microscopy on different areas of the substrates was subsequently employed to back up these findings.

“The results could help industry better understand the kind of uniformity that is required in nanotube arrays to make high-performance transistors,” said Rogers. “Indeed, our work is funded entirely by companies interested in such applications,” he added.

The researchers are busy trying to come up with new ways to purify the nanotube arrays. “This should help reduce variations in density and diameter to levels that allow transistors to meet industry specifications.”

The work was reported in the *Journal of Applied Physics*.

About the author

Belle Dume is contributing editor at *nanotechweb.org*