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# Silicon micro-masonry using elastomeric stamps for three-dimensional microfabrication

**Hohyun Keum[1], Andrew Carlson[2], Hailong Ning[2], Agustin Mihi[2], Jeffrey D Eisenhaure[1], Paul V Braun[2], John A Rogers[2] and Seok Kim[1]**

[1] Department of Mechanical Science and Engineering, University of Illinois at Urbana-Champaign, 1206 West Green Street, Urbana, IL 61801, USA
[2] Department of Materials Science and Engineering, University of Illinois at Urbana-Champaign, 1304 West Green Street, Urbana, IL 61801, USA

E-mail: skm@illinois.edu

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**Abstract**
We present a micromanufacturing method for constructing microsystems, which we term 'micro-masonry' based on individual manipulation, influenced by strategies for deterministic materials assembly using advanced forms of transfer printing. Analogous to masonry in construction sites, micro-masonry consists of the preparation, manipulation, and binding of microscale units to assemble microcomponents and microsystems. In this paper, for the purpose of demonstration, we used microtipped elastomeric stamps as manipulators and built three dimensional silicon microstructures. Silicon units of varied shapes were fabricated in a suspended format on donors, retrieved, delivered, and placed on a target location on a receiver using microtipped stamps. Annealing of the assembled silicon units permanently bound them and completed the micro-masonry procedure.

(Some figures may appear in colour only in the online journal)

## 1. Introduction

Small-scale (<1 mm) functional structures or devices, such as the miniaturization of large-scale ordinary machines and systems, are attractive in terms of performance enhancement and manufacturing cost reduction. In the past several decades, many small-scale manufacturing methods have been developed to enable such types of miniaturization. The most versatile and commercially successful of these techniques is microelectromechanical systems (MEMS) fabrication, a process influenced heavily by integrated circuit technology [1]. For example, MEMS fabrication has been extremely popular for miniaturizing electrical and mechanical switches [2, 3], chemical and physical sensors [4, 5], displaying mirrors [6], and power generators [7]. Common components of MEMS processes include photoresist spin coating, optical lithography, physical and chemical deposition, dry and wet etching, and abrasive polishing to generate different layers and constitutive elements of the final device architecture; often many cycles of these basic processes are required to fabricate a fully functioning device [8]. Because of the repetitive nature of MEMS fabrication there are several limitations to consider: first, the process is inherently additive and subtractive from a materials perspective. Source materials are deposited everywhere on substrates and considerable amount of those are etched away to form target patterns. Second, careful planning is required since materials and structures formed early in the fabrication sequence should be protected or withstand later process conditions such as high temperature deposition, corrosive wet etching, and high vacuum environment. Third, most material deposition methods are isotropic such that planarization using chemical mechanical polishing is often necessary for subsequent lithographical patterning steps. Fourth, structures cannot be deposited in a suspended manner. Free-standing mechanical members are fabricated by removing predeposited sacrificial materials or part of substrates which exist under the members. Owing to these characteristic limitations, MEMS fabrication

 

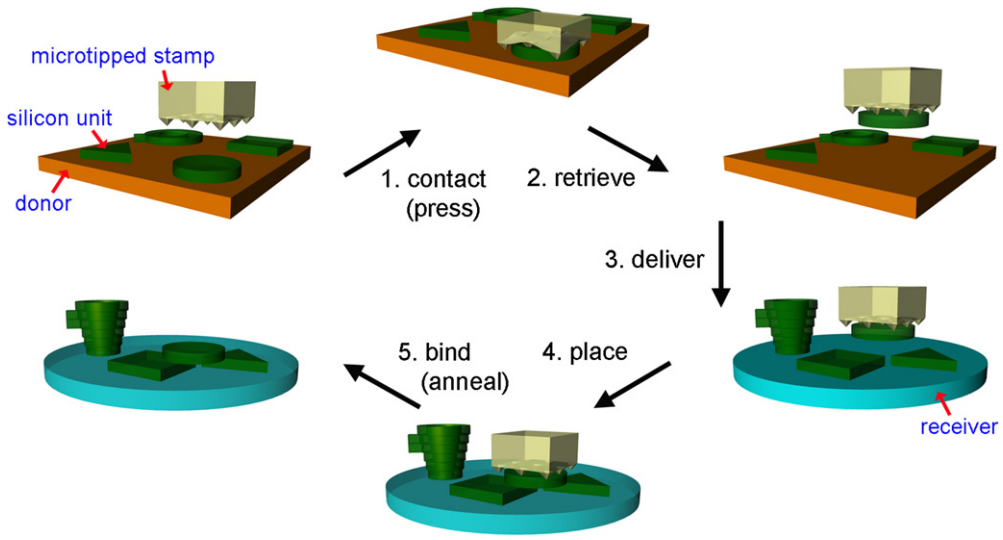


**Figure 1.** Schematic illustration of micro-masonry with silicon units using a microtipped stamp: contact between a stamp and a unit with high preload on a donor substrate; retract the stamp rapidly; move to a target; place the unit with low preload on the target; anneal the assembled units at 900 °C for 5 min.

is more complex than many typical macroscale manufacturing methods such as forming, machining, and direct assembly. Particularly, assembling three-dimensional (3D) structures and devices, while easy at the macroscale, is very challenging to achieve at the microscale using MEMS fabrication. Alternate approaches to 3D fabrication such as self-assembly [9], self-folding [10], and complex lithography [11, 12] have been developed to construct 3D microstructures. However, a direct assembly method to integrate microscale solid units, analogous to masonry in construction sites, has not been developed successfully to the best of our knowledge.

Masonry is the building of structures from individual units laid in and bound together by mortar [13]. Here, we propose a micromanufacturing strategy similar in principle to masonry and complementary to MEMS fabrication, which we term 'micro-masonry' based on individual manipulation. The term 'micro-masonry' was previously used by G Javier *et al* in 2010 [14] to describe a technique of fabricating 3-dimensional structure utilizing self-assembly. Instead, our proposed micro-masonry is defined as the full or partial fabrication of microsystems from individual microscale units deterministically manipulated and mechanically bound together. Here, the individual units can be semiconductors, dielectrics, metals, and even polymers of certain shapes. Those units are fabricated on a donor substrate, analogous to 'brick factory', in a way that makes those retrievable by an external manipulator. The manipulator repeatedly retrieves and delivers the units from the donor substrate to a target area on a receiver substrate. Finally, the placed and stacked units are mechanically or chemically bound in the final geometry.

In recent work [15], we reported elastomeric stamps having molded surface relief in the shape of pyramidal microtips that exhibited extremely high adhesion on-off switchability (>100) to transfer print thin, square silicon platelets. However, those plates were of limited thickness (<3 $\mu$m) and shape (100 by 100 $\mu$m square), had very smooth surfaces, and were assembled on the same materials. In this paper, we extend the microtipped stamp based transfer printing technique to a micromanufacturing strategy, which is 'micro-masonry'. For the purpose of demonstration, thicker (>10 $\mu$m) silicon objects having smooth as well as even rough surfaces and of arbitrary shape, such as square blocks and circular rings were used as microscale units. These silicon units were assembled not only on silicon surfaces but also on a silicon dioxide surface. Elastomeric stamps having large numbers (>100) of microtips and high temperature (∼900 °C) annealing were exploited as manipulators and a binding method, respectively. Finally, simple passive structure composed of a silicon plate with a nanostructured photonic surface supported by four silicon circular rings is demonstrated to highlight the simple fabrication technique. Reflectance characterization of the constructed photonic element shows minimal change in performance upon micro-masonry is also presented in the paper.

## 2. Micro-masonry procedure with a microtipped stamp and silicon units

Figure 1 demonstrates the typical micro-masonry procedure to assemble microscale silicon units at a target location on a receiver substrate using a microtipped stamp. The micro-masonry procedure is divided into retrieval, delivery, and binding steps which are influenced by the transfer printing process [15, 16]. The retrieval step begins with contact between a microtipped stamp and an individual silicon unit on a donor substrate with high preload. The silicon unit can be of any shape laterally but must have a flat top face. Pressing with high preload mechanically collapses the region between microtips of the stamp, maximizing the contact area and, therefore, the adhesion between the stamp and the unit. This state of the stamp is termed 'adhesion-on'. The stamp is quickly retracted to generate an even larger adhesion force against the unit owing to the viscoelastic nature of the stamp material. For sufficiently low adhesion between the unit and the donor, the unit is

effectively retrieved by the stamp. Shortly after retracting, the microtipped stamp is restored to its original geometry due to its elastic stiffness. At this moment, the adhesion of the stamp against the unit is determined by the contact area between the microtips and the flat top surface of the unit, which is extremely small, and termed the 'adhesion-off' state. Thus, the retrieval step is finished with the stamp in adhesion-off condition. Next, in the delivery step, the unit suspended on microtips is transferred and gently placed on to a target area on a receiver substrate. At this moment, the adhesion of the unit against the target surface should be larger than that of the unit against the stamp. The delivery step is completed by slowly retracting the stamp while the unit remains the target area. After retrieval and delivery steps, the assembled units are thermally annealed at 900 °C for 5 min to permanently bind them to the substrate and each other in the binding step, which ends the micro-masonry procedure.

## 3. Design and fabrication

### *3.1. Silicon units*

Microscale silicon units, retrievable from donor substrates, were fabricated from silicon-on-insulator (SOI) wafers (3, 10, 20, 50 $\mu$m thick top silicon and 1 $\mu$m buried oxide, from Ultrsil corporation) and illustrated in figures 2(*a*)–(*d*). The shape of silicon units were determined by patterning a layer of photoresist (AZ5214, 1.5 $\mu$m thick) and then etching the exposed silicon layer using reactive ion etch (RIE; Plasma-Them) or deep reactive ion etch (DRIE; STS ICP-RIE) (figure 2(*a*)). Wet etching with hydrofluoric acid (HF) removed the buried oxide to form an undercut trench below the borders of the patterned silicon units (figure 2(*b*)). Next, the wafer was spin-coated with photoresist (AZ5214) and flood-exposed to ultra-violet (UV) light (365 nm wavelength) with a dose of 150 mJ cm$^{-2}$. At this step, only the photoresist under the undercut trench was not exposed to the UV light. The wafer was immersed in a basic developer (AZ 327 MIF) removing photoresist everywhere except in the undercut regions (figure 2(*c*)). Finally, the buried oxide layer under the silicon unit, surrounded by the remaining photoresist was eliminated by HF wet etching. After the final HF etching, the silicon unit was suspended on the photoresist which tethers the unit to the underlying silicon wafer and is ready for retrieval (figure 2(*d*)). Scanning electron microscope (SEM) images of a fabricated Si unit and a remaining photoresist anchor-like structure after the Si unit retrieval are shown in figures 2(*e*), (*f*). Each image includes its magnified view of the corner in the right frame.

### *3.2. Microtipped stamps*

A microtipped stamp having 121 pyramidal microtips on a 250 $\mu$m tall, 400 $\mu$m by 400 $\mu$m square post was fabricated to manipulate the silicon units described in the previous section. The individual microtips are periodically located on the post in a square packing arrangement with predefined height and separation. For a given separation, there exists a minimum height of the microtip, $h_{\min}$, below which the elastic restoring

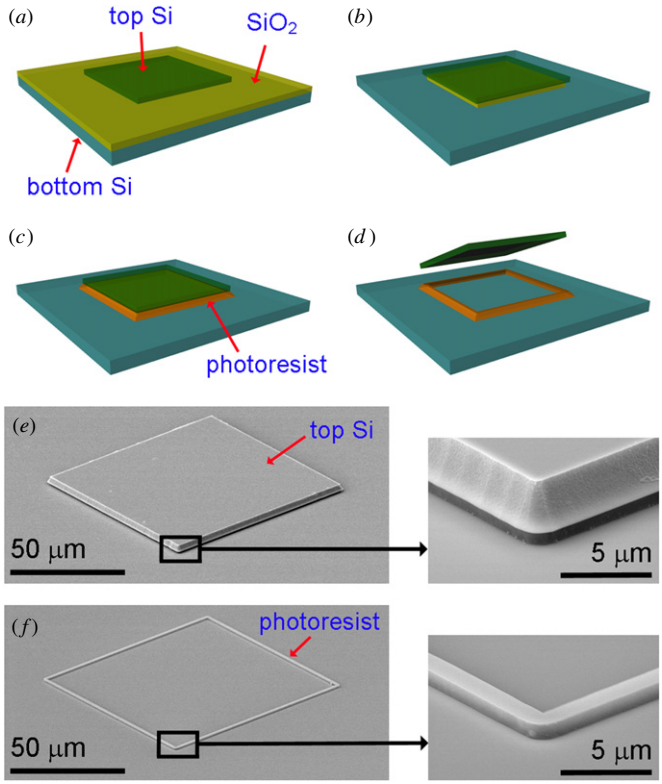


**Figure 2.** Overview of the process flow to fabricate silicon units which are ready to retrieve using microtipped stamps from a donor. (*a*) A top silicon layer is patterned on a silicon-on-insulator (SOI) wafer. (*b*) A sacrificial layer ($SiO_2$) is under-cut etched. (*c*) A photoresist is spun on the sample and flood-exposed to UV. After development, a photoresist under the top silicon remains. (*d*) The sacrificial layer is etched away and the top silicon is suspended on the photoresist and ready to retrieve. Scanning electron microscope (SEM) images of a fabricated silicon unit (*e*) and a residual photoresist after the silicon unit retrieval (*f*).

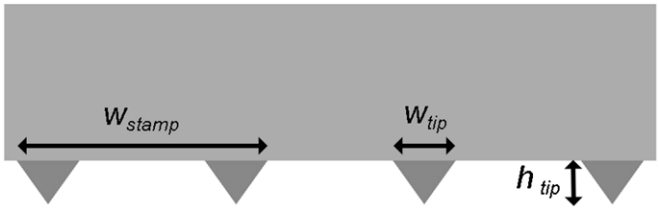


**Figure 3.** Schematic illustration showing critical microtipped stamp dimensions.

force is too small to bring the microtip back to its original geometry after mechanical collapse and retraction in the retrieval step. An optimal height for a microtip and a given separation has recently been determined as [15]:

$$h_{\min} = \sqrt{\frac{w_{\text{stamp}}\gamma}{\bar{E}}\left[3.04\ \text{In}\left(\frac{w_{\text{stamp}}\bar{E}}{\gamma\tan^2\frac{\theta}{2}}\right) - 11.5\right]} \qquad (1)$$

where $w_{\text{stamp}}$ is the microtip spacing defined schematically in figure 3. The plane-strain modulus is given as $\bar{E} = \frac{E}{(1-\nu^2)}$ of PDMS ($E = 1.8$ MPa $-$ Young's modulus [17], $\nu \approx 0.5$ $-$ Poisson's ratio), the work of adhesion between PDMS and silicon is $\gamma = 155$ mJ m$^{-2}$ [18], and $\theta$ is 90°. For $w_{\text{stamp}} = 48$ $\mu$m, equation (1) gives $h_{\min} = 6.6$ $\mu$m; our designed tips

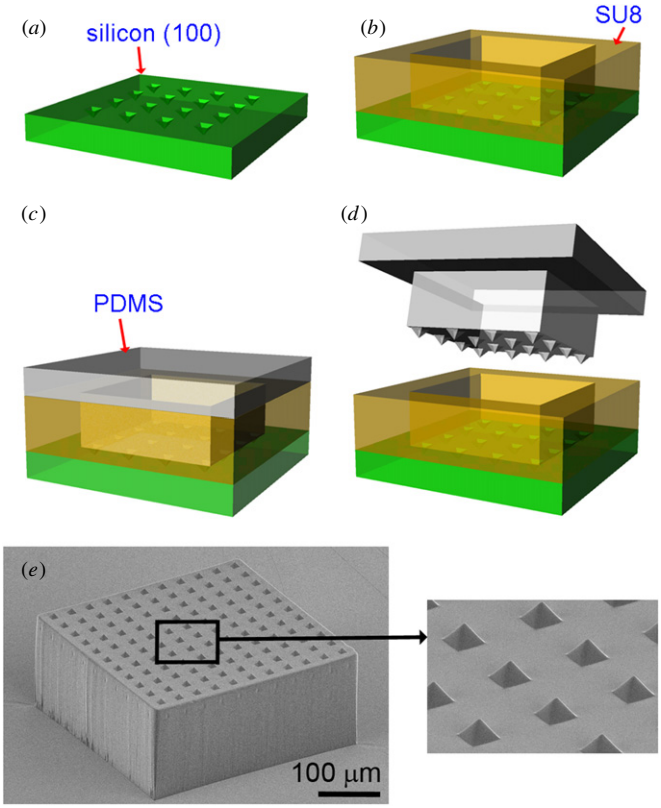


**Figure 4.** Overview of microtipped stamp fabrication process. (*a*) Formation of multiple pits using KOH etch on a silicon (100) wafer, (*b*) Photolithographical epoxy layer (SU8) pattern, (*c*) Polydimethylsiloxane (PDMS) molding, (*d*) PDMS demolding after curing. (*e*) The SEM image of a fabricated microtipped stamp with its magnified view in the right frame.

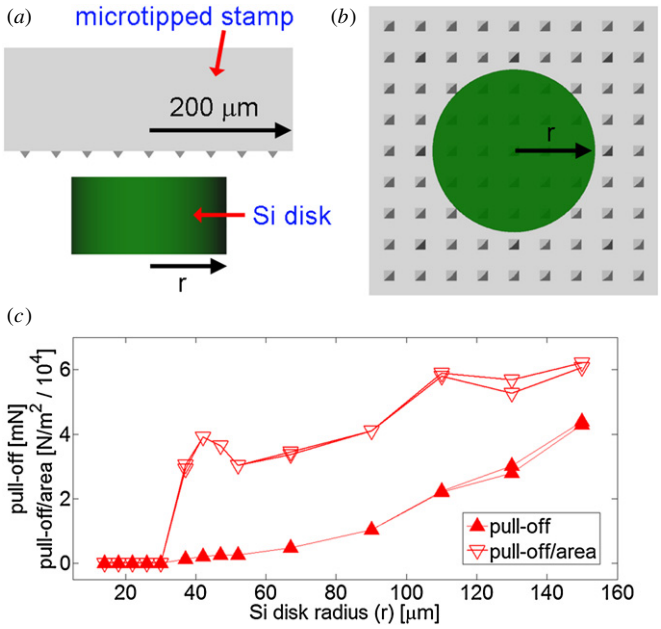


**Figure 5.** Schematic illustrations of the microtipped stamp and a contact silicon disk to measure pull-off per contact area in a profile view (*a*) and a plan view (*b*); (*c*) pull-off and pull-off per contact area of the microtipped stamp against the silicon disk as a function of the radius of the disks.

are 8.1 $\mu$m tall with 12 by 12 $\mu$m square base. It is possible to design a stamp with smaller and more numerous microtips in order to retrieve and deliver smaller silicon units; however, $w_{\text{stamp}} = 48$ $\mu$m and $w_{\text{tip}} = 12$ $\mu$m were chosen for this work since these are large enough to lithographically fabricate reliably.

To generate a microtipped stamp for this work, a molding and demolding process of polydimethylsiloxane (PDMS, Sylgard 184, Dow Corning; 5:1 mixture of base to curing agent) against negative templates was used as illustrated in figures 4(*a*)–(*d*) [15]. The negative template consists of silicon wafer (100) and an epoxy (SU8 50, MicroChem Corp., 250 $\mu$m thick) layer. The silicon wafer was anisotropically wet etched in KOH solution at 80 °C with a lithographically patterned mask of SiN (100 nm thick, formed using PECVD, PlasmaTherm) to define pyramidal pits (figure 4(*a*)). After etching the silicon wafer, the epoxy was spun and lithographically patterned to form square openings (400 × 400 mm) (figure 4(*b*)). The precursor to PDMS (base oligomer and crosslinking agent) was poured against the functionalized (trichlorosilane, United Chemical Technology) surface of this negative template and the PDMS was thermally cured (70 °C for >1 h) (figure 4(*c*)). After curing, demolding it from the negative template produces the microtipped stamp with the desired surface relief (figure 4(*d*)). The SEM image of a fabricated microtipped stamp is shown in figure 4(*e*), with its magnified view in the right frame.

## 4. Results and discussion

### *4.1. Adhesion test*

Adhesion performance of a fabricated microtipped stamp was characterized by measuring pull-off force of a stamp from a silicon surface. A custom setup described previously [15], was used to measure the stamp delamination forces with different silicon surface area. Clean, smooth, flat silicon disks with radii ranging from 14 $\mu$m to 190 $\mu$m, patterned on a silicon wafer, were connected to a precision load cell (transducer Techniques, GSO-10, ~50 $\mu$N resolution) attached to motorized rotational and $x$, $y$ translational stages. The stamp, attached to an independent vertical translational stage (Aerotech, PRO165, 500 nm resolution), was positioned over the load cell and brought into contact with the Si piece at 5 $\mu$m s$^{-1}$, held at a predefined preload for a relaxation period of 5 s, and the retracted at speed of 200 $\mu$m s$^{-1}$. While the stamp was retracted, maximum tensile forces were recorded by the load cell and chosen as the reported pull-off values. Figures 5(*a*), (*b*) depicts schematic illustration of the stamp and a silicon disk in profile and plan view, respectively.

For silicon disks with less than 30 $\mu$m radius, the stamp did not show any adhesion whereas it showed increasing pull-off for silicon disks with larger radii. For larger radius disks, pull-off per contact area ranged from 3 × 10$^4$ N m$^{-2}$ to 6 × 10$^4$ N m$^{-2}$, which varies due to the discrete position of microtips. Based on this trend found in figure 5(*c*), it was estimated that the minimum silicon unit lateral feature size,

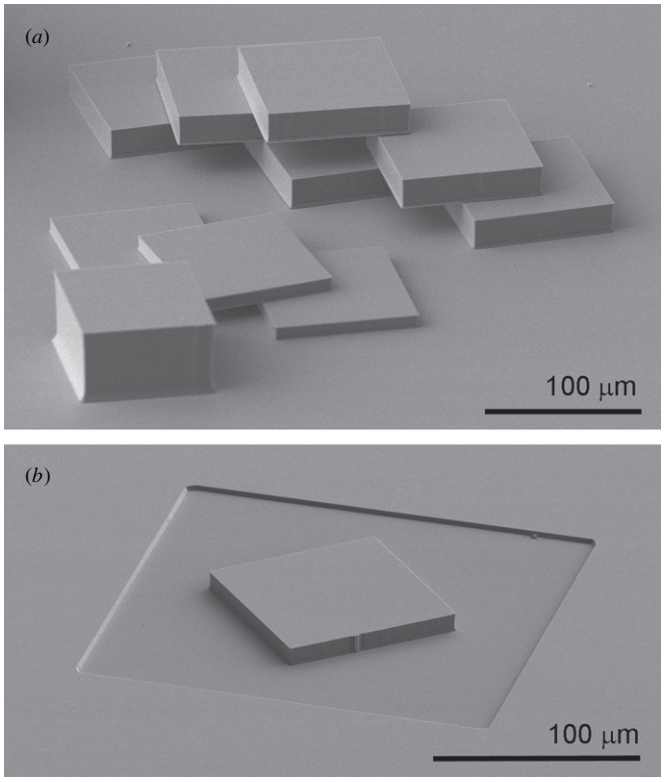


**Figure 6.** SEM images of assembled silicon blocks on a silicon wafer (*a*) and on silicon dioxide, which is defined via patterning top silicon layer of a SOI wafer (*b*). All blocks are 100 by 100 $\mu$m square laterally with varied thickness of 10, 20, 50 $\mu$m.

above which the unit is reliably retrieved using the proposed microtipped stamp, is about 30 $\mu$m or larger.

### *4.2. Three-dimensional silicon structures*

To demonstrate the microscale manufacturing capabilities of micro-masonry, we constructed several 3D silicon microstructures by assembling silicon square blocks and circular rings. As shown in figure 6(*a*), 100 by 100 $\mu$m silicon square blocks which are 10, 20 or 50 $\mu$m tall were assembled and permanently bound on a flat silicon wafer in one, two, and three layered formats. Individual silicon blocks were retrieved from donor substrates, which were made of SOI wafers with the appropriate device layer thickness. The retrieved blocks were delivered to a receiver silicon substrate and placed on target location with ~1 $\mu$m precision using manual translation and rotational stages and an optical microscope. After finishing one layer, the sample was moved to a furnace and annealed at 900 °C for 5 min to enhance the adhesion between assembled silicon units. It is discovered that this micro-masonry process was able to assemble silicon units on a silicon dioxide surface as well. Figure 6(*b*) shows a 10 $\mu$m thick, 100 by 100 $\mu$m square block placed and bound on a silicon dioxide layer which was formed by opening 3 $\mu$m thick device layer of a SOI wafer. This feature indicates that micro-masonry is not limited to semiconducting material assembly, but is accessible by other classes of materials as well.

In addition to square blocks, silicon circular rings were also assembled in a variety of unusual configurations on silicon surfaces. Figure 7 shows SEM images of five silicon annular microstructures (middle left frame) and their magnified views. Annular disks (3 $\mu$m thick) with varied diameters were retrieved and delivered repeatedly using microtipped stamps and bound together through rapid thermal annealing. In the same manner, thicker silicon rings (10 or 50 $\mu$m thick) with varied diameter were also assembled on a flat silicon wafer using the microtipped stamp to construct a teapot-like

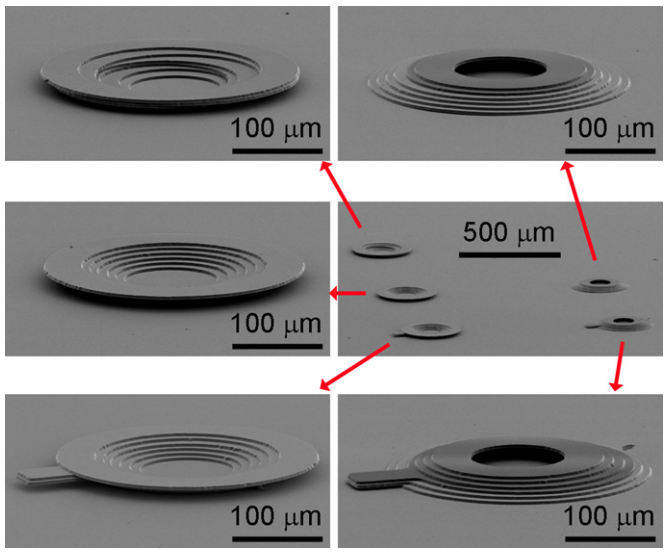


**Figure 7.** SEM images of assembled silicon rings with the thickness of 3 $\mu$m and varied diameter (from 200 $\mu$m to 300 $\mu$m) on a silicon wafer.

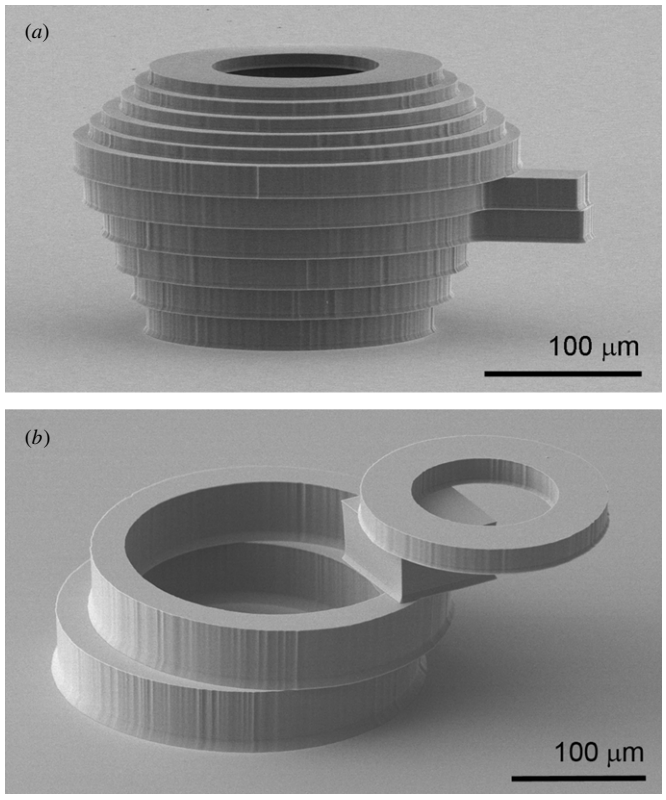


**Figure 8.** SEM images of stacked silicon rings with varied thickness (10 and 50 $\mu$m) and diameter (from 200 $\mu$m to 300 $\mu$m) (*a*), and the combination of silicon rings and a silicon square block (*b*).

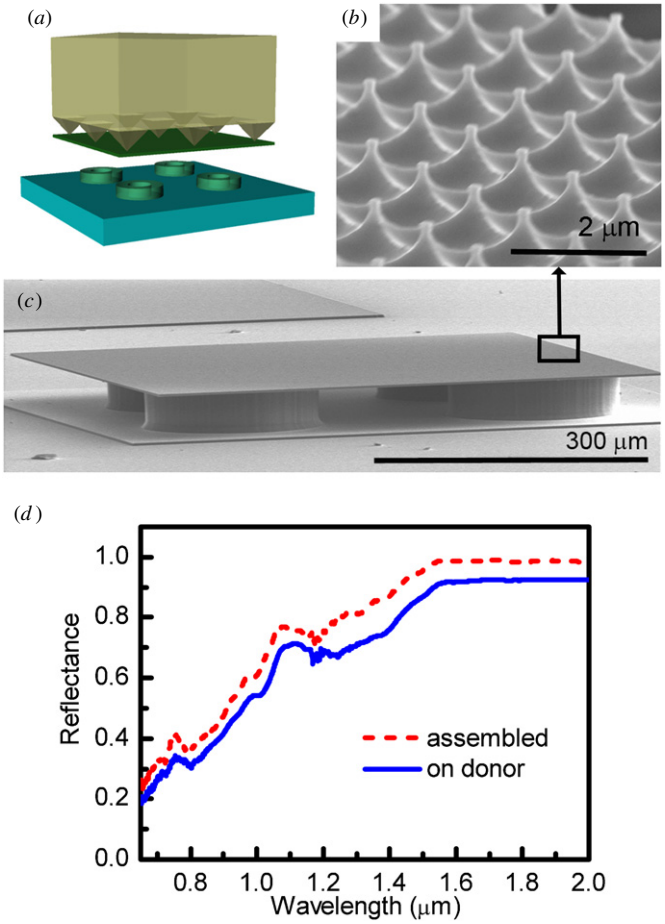


**Figure 9.** An illustration of micro-masonry of a silicon photonic surface and four silicon rings (*a*) and SEM images of the nanostructures on the photonic surface (*b*) and the assembled silicon photonic surface on four silicon rings (*c*); (*d*) Reflectance spectrum plots of the photonic surface before and after assembly.

microstructure (figure 8(*a*)). Silicon square blocks and rings were also combined and assembled together. Figure 8(*b*) shows SEM image of the combination of 20, 50 $\mu$m tall silicon rings and a 50 $\mu$m tall silicon square block.

For the demonstration of more advanced assembly, a micro-photonic table was constructed using micro-masonry. Initially, four 50 $\mu$m tall silicon rings were placed with the microtipped stamp onto silicon surface to form support structures for further assembly. Next, a 3 $\mu$m thick, 600 by 600 $\mu$m large silicon photonic surface made using a nanoimprint lithography and the procedures outlined in figure 2 was placed on the supports and bound by annealing (figure 9(*a*)). Figures 9(*b*) and (*c*) show SEM images of a magnified photonic surface and the assembled micro-photonic table. To compare optical properties of the photonic structures before and after micro-masonry, reflectance measurements were performed on two identical photonic elements: one on the donor substrate and the other on assembled silicon rings. The reflection spectra was measured by spectrometer (Bruker, Vertex 70 FTIR) coupled with a microscope (Bruker, Hyperion 1000). Both surfaces were coated with 50 nm of gold (electron beam evaporation) for two reasons: (1) the resulting periodically patterned nano-structured metal surface has a well-known surface-plasmon polaritonic (SPP) enhancement of the electromagnetic field and can facilitate optical characterization [19]; (2) the gold film can significantly prevent incident light from transmitting into the photonic structures underneath, which can complicate reflectance measurements due to Fabry–Perot interferences [20] caused by the thin-film silicon layer. As shown in figure 9(*d*), the reflectance spectra of the surfaces on donor and assembled structures present a similar trend over the entire measured wavelengths except for a small difference in reflectance values ($\sim$ 4%). The assembled SPP crystal has slightly higher reflectance because the air gap between the assembled surface and the receiver substrate introduces extra refractive index contrast and thus partially reflects the transmitted light. However, no interfacial reflection occurs in the surface on donor since both the surface and the donor substrate are made of silicon and in contact with each other. As expected, the two SPP resonance peaks, which are located at 0.75 $\mu$m and 1.1 $\mu$m in spectra respectively, had approximately the same spectral position and amplitude for both surfaces, indicating that the optical properties of the photonic structure is preserved after the micro-masonry process. Furthermore, as evidenced in this demonstration, the micro-masonry processes do not damage any delicate nanostructures on the photonic surface since the microtipped stamp was made of soft elastomer. These results also indicate that the top surface of silicon units must be flat but is not necessarily smooth for reliable retrieval and delivery steps.

## 5. Conclusion

The article reports a manufacturing route to three dimensional silicon microsystems, which we term 'micro-masonry' based on individual manipulation. The use of microstructured elastomeric stamps with high switchable adhesion strength is presented to manipulate and assemble silicon units. The high temperature annealing is utilized for the mechanical binding of assembled silicon units to complete the micro-masonry process.

This manufacturing strategy provides many attractive features such as cost-effectiveness through fabrication of highly dense individual units on a single donor substrate that can be assembled on multiple foreign substrates in a sparse manner. Its manufacturing throughput can be increased when combined with automation. Moreover, it is highly fault tolerant since one unit assembly failure does not affect other neighboring units assembly. Future opportunity includes developing microdevices using the reported micro-masonry techniques and exploring similar assembly concepts with not only silicon but also other materials including metals, dielectrics, and polymers.

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