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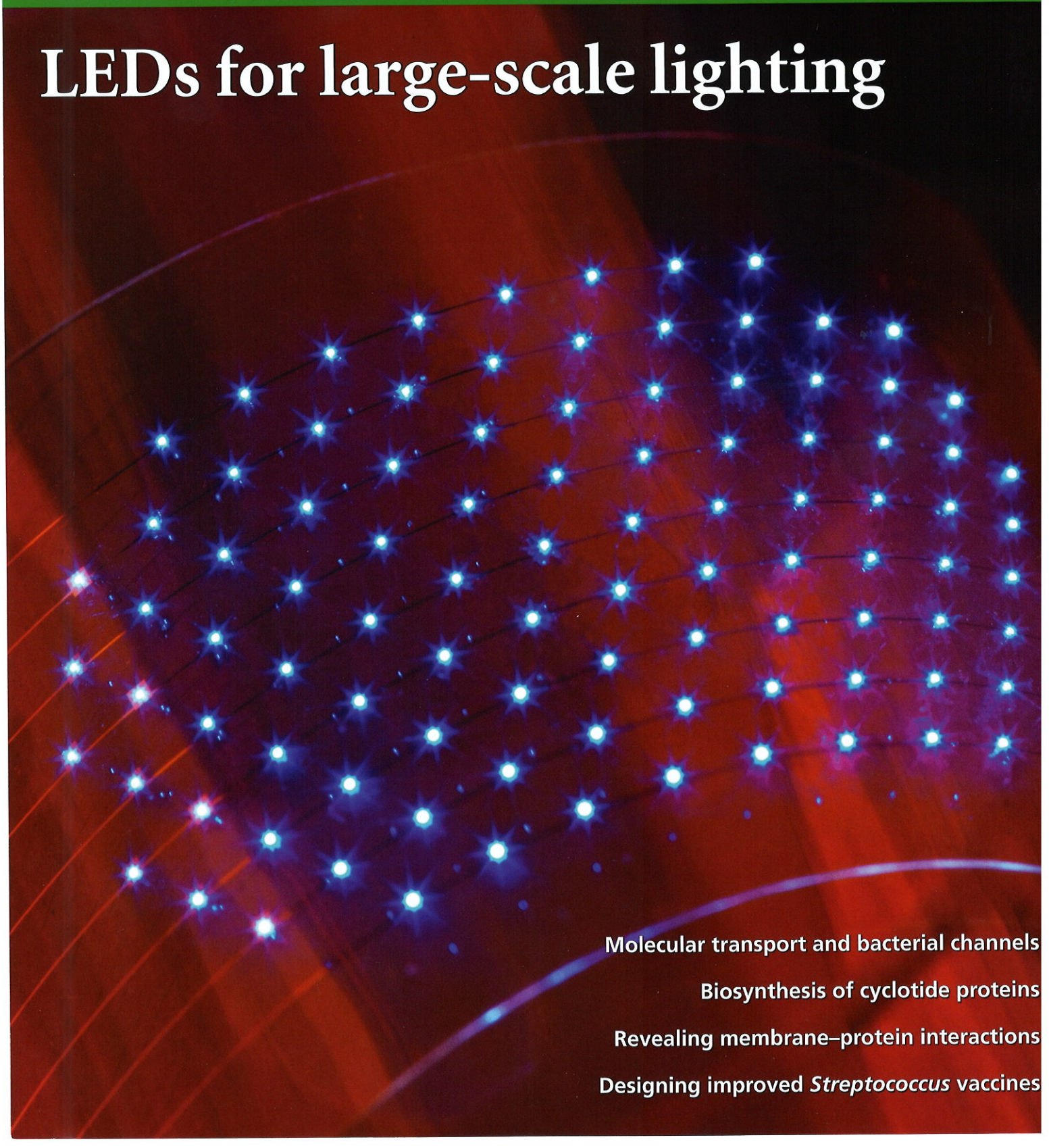
LEDs for large-scale lighting



Molecular transport and bacterial channels

Biosynthesis of cyclotide proteins

Revealing membrane–protein interactions

Designing improved *Streptococcus* vaccines

Unusual strategies for using indium gallium nitride grown on silicon (111) for solid-state lighting

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Properties that can now be achieved with advanced, blue indium gallium nitride light emitting diodes (LEDs) lead to their potential as replacements for existing infrastructure in general illumination, with important implications for efficient use of energy. Further advances in this technology will benefit from reexamination of the modes for incorporating this materials technology into lighting modules that manage light conversion, extraction, and distribution, in ways that minimize adverse thermal effects associated with operation, with packages that exploit the unique aspects of these light sources. We present here ideas in anisotropic etching, microscale device assembly/integration, and module configuration that address these challenges in unconventional ways. Various device demonstrations provide examples of the capabilities, including thin, flexible lighting "tapes" based on patterned phosphors and large collections of small light emitters on plastic substrates. Quantitative modeling and experimental evaluation of heat flow in such structures illustrates one particular, important aspect of their operation: small, distributed LEDs can be passively cooled simply by direct thermal transport through thin-film metallization used for electrical interconnect, providing an enhanced and scalable means to integrate these devices in modules for white light generation.

gallium nitride | solid-state lighting | transfer printing

Indium gallium nitride-based (InGaN) blue light emitting diodes (LEDs) hold a dominant position in the rapidly growing solid-state lighting industry (1, 2). The materials and designs for the active components of these devices are increasingly well developed due to widespread research focus on these aspects over the last one and a half decades. Internal and external quantum efficiencies of greater than 70% (3) and 60% (3), respectively, with luminous efficacies larger than 200 lm/W (4) and lifetimes of >50,000 h (5) are now possible. The efficacies (i.e., 249 lm/W), exceed those of triphosphor fluorescent lamps (i.e., 90lm/W), thereby making this technology an appealing choice for energy-efficient lighting systems (4). In particular, electricity consumption for lighting potentially could be cut in half using solid-state lighting (2). Although there remain opportunities for further improvements in these parameters, the emergence of LEDs into a ubiquitous technology for general illumination will rely critically on cost effective techniques for integrating the active materials into device packages, interconnecting them into modules, managing the accumulation of heat during their operation, and spatially homogenizing their light output at desired levels of chromaticity. Existing commercial methods use sophisticated, high-speed tools, but which are based on conceptually old procedures that exploit robotic systems to assemble material mechanically diced from a source wafer, with collections of bulk wires, lenses, and heat sinks in millimeter-scale packages, on a device-by-device basis, followed by separate steps to form integrated lighting modules (6). The intrinsic features of such processes prohibit cost competitive realization of some of the most appealing configurations of LEDs for lighting, such as those that involve large collections of ultrasmall, thin devices distributed uniformly, but sparsely, over emissive areas of large modules that could serve as direct replacements for troffers currently used in fluorescent building lights. Alternative techniques, such as those that use directed assembly of solution suspensions of LEDs, first reported nearly twenty years ago (7), appear interesting, but efforts to design commercially relevant manufacturing schemes have been unsuccessful. Here we describe a set of procedures that aims to address the limitations of existing approaches in a different way, using ideas that extend our recent work in flexible electronics (8), information display (9), and photo-voltaics (10, 11), to the area of solid-state lighting by introducing new materials, etching strategies, interconnection methods, thermal management techniques, and schemes for wavelength conversion and light distribution. The process begins with removal of InGaN epitaxial material grown on silicon wafers with (111) orientation, using lithographically defined structures and anisotropic wet chemical etching, in ways that bypass conventional laser lift-off techniques and wafer dicing. When implemented with fully formed LEDs, these ideas can be combined with deterministic assembly via transfer printing (12) to allow high-throughput manipulation of devices with geometries that are orders of magnitude smaller than those compatible with robotic pick-and-place procedures. Self-aligned techniques for thin-film metallization that exploit the large band-gap of GaN provide remarkably simple routes to interconnect large collections of devices. The outcome consists of finely distributed sources of illumination that naturally manage the thermal aspects of operation through dramatically accelerated rates for passive heat spreading, consistent with analytical models for heat flow. Laminating such systems with patterned layers of phosphors and film-type optical diffusers yields thin, flexible lighting modules whose formats make them attractive for wide ranging applications in general illumination, both conventional and unconventional.

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Results

The work focuses on model multilayer InGaN epitaxial stacks grown on Si wafers with (111) orientation (13), due to the cost and throughput advantages that are expected to result from this materials technology when optimized to offer levels of quality (e.g., threading dislocation densities $<10^9$ cm^{-2}) (13) currently available from material grown on conventional substrates such as sapphire or SiC. The layer configurations appear in Fig. S1. As illustrated in Fig. S2, lithographically patterned n-type ohmic contacts (Ti:15 nm/Al:60 nm/Mo:20 nm/Au:100 nm) (14) result from electron beam (e-beam) evaporation and rapid thermal annealing (RTA, in N_2 ambient) of metal deposited on regions of n-GaN exposed by inductively coupled plasma reactive ion etching (ICP-RIE). Similar procedures yield partially transparent p-type ohmic contacts (Ni:10 nm/Au:10 nm) to the top p-GaN layer, as shown in Fig. S3. Opaque pads (Ti:10 nm/Au:120 nm) e-beam evaporated on top of the p- and n- contacts enable single-step planarization and self-aligned passivation, using procedures outlined subsequently. Etching by ICP-RIE (i.e., mesa etch) defines the lateral dimensions of individual devices, in densely packed, arrayed layouts. Etching proceeds through the entire thickness of the InGaN material, and to a controlled depth (~1 μm) into the silicon for purposes of release described next. A representative array of such devices appears in graphic illustration in Fig. 1*A*, and in a corresponding scanning electron microscope (SEM) image in Fig. 1*C*.

The procedure for releasing these devices from the underlying substrate exploits the large differences in rates (>100×) (15, 16) for removing planes of Si(110) compared to Si(111) with wet chemical etching baths of potassium hydroxide (KOH) or tetramethylammonium hydroxide. To take advantage of this effect, the arrays are configured such that two sides of each device lie perpendicular to ⟨110⟩. The devices are tightly packed in this direction (i.e., spacing of 10 μm for this example, but with values that can be as small as 2 μm), and somewhat less so in the orthogonal direction (i.e., 40 μm shown here). Immersion in a hot, aqueous solution of KOH rapidly removes silicon along the Si (110) planes exposed by the mesa etch, thereby undercutting the devices without etching into the depth of the silicon wafer. Because the etching proceeds only along ⟨110⟩, relief structures of silicon remain in the orthogonal (⟨111⟩) direction between devices. A pair of small supporting structures (i.e., anchors) of GaN, also defined during the mesa etch, connects each of the devices to the silicon in these regions (i.e., anchor bars), to yield freely suspended configurations after the KOH etching self-terminates on the (111) planes. A graphical illustration and corresponding SEM image appear in Fig. 1 *B* and *D*, respectively. Fig. 1 *E* and *F* show magnified views of the anchor regions before and after anisotropic silicon etching. At this stage, the devices can be removed, in a nondestructive, high-speed and parallel operation, using soft stamps and the techniques of transfer printing (12). In this way, assembly into arrayed layouts on glass, plastic, or other classes of substrate can be achieved at room temperature, with throughputs of millions of devices per hour and micron-scale positioning accuracy, in deterministic and adjustable ranges of pitch (Fig. S4) (9) over areas that can be much larger than those defined by the devices on the source wafer. The SEM images of Fig. 1 *G–I* show a progression of a representative device from delineation on a donor substrate, to removal and delivery onto a receiving substrate, respectively. The LEDs formed in this manner have emission areas and thicknesses that can be up to 1,600× and 100× smaller, respectively, than conventional devices (i.e., 1×1 mm^2). For these reasons, we refer to the devices as microscale inorganic light emitting diodes (μ-ILEDs), following previous reports on different materials systems (9, 17).

The small thicknesses of μ-ILEDs make them amenable to interconnect based on thin-film metallization, to provide a high-speed, parallel alternative to traditional wire bonds. Practical

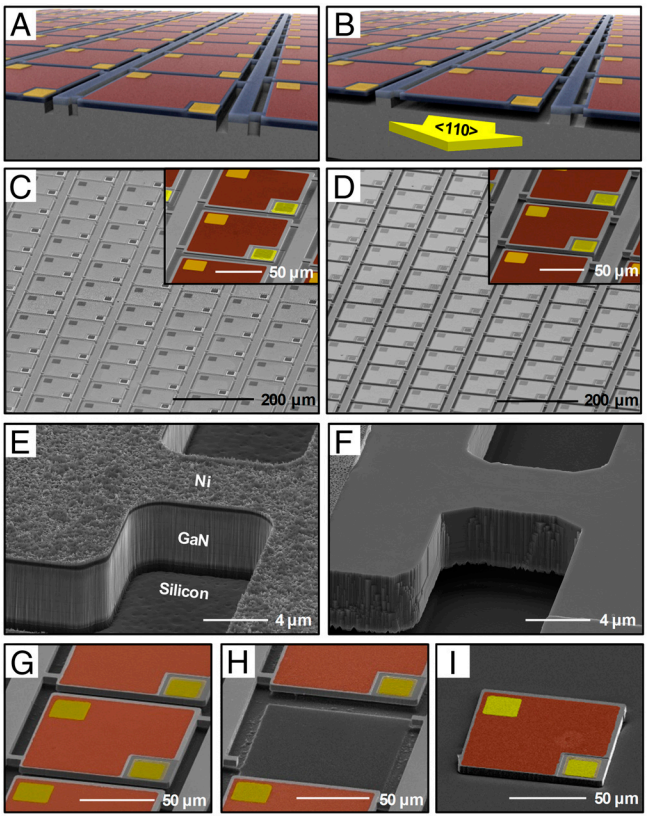

Fig. 1. Schematic illustration of arrays of InGaN μ-ILED arrays (*A*) before and (*B*) after anisotropic etching of the near-interfacial region of a supporting Si (111) wafer. The colors correspond to the InGaN (light blue), the contact pads (gold), and a thin current spreading layer (red). SEM images of a dense array of μ-ILEDs on a Si (111) wafer (*C*) before and (*D*) after this type of anisotropic etching process. The insets provide magnified views (colorized using a scheme similar to that in *A*). SEM images of the region of the μ-ILED structure that connects to the underlying silicon wafer (*E*) before and (*F*) after etching. Break-away anchors serve as fracture points during retrieval of μ-ILEDs from Si (111) wafer. SEM images of a representative μ-ILED, shown in sequence, (*G*) after undercut, (*H*) after removal from the Si wafer, and (*I*) after assembly onto a receiving substrate (colorized for ease of viewing).

challenges exist for applications in lighting, however, due to requirements on overlay and registration, especially for large area modules (i.e., troffer-scale). Fortunately, the properties of GaN devices allow a remarkably simple method for accomplishing precise registration, without the need for lithographic alignment or photo-resist processing. In this "back-side exposure" (BSE) technique, both planarization and via formation occur simultaneously in a single-step, self-aligned process. Here, the device structures themselves serve as a mask for photoinduced crosslinking of a polymer overcoat (Fig. S5). Fig. 2*A* shows an SEM image of a single 100×100 μm^2 μ-ILED printed on a glass substrate. Spin-coating a photosensitive polymer [Dow Chemical, Benzocyclobutene (BCB), Cyclotene 4024-40 Resin] fully encapsulates the device (Fig. 2*B*). H-line radiation incident on the backside of the structure passes through the transparent substrate (e.g., glass or plastic) and the GaN (band gap ≈3.4 eV), to flood expose the polymer in all regions except those shadowed by the opaque contact pads, shown in colorized gold in Fig. 2*C*. Washing away the unexposed regions leaves a pattern of polymer with openings at the contacts, and with positively sloped sidewalls for conformal deposition of interconnect metal (Fig. 2*D*). Due to the encapsulating nature of the polymer coating, requirements on registration for the interconnects are greatly relaxed compared to those for the contact pads themselves. In particular, the relevant length scale for registration decreases from roughly

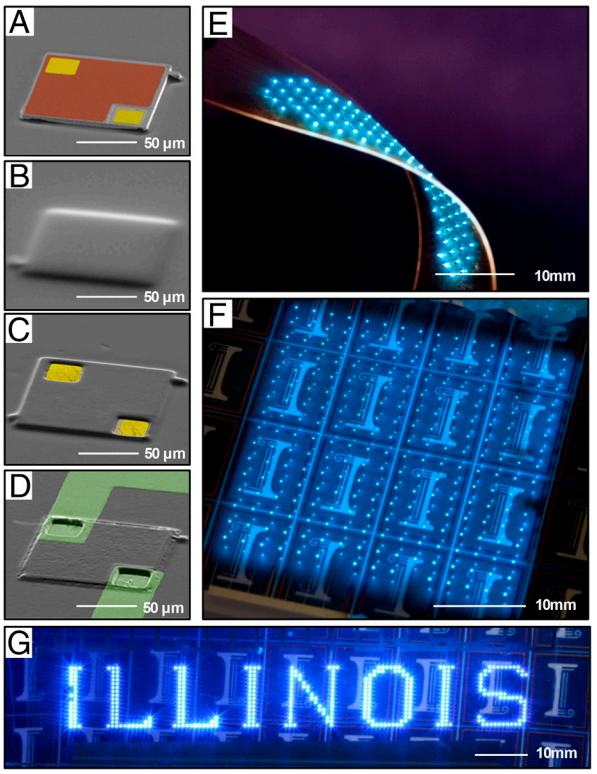

Fig. 2. SEM images of the interconnection process for a representative InGaN μ-ILED, shown in sequence, (*A*) after assembly onto a optically transparent substrate (e.g., glass or plastic), (*B*) after spin-coating a photo-sensitive polymer, (*C*) after self-aligned via formation using a BSE process, and (*D*) after deposition and patterning of a metallic interconnect layer. The colorized regions correspond to the contact pads (gold), a thin current spreading layer (red), and Al interconnects (green). Optical images of various lighting modules based on arrays of μ-ILEDs (*E*) plastic and (*F, G*) glass substrates.

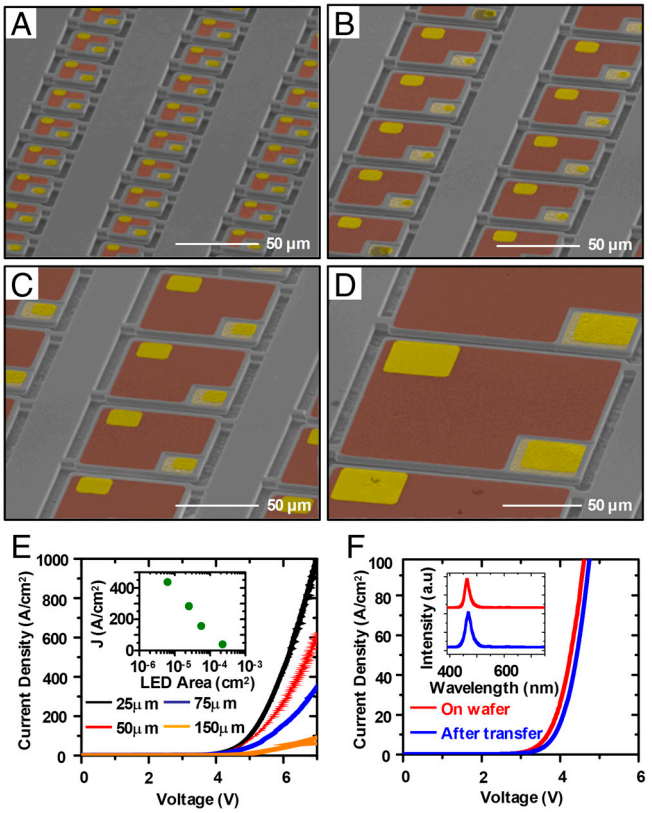

Fig. 3. SEM images of arrays of released InGaN μ-ILEDs with dimensions from (*A*) 25×25 μm^2, (*B*) 50×50 μm^2, (*C*) 75×75 μm^2 to (*D*) 150×150 μm^2. The colorized regions correspond to the contact pads (gold), and thin current spreading layers (red). (*E*) Corresponding current density-voltage (J-V) characteristics for μ-ILEDs with the dimensions shown in (*A*). The inset provides a plot of current density as a function of μ-ILED area, measured at 6 V. (*F*) Current density-voltage (J-V) characteristics and emission spectrum (inset) of a representative device before undercut etching on the Si wafer, and after assembly onto a glass substrate.

the size of a contact pad to the size of an entire device. This improvement corresponds to a factor of four for the case considered here with 25×25 μm^2 contact pads, but could be as large as a factor of 20 with 5×5 μm^2 contact pads. As shown in Fig. 2*D*, we purposefully interconnected arrays with overly wide leads (which we find easily accommodates small misalignments in the printed location of devices) by edge-over metallization, photolithographic patterning, and subsequent metal etching. This method is amenable to interconnecting large numbers of μ-ILEDs over large area arrays (e.g., 396 μ-ILEDs over ~12 cm^2 in Fig. 2*G*), shown here for arrays integrated on polyethylene terephthalate (PET) (Fig. 2*E*) and on glass (Fig. 2 *F* and *G*) substrates, and for exceptionally small devices. As an example of the latter capability, we could easily form vias of $\sim 4 \times 4$ μm^2 on devices with lateral dimensions as small as 25×25 μm^2 (Fig. S5*D*).

To illustrate the versatility, Fig. 3 *A–D* show SEM images of exemplary μ-ILEDs with various sizes from (*A*) 25×25 μm^2, (*B*) 50×50 μm^2, (*C*) 75×75 μm^2, and (*D*) 150×150 μm^2. The sizes of the smallest and largest devices are limited by the resolution in device processing (i.e., lithography and mesa etching) and by degradation of etch-resist layers during silicon etching, respectively. The current density-voltage (*J-V*) characteristics of these μ-ILEDs show a noticeable increase in *J* as the size of μ-ILEDs decreases (Fig. 3*E*). This behavior might be attributed to superior current spreading in small devices (18). The properties are unaltered by the processing, as shown in Fig. 3*F*. The small, thin geometries also provide enhanced mechanical bendability (Fig. S6) (19) and dramatically improved rates for passive thermal spreading. Both of these qualities facilitate integration with flexible sheets of plastic, as shown in Fig. 2*E*. Details related to the bending mechanics appear in the *SI Text*; the thermal properties represent a focus of the *Discussion* section.

To demonstrate integrated sources of white light that exploit these unique capabilities, we developed schemes for integrating phosphors, patterned into small tiles, with arrays of μ-ILEDs and thin-film optical diffusers. As an example, we built a flexible lighting device that incorporates an amount of active material equal to that of a single, conventional 1×1 mm^2 LED, but spread sparsely across an area of ~300 mm^2 at an areal coverage corresponding to ~0.3% to optimize the thermal and optical properties (Fig. 4, Fig. S7). The process for constructing these systems follows two parallel routes: (*i*), μ-ILED fabrication, array assembly, and interconnection as shown in Fig. S2 using a thin, PET substrate similar to the one in Fig. 2, but with interconnects patterned such that 90% of each device is covered by reflective metal (Ti:3 nm/Al:500 nm), and the remaining 10% comprises the separation of leads to the p- and n- contacts; and, (*ii*), generation of a separate, patterned array of phosphor tiles matching the spatial geometry of the printed devices, on a soft, flexible sheet of the elastomer poly(dimethylsiloxane) (PDMS). The design of this second submodule is important because it allows the use of phosphor only where required, i.e., directly above each of the μ-ILEDs in the array. A schematic representation of the processing steps appears in Fig. 4*A*. The substrate consists of a thin sheet of PDMS embossed with an array of square wells of relief. A slurry incorporating a cerium-doped yttrium aluminum garnet phosphor (Intematix, NYAG-1) in an uncured PDMS matrix uniformly

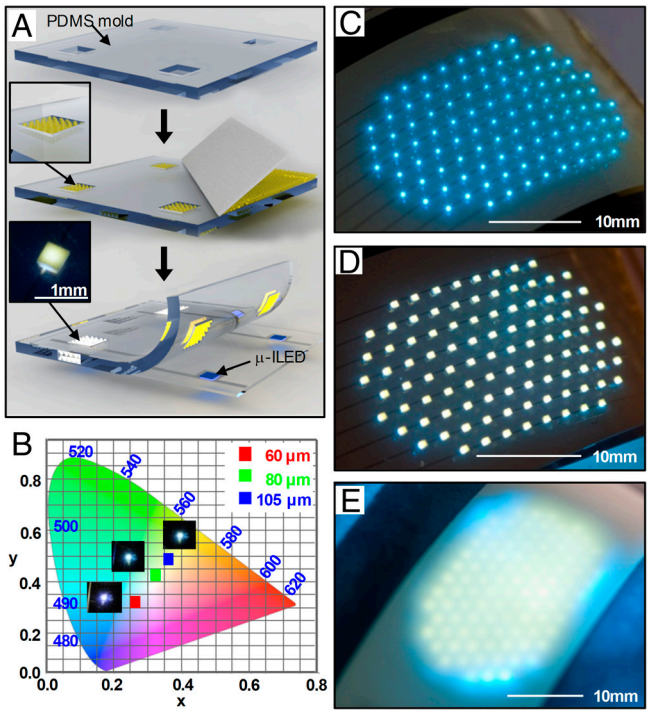

Fig. 4. (*A*) Schematic illustration of the process for fabricating flexible, white lighting modules, achieved by integrating patterned, encapsulated tiles of YAG:Ce phosphor islands with arrays of InGaN μ-ILEDs. (*B*) Color chromaticity plotted on a CIE 1931 color space diagram for μ-ILEDs integrated with phosphors with thicknesses of 60 μm, 80 μm, and 105 μm. Optical images of a fully interconnected array of μ-ILEDs (*C*) without phosphor, (*D*) with a laminated film of encapsulated YAG:Ce phosphor islands (500 × 500 μm^2), and (*E*) with a laminated diffuser film.

disperses the phosphor particles (Fig. S8), in a manner that allows their delivery to the wells using a doctor blade. Thermally curing the slurry completes this part of the fabrication process. Soft contact lamination against a patterned, interconnected array of μ-ILEDs yields white light output, with chromaticity that can be tuned by controlling the well depth using slurries at a constant phosphor-in-PDMS weight loading (37.35 wt%). Chromaticity data at different phosphor thicknesses appear in an International Commission on Illumination (CIE) 1931 color space diagram in Fig. 4*B*. As expected, the chromaticity follows an approximately linear path between the limits of the blue emission of the μ-ILED and yellow emission of the phosphor with increasing thickness. For this PDMS-phosphor composition we obtain CIE coordinates of $x = 0.321$ and $y = 0.376$ with a phosphor thickness of 80 μm.

The LED component of the system consists of 100 μ-ILEDs, each 100 × 100 μm^2, in a hexagonal array, printed with an interdevice spacing of 2 mm, set to exceed the characteristic thermal diffusion length in this system. Fig. 4 *C* and *D* shows images of the array before and after lamination against a sheet of patterned phosphor, respectively. (In this layout, the PET substrate provides a spacer between the μ-ILEDs and the phosphor tiles.) To complete the fabrication, a thin plastic diffuser film laminates onto the array to achieve diffuse, larger area emission, as in Fig. 4*E*. This sparse array of printed μ-ILEDs provides an effective illuminated area >100 times larger than the area of a traditional LED die, in a way that uses the same amount of InGaN in a configuration that has strong optical and thermal benefits.

Discussion

The thermal benefits of the type of layout in Fig. 4 are critically important, due to the adverse effects of excessive heating that can occur in devices with conventional sizes (e.g., 1 × 1 mm^2) in the absence of bulk, or miniature, heat sinking structures (20, 21). Quantitative study shows that for the sparse, μ-ILED designs, the electrical interconnects serve simultaneously as effective heat sinks. We examine the system using both analytical treatments and rigorous finite element methods (FEM) simulations. For the former, the approximately axi-symmetric nature of the system allows a precise analytical study of the thermal transport properties. The heat source is modeled as a disk with a radius r_0, and total heat generation Q, which is approximately equal to the input power to the μ-ILED that does not result in light emission (22). The temperature distribution is obtained from the steady-state heat transfer governing equation $\frac{\partial^2 T}{\partial r^2} + \frac{1}{r}\frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial z^2} = 0$ in cylindrical coordinates (r, z) (Fig. S9). The boundary conditions include the free convection $-k_m \frac{dT}{dz} = h(T - T_\infty)$ at the top (air-interconnect) surface, and constant temperature $T = T_\infty$ at the bottom (glass) surface, where h is the coefficient of natural convection. The continuity of temperature and heat flux across the interconnect-BCB interface requires $[T] = 0$ and $[k\frac{\partial T}{\partial z}] = 0$, where [] stands for the discontinuity between two adjacent layers. The above continuity conditions also hold at other interfaces. Heat generation requires $[k\frac{\partial T}{\partial z}] = \frac{Q}{\pi r_0^2}(r \le r_0)$ across the top and bottom surfaces of the μ-ILED. The interconnect surface temperature is obtained as (see *SI Text* for details)

$$T_{\text{surface}}(r) = T_\infty + \frac{Q}{2\pi r_0 k_b}\int_0^\infty [C_1(\xi) + C_2(\xi)e^{2\xi H_b}]e^{-\xi(H_b+H_m)} \times \frac{k_m}{k_m\xi + h} J_1(\xi r_0)J_0(\xi r)d\xi, \quad [1]$$

where

$$C_1(\xi) = (1 + k_b/k_m)\{[(1 + k_g/k_b) - (1 - k_g/k_b)e^{2\xi(H_L+H_g)}]\beta(\xi) + 1\},$$

$$C_2(\xi) = (1 - k_b/k_m)\{[(1 - k_g/k_b) - (1 + k_g/k_b)e^{2\xi(H_L+H_g)}]\beta(\xi) - 1\},$$

$$\beta(\xi) = (\kappa + 1)/\Big\{[(1 - k_g/k_b) - (1 + k_g/k_b)\kappa] - [(1 + k_g/k_b) - (1 - k_g/k_b)\kappa]e^{2\xi(H_L+H_g)}\Big\},$$

$$\kappa = \left[\left(1 - \frac{k_b}{k_m}\right) - \frac{k_m\xi - h}{k_m\xi + h}\left(1 + \frac{k_b}{k_m}\right)e^{-2\xi H_m}\right]e^{-2\xi H_b} \Big/ \left[\frac{k_m\xi - h}{k_m\xi + h} \times \left(1 - \frac{k_b}{k_m}\right)e^{-2\xi H_m} - \left(1 + \frac{k_b}{k_m}\right)\right],$$

with J_0 and J_1 being the Bessel functions of order 0 and 1, respectively. The operating μ-ILED temperature is given by

$$T_{\text{LED}} = T_\infty + \frac{2Q}{k_b\pi r_0^2}\int_0^\infty (1 - e^{2\xi(H_L+H_g)})\frac{\beta(\xi)}{\xi^2}J_1^2(\xi r_0)d\xi. \quad [2]$$

This analytical treatment agrees well with full three-dimensional FEM simulations as shown in Fig. S10*D*. The differences between temperatures in Eqs. **1** and **2** and FEM simulations are less than 3% for μ-ILED sizes from 10 μm to 100 μm with a 1,000 nm-thick interconnect at a power density 400 W/cm^2. The coefficient of natural convection is $h = 25$ W/m^2/°C (23). Other conditions in experiments include the surrounding temperature $T_\infty = 50$ °C, thickness and thermal conductivity $H_b =$ 1 μm, $k_b = 0.3$ W/m/°C for BCB (24); $H_g = 800$ μm, $k_g =$ 1.1 W/m/°C for glass (25); and $H_L = 5$ μm for μ-ILED. The thermal conductivity for Al interconnects is thickness dependent (26–29), and is taken as 70 W/m/°C and 160 W/m/°C for

300 nm-thick and 1,000 nm-thick interconnects, respectively. The radius of the disk heat source is $r_0 = 56$ μm to yield the same area as the square μ-ILED with dimensions of 100×100 μm^2.

The left and right frames of Fig. 5 *A–D* show a set of experiments involving infrared thermal imaging of temperature distributions (QFI Infra-Scope Micro-Thermal Imager) and analytical predictions, respectively. These experiments compare surface temperatures for cases of Al interconnects with thicknesses of 300 nm and 1,000 nm (Fig. 5 *A–B* for 300 nm and Fig. 5 *C–D* for 1,000 nm), for input power ranging from 7.8 mW to 43.2 mW (i.e., power density ranging from 78 W/cm^2 to 432 W/cm^2). Fig. 5*E* presents surface temperatures as a function of power, where analytical model results (lines) agree very well the experimental measurements (symbols) for devices with these two interconnect thicknesses.

The results of Fig. 5 *A–E* clearly show pronounced decreases in the temperatures with thicker Al interconnects, thereby demonstrating that the interconnects themselves serve a dual role as efficient heat sinks by accelerating the rates of lateral thermal diffusion. These effects can be attributed predominantly to the significant thermal mass of the interconnects compared to the μ-ILEDs, and to their higher thermal conductivities. As a consequence, both the thickness of the interconnects and the size of the devices are important. A theoretical parametric study, summarized in Fig. 5*F*, shows the surface temperatures at a constant heat flux density of 400 W/cm^2, as a function of these two variables. Clearly, the temperature can be greatly reduced by decreasing the sizes of the LEDs and by increasing the thicknesses of the interconnects. As a particular example, consider a conventional, macrosize LED (i.e., 1×1 mm^2) and an array of 100 μ-ILEDs (i.e., 100×100 μm^2) at a spacing of 2 mm on otherwise identical platforms, both at total input power densities of 400 W/cm^2. The method of superposition is used to determine the temperature of μ-ILED arrays based on the solution for a single LED, i.e., $T_{\text{array}}(r,z) = T_\infty + \sum_i [T_i(r,z) - T_\infty]$, where $T_i(r,z)$ is the temperature distribution due to *i*th μ-ILED. The surface temperature distributions for a macrosize LED and μ-ILED array with spacing 2 mm are shown in Fig. 5 *G* and *H*, respectively. The maximum temperature occurs at the center of the array and it decreases with increasing spacing (Fig. 5*I*). The conventional LED would reach a temperature of over 1,000 °C whereas the array of μ-ILEDs would operate at ~100 °C (Fig. S10*D*). In real devices, the conventional LED would be completely destroyed under these conditions, thereby motivating the requirement for advanced heat sinking structures of the type that are presently in use commercially. By contrast, the μ-ILEDs experience temperatures that enable stable operation, without any additional components.

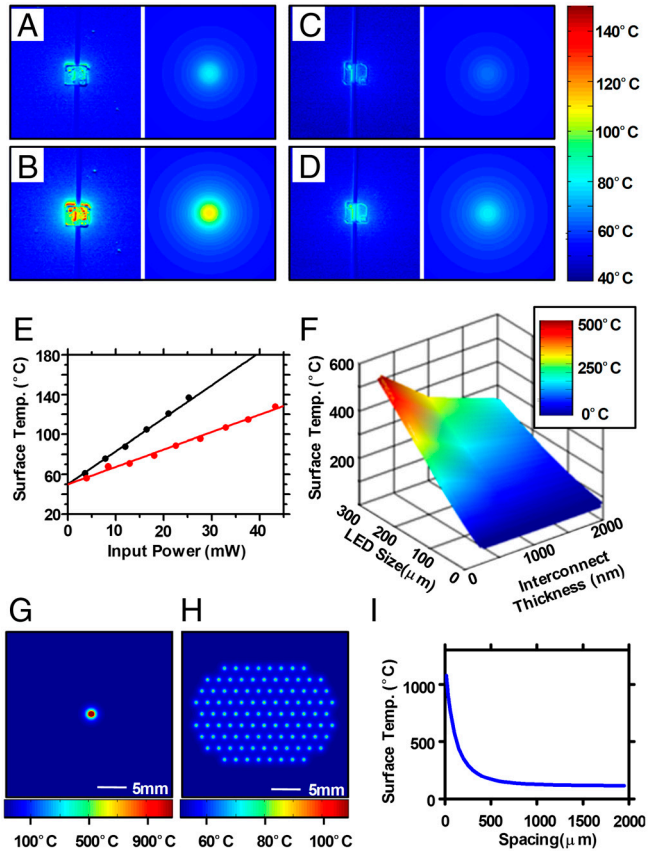

Fig. 5. (*A–D*) Temperature distributions for isolated InGaN μ-ILEDs with Al interconnects [300 nm and 1,000 nm-thick for (*A–B*) and (*C–D*), respectively] at input powers of (*A*) 7.8 mW, (*B*) 16.4 mW, (*C*) 8.4 mW, and (*D*) 18.0 mW captured using a QFI Infra-Scope Micro-Thermal Imager (left) and calculated by analytical models (right). (*E*) Surface temperature for μ-ILEDs with Al interconnect thicknesses of 300 nm (black) and 1,000 nm (red) extracted from experiments (dots) and computed using the analytical model (lines) as a function of input power. (*F*) Three-dimensional plot of the surface temperature as function of device size and interconnect thickness, at a constant heat flux of 400 W/cm^2. Temperature distribution for (*G*) a macrosize LED (i.e., 1×1 mm^2), and (*H*) an array of 100 μ-ILEDs (i.e., 100×100 μm^2) at a spacing of 2 mm. (*I*) μ-ILEDs surface temperature vs. spacing for an array of 100 μ-ILEDs.

Conclusions

The strategies reported here incorporate advanced ideas in etching to release thin devices, self-aligned photoexposures to form metal features that serve simultaneously as electrical interconnects and thermal heat spreaders, and module designs that include thin, patterned phosphors with film diffusers. This collection of procedures, combined with analytical models of heat flow, create new design opportunities in solid-state lighting. Although all of these processes were combined to yield integrated systems, each can be implemented separately and matched to existing techniques for certain steps, to add new capabilities to otherwise conventional module designs. For example, the same concepts can be applied to active materials derived from epitaxial growth on sapphire substrates. These and other possibilities might represent interesting directions for future work.

Materials and Methods

Fabrication of GaN μ-ILEDs. A GaN/Si(111) wafer (Azzurro Semiconductor) with layers of GaN:Mg (110 nm), five repeats of InGaN/GaN:Si (3 nm:10 nm), GaN:Si (1,700 nm), AlN:Si/GaN:Si (1,900 nm), GaN (750 nm), and AlN/AlGaN (300 nm) served as the starting material. Multiple metal layers (Ti:15 nm/Al:60 nm/Mo:20 nm/Au:100 nm) are deposited via e-beam evaporator on regions of n-GaN exposed by ICP-RIE etching and annealed at 860 °C for 30 s in N_2 ambient to form n-type ohmic contact to GaN:Si layer. For p-type ohmic contact to GaN:Mg layer, metal layers (Ni:10 nm/Au:10 nm) are deposited via e-beam evaporator and annealed at 500 °C for 10 min in air ambient. Next, opaque contact pads are formed by e-beam evaporation (Ti:10 nm/Au:120 nm). As a resist for KOH attack on ohmic contacts, a 300 nm layer of silicon nitride was deposited by plasma enhanced chemical vapor deposition. The geometry of the device array was photo-lithographically defined by patterning a metal etch mask of metal (Ti:50 nm/Ni:450 nm) by photoresist lift-off process then removing the exposed silicon nitride by RIE with SF_6. An ICP-RIE step provided the mesa etch, to generate an isolated array of devices. Anisotropic undercut etching of the silicon was performed by complete immersion in a solution of KOH (PSE-200, Transene) at 100 °C (hot plate temperature).

Fabrication of Arrays of InGaN μ-ILEDs. Devices were transfer printed from the source wafer to a target substrate, using procedures described elsewhere. BSE was performed by spin-casting and prebaking a layer of benzocyclobutene (Cyclotene 4024-40 Resin, 2,000 rpm for 60 sec, 80 °C for 2 min). Samples were inverted, placed on a Cr-coated glass slide, exposed under a MJB3 Mask Aligner (Karl Suss), then developed (DS2100). After curing (210 °C for 60 min in O_2-free environment), interconnect metal (Ti/Al in desired thickness) was sputtered and patterned by photolithography and metal etching [Ti-6:1 BOE, Al-Al Etchant Type A (Transene)].

Fabrication of Thin, Flexible, White Light Modules. Fabricating supports for the phosphor involved casting and curing PDMS (10:1 mixture of base to curing agent) against a functionalized silicon wafer (trichlorosilane, United Chemical Technologies) with a photodefined set of structures of epoxy (SU-8 50, MicroChem Corp.) with desired thicknesses. Peeling away the cured PDMS yielded an array of relief features (500×500 μm^2) matching the spatial geometry of interconnected μ-ILEDs. Phosphor islands were created by scraping a PDMS-based slurry of phosphor (NYAG-1, Intematix, created by mixing with uncured PDMS) across the PDMS substrate using a doctor-blade type implement consisting of a PDMS-coated razor blade. Thermal curing (70 °C for >3 h) completed the process. The phosphor mold was manually aligned and laminated to a matching array of μ-ILEDs. The module was completed by bonding an optical diffuser film (AX27425, Anchor Optics) to the phosphor mold.

Characterization of Electrical, Optical, Mechanical, and Thermal Properties. Electrical measurements were performed with a semiconductor parameter analyzer (4155C, Agilent or 2400 Sourcemeter, Keithley). Optical measurements of the emission spectra were performed with a high resolution spectrometer (HR4000, Ocean Optics). Color chromaticity was determined using SpectraSuite (Ocean Optics) with a radiometric calibration source (HL-2000, Mikropack) and an Ocean Optics spectrometer optical fiber in a fixed location, ~1 mm, above the sample. Bending measurements involved determining the forward voltage needed to produce 10 mA current with the sample mounted on cylindrical tubes with various radii, ranging from 5.9 mm to 65.3 mm. Fatigue measurements were performed by repeatedly bending the specimen from a flat state to the bent state with a bending radius of 5.9 mm. Thermal measurements of the surface temperature of μ-ILEDs were performed using MWIR-based InSb thermal imager (InfraScope, QFI) with the base temperature of 50 °C.

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Supporting Information

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SI Text

Stack Design of InGaN/GaN Multiple Quantum Well (MQW) LED on Si(111) Substrate. Fig. S1 shows a schematic illustration of the epitaxial semiconductor multilayer stack of InGaN MQW LED on a Si(111) wafer. Active layers consist of a Si-doped n-GaN layer with a thickness of 1,700 nm, 5 layers of multiquantum well (MQW) of 3 nm InGaN and 10 nm of Si-doped GaN capped with Mg-doped p-GaN layer with a thickness of 110 nm. This wafer was purchased from Azzurro Semiconductor in Germany.

Fabrication Process of InGaN/GaN MQW μ-ILEDs on Flexible Substrates. Fig. S2 shows a schematic overview of the fabrication process. The process starts with InGaN epitaxial layers grown on Si (111) wafer, as illustrated in Fig. S1. For photolithography, photo-resist AZ5214-E was used as both a positive tone and negative tone resist. The steps for photolithography with this material appear below.

Photolithography using AZ5214-E as a positive-tone resist.

Spin-coat at 4,000 rpm for 30 s.
Prebake at 110 °C for 60 s.
Exposure dose of 78.5 mJ/cm^2 at 365 nm.
Develop in metal ion free (MIF) 327 for 35 s.
Hard bake at 130 °C for 180 s.
O_2 descuum for 45 s in 250 mTorr, 20 sccm of O_2 under 50 W.

Photolithography using AZ5214-E as a negative tone resist (image reversal).

Spin-coat at 5,000 rpm for 30 s.
Prebake at 110 °C for 60 s.
Exposure dose of 110 mJ/cm^2 at 320 nm
Postexposure bake (PEB) at 110 °C for 65 s.
Flood UV exposure of 400 mJ/cm^2.
Develop in MIF 327 for 35 s. More negatively sloped sidewalls can be achieved for easy lift-off if developed in MIF 327 for longer time (i.e., additional $10 \sim 15$ s).
O_2 descuum for 45 s in 250 mTorr, 20 sccm of O_2 under 50 W.

N-ohmic contact recession. P-GaN and MQW layers must be etched in the region where n-ohmic contacts are to be formed. First, n-ohmic contact regions are photo-lithographically defined using AZ positive-tone process (see *Photolithography using AZ5214-E as a positive tone resist*). Etching the GaN can be achieved using inductively coupled plasma reactive ion etching (ICP-RIE) with BCl_3 and Cl_2 gases, with pressures of 3 mTorr and temperatures of 25 °C. A two-step etching process was employed. The first step consisted of 15 sccm of BCl_3 with radio frequency (RF) power of 300 W and parallel plate DC voltage of 100 V for 90 s. The second step consisted of 15 sccm of Cl_2 gas with RF power of 300 W and parallel plate DC voltage of 100 V for an additional 120 s. An etch depth of 350 nm to 400 nm can be achieved with this recipe. After the ICP-RIE etching of GaN, the photo-resist (PR) was removed using acetone in an ultrasonic bath for about 120 s. The total etching depth was about 350 nm to 400 nm, as measured using profilometry.

N-ohmic contact deposition and annealing. Image Reversal of AZ5214-E [see *Photolithography using AZ5214-E as a negative tone resist (Image Reversal)*] and lift-off process were used to define n-ohmic contact metal. The native oxide on the surface n-GaN was removed using Buffered Oxide Etchant at a 10:1 mixing ratio for 120 s prior to metal deposition. (Ti:15 nm)/(Al:60 nm)/(Mo:20 nm)/(Au:100 nm) were evaporated at base pressures of 8×10^{-7} Torr as ohmic contacts to the n-GaN. An AG Associates Heatpulse 610 rapid thermal processor was used for rapid thermal annealing at 860 °C for 30 s under N_2 environment. Ohmic contact characteristics of Ti/Al/Mo/Au on n-GaN surface are described elsewhere (1).

P-ohmic contact deposition and annealing. Image reversal with AZ5214-E [see *Photolithography using AZ5214-E as a negative tone resist (Image Reversal)*] was used to define the p-ohmic contact regions. Immersion of p-GaN in HCl:DI = 3:1 for 5 min removed the native oxide. Ni (10 nm)/Au (10 nm) layers were deposited in an e-beam evaporator at a base pressure of $<5 \times 10^{-7}$ Torr at a relatively slow rate (approximately 0.5 A/s). After deposition, PR was removed using acetone in an ultrasonic bath for 120 s, and then Ni/Au layers were annealed in a furnace at 500 °C for 10 min in air (80% N_2 + 20% O_2) to improve the ohmic properties. Ohmic contact characteristics are depicted in Fig. S3.

Opaque contact pad. Image reversal with AZ5214-E [see *Photolithography using AZ5214-E as a negative tone resist (Image Reversal)*] was used to define the opaque contact pad regions on both p-ohmic contact region and n-ohmic contact region. Opaque contact pads served not only as contact electrodes, but also as mask patterns for the self-aligned passivation process, as illustrated in Fig. S5. As an opaque contact pad, Ti(10 nm)/Au(120 nm) was deposited using an e-beam evaporator. After deposition, PR was removed using acetone in an ultrasonic bath for 120 s.

SiN passivation layer deposition condition. SiN, which served as an etch barrier during the KOH undercut process, was deposited using an STS Multiplex plasma enhanced chemical vapor deposition (PECVD) system. Three hundred nm of SiN film was deposited at a pressure of 650 mTorr, temperature of 300 °C, and gas flow rates of 1,960 sccm (N_2) + 40 sccm (SiH_4) + 35 sccm (NH_3). Mixed frequency RF power of 20 W, with frequencies of 13.5 6 MHz for 6 s and 380 KHz for 2 s was used.

Ni etch mask deposition. On top of SiN film, AZ5214-E was used in an image reversal mode [see *Photolithography using AZ5214-E as a negative tone resist (Image Reversal)*] to define the lateral dimensions of the μ-ILEDs and the geometries of the anchors. Ti(50 nm)/Ni(450 nm) was deposited using an e-beam evaporator at relatively high deposition rate of approximately 6 A/s to minimize the thermal stress caused by the heating inside the chamber. After the deposition, PR was removed using acetone in an ultrasonic bath for 60 s.

SiN + GaN dry etching. SiN was dry-etched using a parallel plate RIE (Unaxis/Plasma Therm) with 40 sccm of SF_6, 35 mTorr pressure, and 100 W RF power, for an etch rate of SiN of ~100 nm/min. Upon the removal of SiN, GaN/InGaN/AlN/AlGaN epi-layers were all etched with a gas combination of $BCl_3/Cl_2/Ar$ in inductively coupled plasma reactive ion etching (ICP-RIE, Plasma Therm SLR770). Two etching steps were

incorporated in etching GaN/AlN based epitaxial layers, as in the following.

GaN etching step 1 in ICP-RIE.

Pressure: 5 mTorr.
Temperature: 25 °C.
Gas: 10 sccm of BCl_3 + 16 sccm of Cl_2 + 4 sccm of Ar.
ICP Coil power of 500 W and parallel plate voltage of 300 V.
Etching time: 1 min.

GaN etching step 2 in ICP-RIE.

Pressure: 5 mTorr.
Temperature of 25 °C.
Gas: 20 sccm of Cl_2 + 4 sccm of Ar.
ICP Coil RF power of 500 W and parallel plate voltage of 260 V.
Etching time: 8 additional min.

Anisotropic etching of silicon using KOH (Transene PSE-200).

Hot plate temperature: 100 °C.
Etching time: 45 min for a 100×100 μm^2 device.

Ti/Ni, SiN removal.

Ni etchant: (Transene TFB).
Etch rate: 3 nm/s at 25 °C.
SiN is dry etched using conditions described above.

Transfer-printing. Transfer-printing of μ-ILEDs was carried out onto either glass or PET substrates. Glass substrates were prepared by cleaving a slide into appropriate dimensions. PET substrates were prepared by spinning uncured poly(dimethylsiloxane) (PDMS) (10:1 mixture of base to curing agent) on a glass slide cleaved to appropriate dimensions at 2,000 rpm for 30 s. The PET film (Dura-Lar, Grafix) was laminated to the uncured PDMS and the entire substrate was cured at 70 °C for 3 h. A thin-film adhesive was spin-coated onto the secondary substrate after O_2 plasma at 3,000 rpm for 30 s and soft-baked at 110 °C for 10 min. Transfer-printing of μ-ILEDs was carried out in automated printer system using PDMS as a stamp. Step and repeat printing allowed formation of arrays with arbitrary configurations. The thin-film adhesive was cured under UV light for 10 min.

Self-aligned passivation by Back-side Exposure (BSE).

Adhesion promoter (AP3000) is spin-coated at 2,000 rpm for 30 s.
Soft-baking at 80 °C for 30 s.
BCB (Cyclotene 4024-40, Dow) is spin-coated at 2,000 rpm for 60 s.
Prebaking at 80 °C for 120 s.
Flood exposure dose from the back side of 123 mJ/cm^2 at 405 nm.
Postexposure baking (PEB) at 70 °C for 30 s.
Develop in DS2100 for 70 s.
Curing of BCB is carried out in oxygen-free environment at 210 °C for 60 min.
Descuum process using RIE at the pressure of 200 mTorr with 18 sccm of O_2 with 2 sccm of CF_4 with 150 W RF power for 30 s.

Metallization. Sputtered or e-beam evaporated Al was used for reflective interconnection. Aluminum was deposited and patterned photo-lithographically using AZ5214-E and an etch-back process (Type A, Transene). Fully interconnected arrays of μ-ILED resulted from this metallization process.

Ohmic Contact Characterization of Ni/Au Layers to p-GaN. Fig. S3 illustrates the ohmic contact characteristics of Ni(10 nm)/Au (10 nm) to p-GaN. Fig. S3*A* shows the current-voltage characteristics of Ni/Au contact to p-GaN with TLM pad spacings of 21 μm in three different annealing conditions (i.e., As deposited, 5 min annealing, 10 min annealing, and 15 min annealing). Fig. S3*B* shows a plot of total resistance at four different pad spacing ranging from 2.5 μm to 17 μm. The specific contact resistance could not be extracted due to the large sheet resistance associated with the highly resistive p-GaN. It is, however, qualitatively shown that 10 min annealing at 500 °C exhibits better ohmic characteristic than 15 min or 5 min annealing cases at the same temperature.

Versatility of Transfer-Printing Process. The versatility of the transfer-printing process is shown in Fig. S4 via corresponding SEM images of (*A*) after KOH undercut and (*B*) after transfer-printing. In Fig. S4*C*, μ-ILEDs are transfer-printed onto a glass substrate with varying pitches ranging from 25 μm to 500 μm.

Schematic for Passivation and Via Formation Using BSE Process. In Fig. S5*A*, a schematic illustration of an unusual passivation scheme using BSE process is shown. The self-aligned passivation starts with a transparent substrate such as a glass or a plastic. A transfer-printed μ-ILED exhibits transparency in wavelengths above its band-gap. First, a photosensitive polymer with a significant sensitivity (absorption) in the wavelength regime higher than the corresponding wavelength of the band-gap of GaN (~365 nm) is applied (e.g., by spin-coating) on the surface of printed μ-ILEDs. The polymer can effectively be crosslinked by the irradiation through the GaN and the substrate. The opaque contact pads serve as a masking layer. Corresponding SEM images of μ-ILEDs are shown in Fig. S5 *B* and *C* with 100× 100 μm^2 device and in Fig. S5*D* with 25×25 μm^2 device after the BSE process. Cross-sectional profiles of a passivated μ-ILED (acquired using profilometry) are shown in Fig. S5*E*. This process naturally generates vias with positive sidewall.

Uniformity in Electrical Properties of μ-ILED on Mechanical Deformation. Fig. S6 *A* and *B* show electrical properties (I–V characteristics and forward voltage at 10 mA of current) for representative μ-ILEDs printed on a PET substrate measured for varying bending radii and repetitive cycles. These I–V data demonstrate that the μ-ILEDs do not change in an appreciable way to bending radii down to ~5.9 mm and up to 1,000 bending cycles. For this specific substrate configuration, these results indicate robust operation of the devices to strains up to 0.18%.

Uniformity in Electrical Properties of μ-ILED in an Array. Current-voltage characteristics of 100 μ-ILEDs from an array, shown in Fig. S7*A*, exhibit excellent uniformity. For example, less than 100 mV difference in the forward voltage is shown at 3 mA current. An array consists of 100 μ-ILEDs in a hexagonal arrangement (e.g., equal spacing between all μ-ILEDs) are shown in Fig. S7*B*.

Integration YAG:Ce Phosphors with μ-ILED in an Array. Phosphors must be dispersed uniformly to generate uniform white light. Fig. S8*A* shows optical microscope images of relief features filled with a PDMS/phosphor slurry (left column) and filled with the phosphor powder only (right column). Compared to the "dry filling" method, the PDMS/phosphor slurry provides excellent dispersion and uniformity of phosphor in the PDMS matrix. Emission spectra of white μ-ILEDs are shown in Fig. S8*B* with phosphor layer thicknesses of 60 μm, 80 μm, and 105 μm.

Fabricating SU-8 mold for phosphor-island mold.

Spin-coat SU-8 5 on Si(100) wafer 1,800 rpm for 30 sec.

Bake at 95 °C for 5 min.
Flood exposure dose of 216 mJ/cm^2 at 365 nm.
Spin SU-8 50 and expose.

For 60 μm film: Spin 1,800 rpm for 30 sec, Exposure dose of 432 mJ/cm^2 at 365 nm.
For 80 μm film: 1,600 rpm for 30 sec, Exposure dose of 513 mJ/cm^2 at 365 nm.
For 105 μm film: 1,250 rpm for 30 sec, Exposure dose of 583 mJ/cm^2 at 365 nm.
Bake at 65 °C for 1 min then ramp to 95 °C, total bake time 11 min.
Develop in SU-8 Developer 12 min.
Bake 180 °C for 10 min.
UVO treatment for 2 min.
Treat with tridecafluoro-1,1,2,2-tetrahydrooctyl trichlorosilane for 2 h in air-tight container.

Creating white light, μ-ILED.

Cast 10 : 1 mixture (base to curing agent) of uncured PDMS over SU-8 master.
Cure at 70 °C for 3 h.
Create phosphor/PDMS slurry: Mix 37.35 wt% phosphor in 10 : 1 PDMS with glass stir rod.
Drip small amount of slurry on PDMS mold.
With PDMS-coated razor blade, squeegee slurry into relief features of PDMS mold.
Repeat in orthogonal direction.
Cure at 70 °C for 3 h.
Phosphor-island mold is manually aligned to the back side of a function μ-ILED array.

Analytical Model of Printed μ-ILED on a Glass Substrate. ***Basic equations.*** A half space with built-in disk heat source is used to model the present problem. The cylindrical coordinate system is set such that the origin is coincident with the center of the heat source. Schematic illustration of the device geometry and parameters used in the analytical model of heat flow is shown in Fig. S9. The steady-state axisymmetric heat conduction in cylindrical coordinates is

$$\frac{\partial^2 T}{\partial r^2}+\frac{1}{r}\frac{\partial T}{\partial r}+\frac{\partial^2 T}{\partial z^2}=0. \qquad \textbf{[S1]}$$

Setting $\theta = T - T_\infty$, where T_∞ is the remote temperature, the above equation is equivalent to

$$\frac{\partial^2 \theta}{\partial r^2}+\frac{1}{r}\frac{\partial \theta}{\partial r}+\frac{\partial^2 \theta}{\partial z^2}=0. \qquad \textbf{[S2]}$$

Boundary and continuity conditions are as follows:

1. $z = -H_g - H_L = h_1$ (Glass bottom surface):

$$\theta_g|_{z=h_1}=0. \qquad \textbf{[BC1]}$$

2. $z = 0$ (BCB-glass interface):
Downward heat flux

$$-k_b\frac{\partial \theta_b}{\partial z}\bigg|_{z=0}=G_1(r)=\begin{cases}-q_1, & 0\le r\le r_0\\ q_{0,\mathrm{int}}, & r>r_0\end{cases}. \qquad \textbf{[a]}$$

Upward heat flux

$$-k_g\frac{\partial \theta_g}{\partial z}\bigg|_{z=0}=G_2(r)=\begin{cases}q_2, & 0\le r\le r_0\\ q_{\mathrm{b,int}}, & r>r_0\end{cases}. \qquad \textbf{[b]}$$

Here the heat flux satisfy the following conditions

$$q_1\pi r_0^2+q_2\pi r_0^2=Q, \qquad \textbf{[c]}$$

$$\theta_g\Big|_{z=0}=\theta_b\Big|_{z=0}, \qquad \left[-k_b\frac{\partial \theta_b}{\partial z}\right]_{z=0,r\ge r_0}=\left[-k_g\frac{\partial \theta_g}{\partial z}\right]_{z=0,r\ge r_0}, \qquad \textbf{[BC2]}$$

where k_g and k_b are the thermal conductivities of glass and BCB, r_0 is the equivalent radius of LED and Q is the total heat generated in the LED.

3. $z = H_b = h_2$ (BCB-interconnect interface):

$$\theta_b\Big|_{z=h_2}=\theta_m\Big|_{z=h_2}, \qquad -k_b\frac{\partial \theta_b}{\partial z}\bigg|_{z=h_2}=-k_m\frac{\partial \theta_m}{\partial z}\bigg|_{z=h_2}, \qquad \textbf{[BC3]}$$

where k_m is the thermal conductivity of metal interconnect.

4. $z = H_b + H_m = h_3$ (Interconnect-air interface):

$$-k_m\frac{d\theta_m}{dz}\bigg|_{z=h_3}=h\theta_m|_{z=h_3}, \qquad \textbf{[BC4]}$$

where h is the coefficient of convection at the upper surface of a plate.

Solution. Eq **2** is solved via the Hankel transform, for which the following transform pair of the first kind is used,

$$\varphi(r,z)=\int_0^\infty \bar{\varphi}(\xi,z)J_0(\xi r)\xi d\xi$$
$$\bar{\varphi}(\xi,z)=\int_0^\infty \varphi(r,z)J_0(\xi r)r dr, \qquad \textbf{[S3a,b]}$$

where $\varphi(r,z)$ is the original function and $\bar{\varphi}(\xi,z)$ is the transform. The Hankel transform of **[2]** is

$$\frac{d^2\bar{\theta}}{dz^2}-\xi^2\bar{\theta}=0 \qquad \textbf{[S4]}$$

for which the solution is obtained as

$$\bar{\theta}=Ae^{-\xi z}+Be^{\xi z}, \qquad \textbf{[S5]}$$

and the heat flux is

$$-k\frac{\partial \bar{\theta}}{\partial z}=k\xi(Ae^{-\xi z}-Be^{\xi z}), \qquad \textbf{[S6]}$$

where A and B are two unknown functions to be determined according to boundary and continuity conditions. The temperature and heat flux are obtained as

$$\theta=\int_0^\infty (Ae^{-\xi z}+Be^{\xi z})J_0(\xi r)\xi d\xi \qquad \textbf{[S7]}$$

$$q_z=-k\frac{\partial \theta}{\partial z}=\int_0^\infty k\xi(Ae^{-\xi z}-Be^{\xi z})J_0(\xi r)\xi d\xi. \qquad \textbf{[S8]}$$

The boundary and continuity conditions can also be expressed in Hankel transform. Using **[5–8]**, the two unknowns A and B for each layer can be solved. For glass,

$$A_g=\frac{1}{\beta_1-\beta_2 e^{-2\xi h_1}}\frac{(\kappa+1)}{k_b\xi}\frac{Q}{\pi r_0}\frac{J_1(\xi r_0)}{\xi} \qquad B_g=-A_g e^{-2\xi h_1}. \qquad \textbf{[S9]}$$

For BCB,

$$A_b = \frac{1}{2}\left(1+\frac{k_g}{k_b}\right)A_g + \frac{1}{2}\left(1-\frac{k_g}{k_b}\right)B_g + \frac{1}{2k_b\xi}\frac{Q}{\pi r_0}\frac{J_1(\xi r_0)}{\xi}$$
$$B_b = \frac{1}{2}\left(1-\frac{k_g}{k_b}\right)A_g + \frac{1}{2}\left(1+\frac{k_g}{k_b}\right)B_g - \frac{1}{2k_b\xi}\frac{Q}{\pi r_0}\frac{J_1(\xi r_0)}{\xi}. \quad \textbf{[S10]}$$

For interconnect,

$$A_m = \frac{1}{2}\left[\left(1+\frac{k_b}{k_m}\right)A_b e^{-2\xi h_2} + \left(1-\frac{k_b}{k_m}\right)B_b\right]e^{2\xi h_2}$$
$$B_m = \frac{1}{2}\left[\left(1-\frac{k_b}{k_m}\right)A_b e^{-2\xi h_2} + \left(1+\frac{k_b}{k_m}\right)B_b\right], \quad \textbf{[S11]}$$

where

$$\beta_1 = \left(1-\frac{k_g}{k_b}\right) - \left(1+\frac{k_g}{k_b}\right)\kappa,$$
$$\beta_2 = \left(1+\frac{k_g}{k_b}\right) - \left(1-\frac{k_g}{k_b}\right)\kappa$$
$$\kappa = \frac{\left(1-\frac{k_b}{k_m}\right)e^{-2\xi h_3} - \frac{k_m\xi-h}{k_m\xi+h}e^{-2\xi h_3}\left(1+\frac{k_b}{k_m}\right)}{\frac{k_m\xi-h}{k_m\xi+h}e^{-2\xi h_3}\left(1-\frac{k_b}{k_m}\right)e^{2\xi h_3} - \left(1+\frac{k_b}{k_m}\right)}. \quad \textbf{[S12]}$$

The temperature in each layer can be obtained by Eq. **S7**. For example, the temperature in interconnect is given by

$$T_m(r,z) = T_\infty + \int_0^\infty (A_m e^{-\xi z} + B_m e^{\xi z}) J_0(\xi r)\xi d\xi. \quad \textbf{[S13]}$$

The interconnect surface temperature is then obtained by setting $z = h_3$. The LED temperature can be approximately by its average value over the entire active region as

$$T_{LED} = T_\infty + \frac{2}{r_0}\int_0^\infty (1-e^{-2\xi h_1})A_g J_1(\xi r_0)d\xi. \quad \textbf{[S14]}$$

The thermal conductivity of Al decreases as the film thickness decreases (2–5) as shown in Fig. S10*A*, which is extracted from several references. For our model, the thermal conductivity of Al is used as a fitting parameter, but with constraints to approximate the literature values. In the case of 300 nm and 1,000 nm Al interconnects, the thermal conductivities of 70 W/m/k and 160 W/m/k, respectively, are used in the model. These values were compared with reported values from the literatures to make sure they are within the reasonable range as depicted in Fig. S10*A*.

Finite Element Model to Determine the Temperature Distribution. A three-dimensional finite element model is established to study the temperature distribution in the LED system and validate the analytical model. Eight-node, hexahedral brick elements in the finite element software ABAQUS are used to discretize the geometry. A volume heat source is applied on the LED. The thermal convection boundary is applied at the air-interconnect interface and a constant temperature is applied at the bottom of the glass substrate. For LED arrays, a $\frac{1}{4}$ unit cell is used to take advantage of symmetry and periodic boundaries are applied. The finite element simulations agree well with analytical modeling as shown in Fig. S10*D*.

Experimental Setup for Measuring the LED Temperature. The printed μ-ILED is placed on a heated chuck with a base temperature of 50 °C, and pixel-by-pixel calibration is performed to yield a reference irradiance image of an unpowered sample in order to account for the emissivity differences on the sample surface. In some cases, however, when the material has emissivity <0.1, such as Al, temperature measurement could be inaccurate due to very low thermal emission (6). A surface ink or polymer that emits as a blackbody can be placed on top of the sample and to eliminate variation in emissivity (7). We did not use this procedure because of the destructive nature of this material to electrical device. As a result, we extracted quantitative values for the temperature only at the open areas between Al interconnects.

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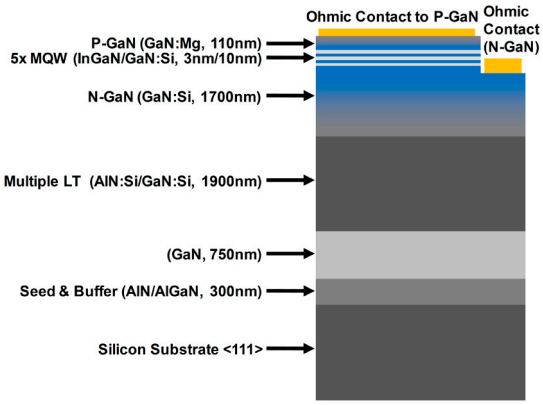

Fig. S1. Schematic illustration of epitaxial stack of InGaN MQW LED on Si (111) wafer.

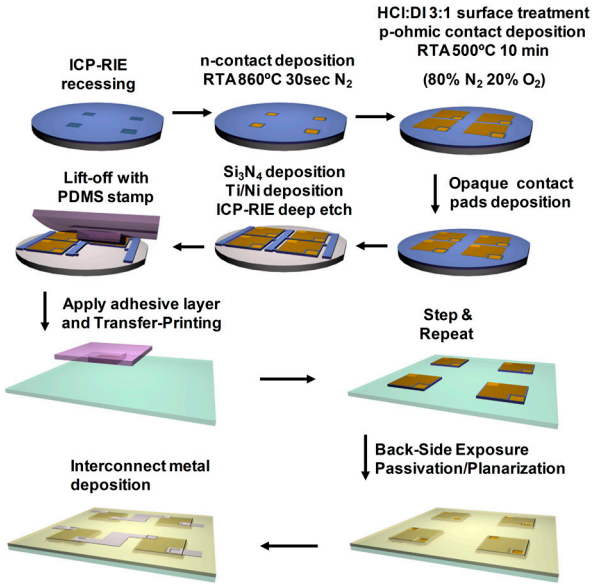

Fig. S2. Schematic overview of the fabrication process.

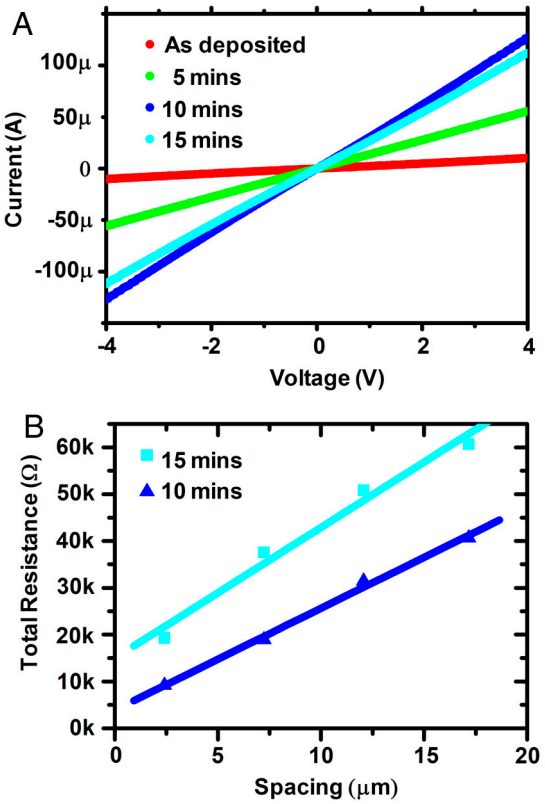

Fig. S3. Ohmic contact characteristics of Ni(10 nm)/Au(10 nm) to p-GaN. (*A*) Current-voltage characteristics of Ni/Au contact to p-GaN with TLM pad spacing of 21 μm in three different annealing conditions (i.e., As deposited, 5 min, 10 min, and 15 min annealing). (*B*) Plot of total resistance at four different pad spacing of 2.5 μm, 7.25 μm, 12 μm, and 17 μm.

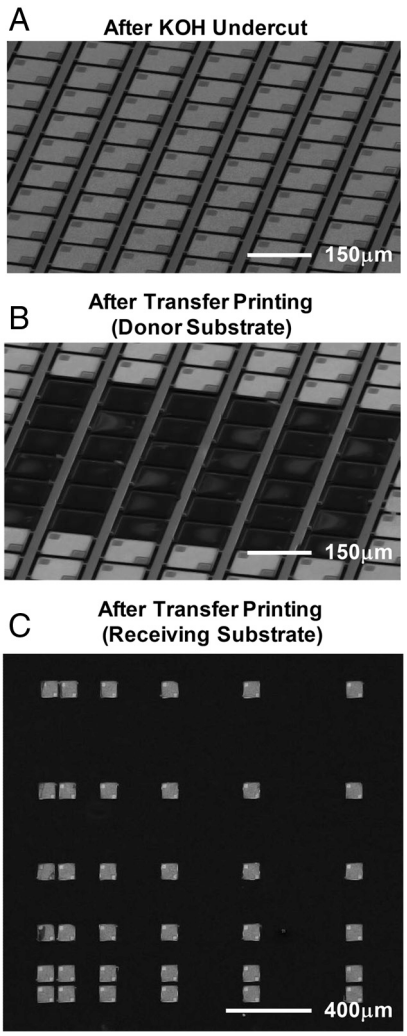

Fig. S4. SEM images of μ-ILEDs on (*A*) donor substrate after KOH undercut process, (*B*) donor substrate after transfer-printing process, and (*C*) receiving substrate (i.e., glass) after the transfer-printing process. μ-ILEDs are transfer-printed onto a glass substrate with varying pitches ranging from 25 μm to 500 μm.

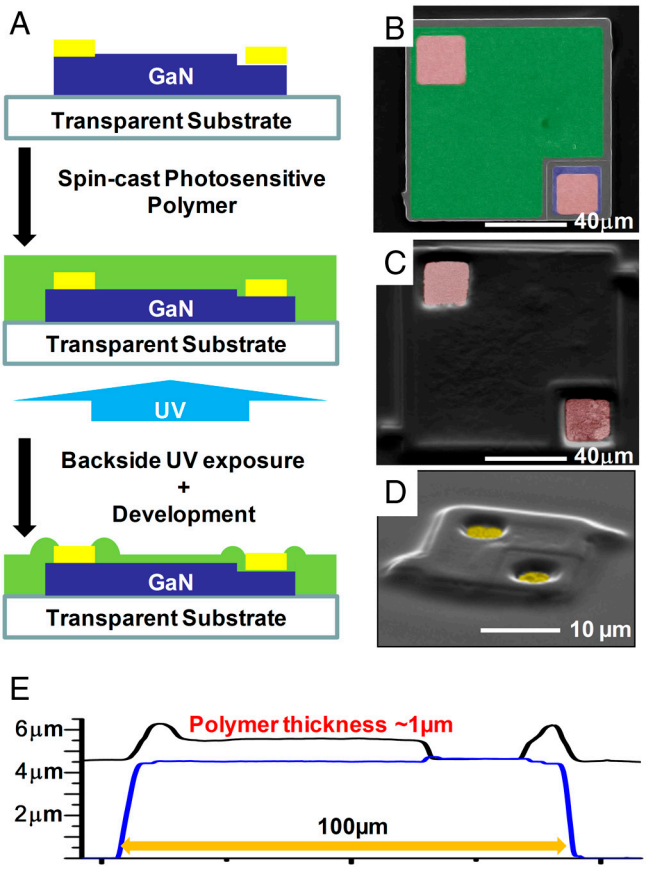

Fig. S5. (*A*) Schematic illustration of BSE process for self-aligned passivation and via formation. SEM image of a 100×100 μm^2 printed μ-ILED (*B*) before, and (*C*) after BSE process. (*D*) SEM image of 25×25 μm^2 μ-ILED after BSE process (colorized for easy of viewing). (*E*) Cross-sectional profile of μ-ILEDs after BSE process.

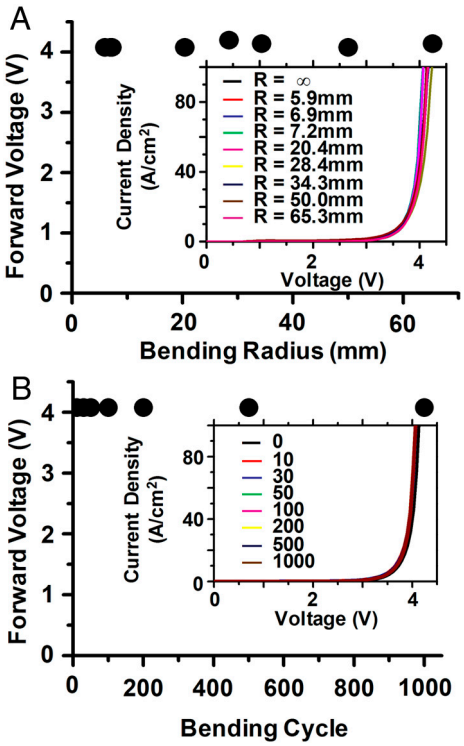

Fig. S6. (*A*) Forward voltage at 10 mA of current and corresponding current-voltage characteristics (inset) for representative μ-ILEDs printed on a PET substrate measured for varying bending radii. (*B*) Forward voltage at 10 mA of current and corresponding current-voltage characteristics (inset) for representative μ-ILEDs printed on a PET substrate measured for repetitive cycles.

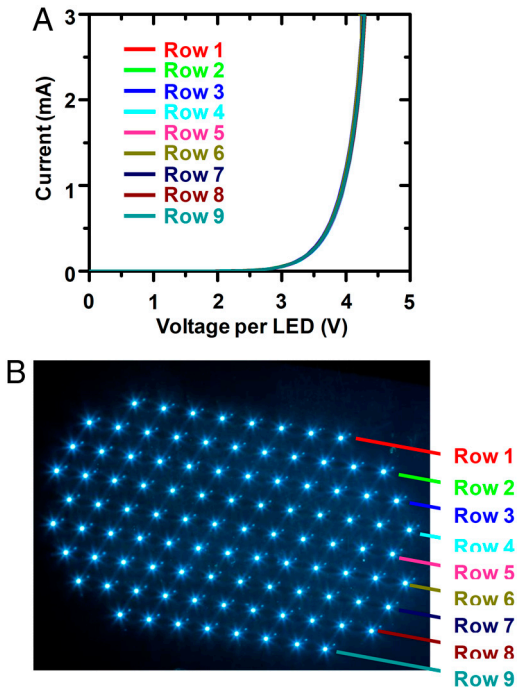

Fig. S7. (*A*) Current-voltage (I-V) characteristics of 100 μ-ILEDs from an array. (*B*) Optical image of an array consists of 100 μ-ILEDs.

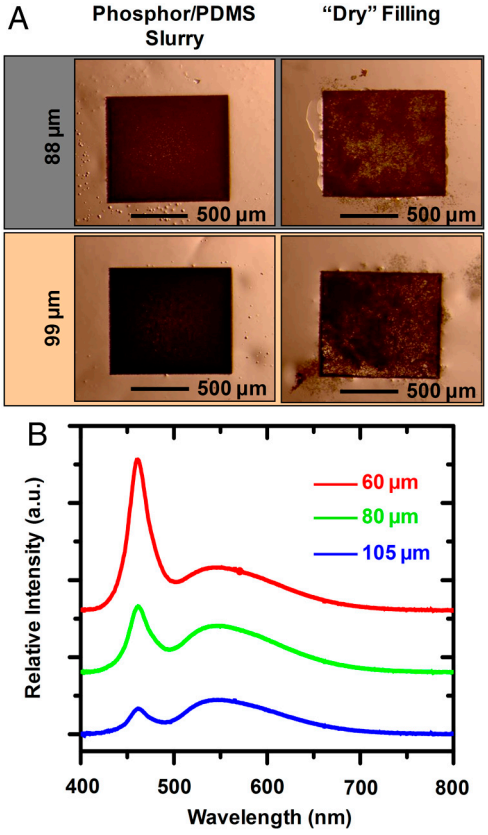

Fig. S8. (*A*) Optical microscopy images of relief features filled with a PDMS/phosphor slurry (left column) and filled with the phosphor powder only (right column). (*B*) Emission spectra of white μ-ILEDs with phosphor layer thickness of 60 μm, 80 μm, and 105 μm.

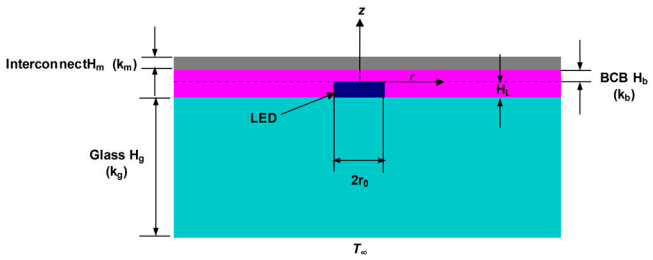

Fig. S9. Schematic illustration of the device geometry and parameters used in the analytical model of heat flow.

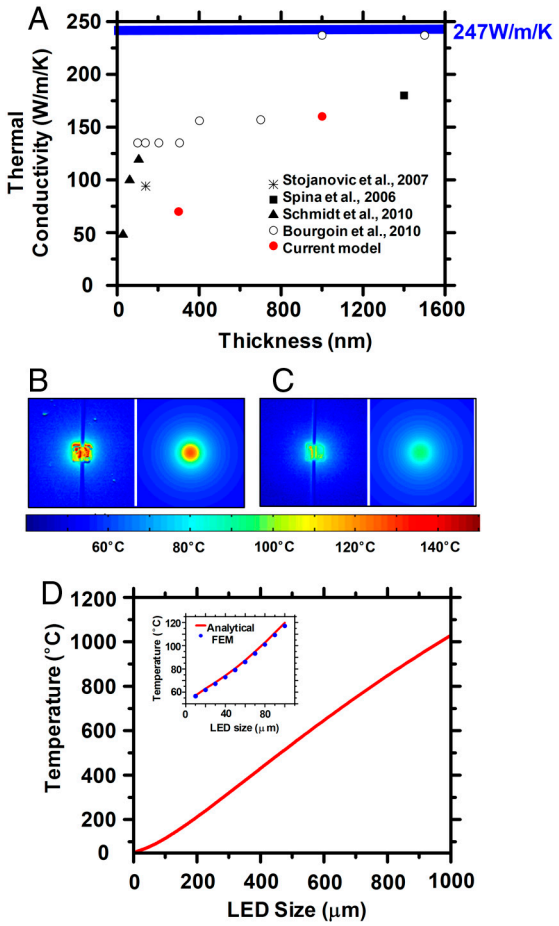

Fig. S10. (*A*) Reported thermal conductivities of a thin-film Al from several references. (*B–C*) Temperature distributions for isolated InGaN μ-ILEDs with Al interconnects [300 nm and 1,000 nm thick for (*B*) and (*C*), respectively] at input powers of (*B*) 25.2 mW and (*C*) 27.6 mW captured using a QFI Infra-Scope Micro-Thermal Imager (left) and calculated by analytical models (right). (*D*) A plot from analytical results on the surface temperature as function of LED size up to 1×1 mm^2. Inset provides comparison between analytical solution and FEM simulations on the surface temperature as function of LED size ranging from 10×10 μm^2 up to 100×100 μm^2.