Piezoresistive Strain Sensors and Multiplexed Arrays Using Assemblies of Single-Crystalline Silicon Nanoribbons on Plastic Substrates

Sang Min Won, Hoon-Sik Kim, Nanshu Lu, Dae-Gon Kim, Cesar Del Solar, Terrisa Duenas, Abid Ameen, and John A. Rogers

***Abstract*—This paper describes the fabrication and properties of flexible strain sensors that use thin ribbons of single-crystalline silicon on plastic substrates. The devices exhibit gauge factors of 43, measured by applying uniaxial tensile strain, with good repeatability and agreement with expectation based on finite-element modeling and literature values for the piezoresistivity of silicon. Using Wheatstone bridge configurations integrated with multiplexing diodes, these devices can be integrated into large-area arrays for strain mapping. High sensitivity and good stability suggest promise for the various sensing applications.**

***Index Terms*—Flexible circuits, single-crystalline silicon sensor, strain gauge.**

I. Introduction

THE DISCOVERY of piezoresistive effects in silicon by Smith in 1954 [1] led to the development of classes of silicon-based electromechanical sensor technologies that are now in widespread use in various applications, including structural health monitoring [2], tactile image detection [3], cardiovascular pressure measurement [4], and many others [5]. Large piezoresistive coefficients, high natural abundance, and mature processing technologies represent attractive aspects of silicon for these applications. Typically, silicon-based sensors are fabricated on wafers and then subsequently diced and integrated into small packages with microelectronic integrated circuits for signal manipulation and recording [2]–[5]. Although well configured for many applications, devices in this form are incompatible with certain applications in structural health monitoring for aircraft and in interfaces to the human body, where large-area large-scale integrated networks of sensors on thin deformable substrates are required. Conventional metal-foil strain gauges offer flexibility and the potential for use in this format, but they suffer low sensitivity [i.e., gauge factor (GF)] and limited scalability to large areas due to lack of strategies for multiplexed addressing (e.g., even a small 6×6 array can require as many as 72 electrode pads for addressing.) [6]. Recent research has aimed to overcome this limitation through the use of thin-film amorphous, microcrystalline, and polycrystalline silicon-based sensors and multiplexing devices [7]–[9]. Piezoresistive effects in these materials are, however, substantially lower than those in single-crystalline silicon [8]. Other approaches require the development of new classes of electronic materials, based on organic semiconductors, networks of single-walled carbon nanotubes [10], sheets of graphene [11], and others. Although certain of these technologies appear promising, none has the maturity and proven effectiveness of silicon.

In this paper, we report materials, integration strategies, mechanical modeling results, and system demonstrations of distributed networks of piezoresistive strain sensors based on ultrathin single-crystalline silicon membranes bonded to thin plastic substrates (i.e., polyimide). Such systems offer high sensitivity (i.e., piezoresistive coefficient or GF) of single-crystalline silicon while providing lightweight construction and mechanical flexibility. By using Wheatstone bridge (WB) configurations for the sensors and coupling them to multiplexing diodes, this technology can be scaled to large-area integrated monitors with spatial mapping capabilities.

II. Device Structure and Fabrication

The procedures that we use here build on concepts demonstrated for flexible electronics, in which ultrathin silicon ribbons or membranes (which we refer to as microstructured silicon, or μs-Si) are derived from bulk wafers, or silicon-on-insulator (SOI) substrates, and then assembled using printing-like techniques onto thin sheets of plastic [12]–[14]. Here, we use SOI (Soitec, unibond with 300-nm top p-type Si layer with resistivity of 14–22 $\Omega \cdot$ cm) to create devices schematically illustrated in an exploded view format in Fig. 1(a). The process begins by defining p- and n- doped regions in μs-Si via impurity diffusion procedures described in detail elsewhere [14]. Increasing the doping concentration improves the quality of the ohmic contacts and reduces the temperature dependence of the resistance,

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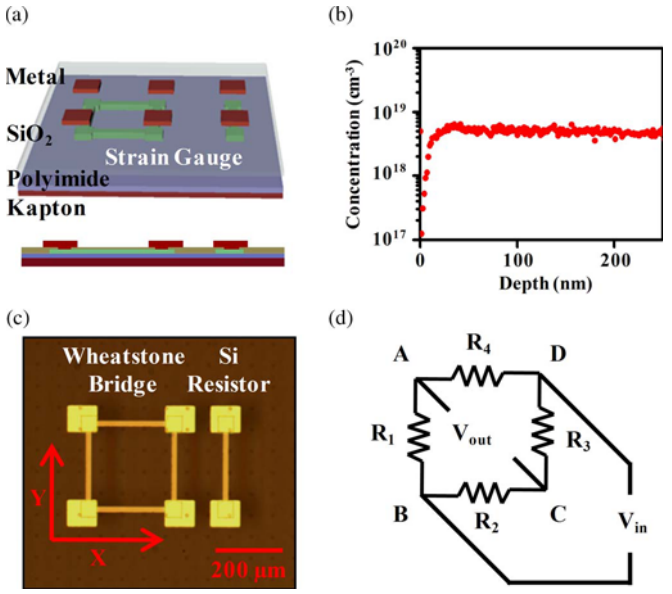

Fig. 1. (a) Schematic of a μs-Si resistor and a WB on a thin plastic substrate (Kapton; 75-μm thick) (b) Secondary ion mass spectrometry results showing a boron impurity concentration of $\sim 5 \times 10^{18}/\text{cm}^3$ through the entire thickness of μs-Si strain gauge. (c) Top-view optical micrograph of a representative WB and an isolated μs-Si resistor. (d) Circuit diagram of the WB. A ± 3 V input bias is applied between nodes B and D. The voltage difference between nodes A and C correlates to the uniaxial strain.

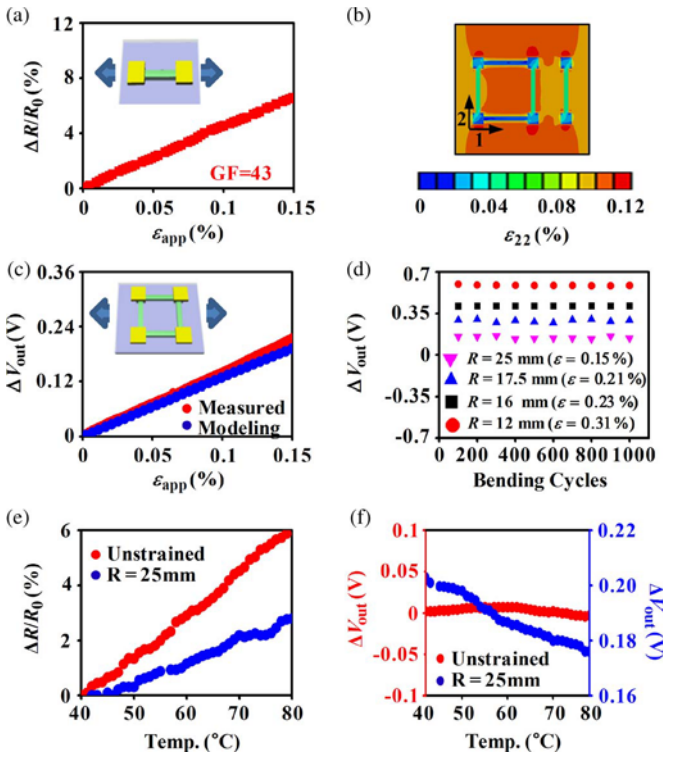

Fig. 2. (a) Fractional change in resistance $(\Delta R/R_0)$ of a μs-Si resistor as a function of the applied longitudinal tensile strain; the slope corresponds to a GF of 43. (b) Contour plot of strain calculated by FEM in a μs-Si resistor and a WB for a strain of 0.1% applied to the polyimide substrate in the longitudinal direction. (c) Change in output voltage ΔV_{out} from a WB as a function of uniaxial tensile strain. (d) Voltage output from a WB measured at different stages of fatigue testing, which involves 1000 bending cycles to different radii of curvature R indicated in the legend. For current designs, the minimum bending radius is $\sim$3 mm. (e) Fractional change in resistance $(\Delta R/R_0)$ of a μs-Si resistor as a function of temperature from 40 °C to 80 °C, indicating a TCR of $1.5 \times 10^{-3}/°\text{C}$ and $7.0 \times 10^{-3}/°\text{C}$ for unstrained and strained conditions, respectively. (f) Change in output voltage ΔV_{out} from a WB as a function of various temperatures from 40 °C to 80 °C.

but at the expense of reductions in the piezoresistance factor (i.e., strain sensitivity or GF) [15], [16]. With a boron concentration of $\sim 5 \times 10^{18}/\text{cm}^3$, silicon is sufficiently doped to provide good ohmic contacts. Furthermore, at this concentration, the temperature dependence (i.e., temperature coefficient of resistance or TCR) is reduced by a factor of $\sim 5\times$ [15], whereas the longitudinal piezoresistance factor is maintained to $\sim$80% [16] of its value at concentrations of $1 \times 10^{16}/\text{cm}^3$. By precisely controlling the diffusion temperature and duration, approximately uniform concentrations of boron $(\sim 5 \times 10^{18}/\text{cm}^3)$ can be achieved throughout the thickness (i.e., 300 nm) of the silicon used here, as illustrated in Fig. 1(b). We then print μs-Si on a polyimide substrate (DuPont Kapton(R) 100E film, 75-μm thickness) spin cast with a thin adhesive layer of polyamic acid (Sigma Aldrich Inc.), as described in detail elsewhere [12]–[14]. We use a simple strain gauge geometry, in which a layer of SiO_2 (200 nm deposited by plasma-enhanced chemical vapor deposition) and metallization of Cr/Au (50 nm/200 nm deposited by electron beam evaporation) serve as interlayer dielectric (ILD) and electrodes, respectively. Fig. 1(c) provides optical images of a strain gauge that uses a WB design with four separate μs-Si resistors, as well as a separate isolated μs-Si resistor, all on a polyimide substrate. The corresponding circuit schematic appears in Fig. 1(d); power is applied to nodes A and C, whereas output voltages are measured between nodes B and D. Imbalances between the voltage drops across the four resistors, caused by strains, lead to changes in V_{out}. We note that the devices can be stretched along different uniaxial modes, or in biaxial or other configurations. More complex layouts of strain gauges are, however, needed to characterize multiple strain components.

III. Result and Discussion

Uniaxial tensile strain applied along the lengths of resistor devices reveals its strain-induced changes in resistance. Fig. 2(a) shows a representative set of data from a device that incorporates a strip of silicon with dimensions of 20×200 μm^2; the inset provides a schematic. The resistance linearly varies with tensile strain throughout this range; the effective GF of this heterogeneous system is $\sim$43 derived by

$$\text{GF} = \frac{\Delta R}{R \times \varepsilon_{\text{app}}} \tag{1}$$

where ε_{app} is the applied strain onto the polyimide substrate.

Since the mechanical properties (e.g., moduli) of silicon and the polyimide substrate differ by nearly a factor of 100, the GF measured in this manner does not directly yield the value for the μs-Si. An analysis by finite-element modeling (FEM) yields distributions of strain that can be then used to determine intrinsic GF values (i.e., GF_{Si}). Fig. 2(b) presents a plot of the calculated strain on the top layer of the silicon resistor and the WB strain gauge for an applied tensile strain of 0.1% along the vertical direction. The FEM results indicate that the strain in the silicon is approximately 0.045% when a strain of 0.1% is

applied to the polyimide substrate for a device that has overall dimensions (i.e., silicon and surrounding polyimide) of 30 mm × 1 mm. The value of GF_{Si} can be calculated by

$$GF_{Si} = GF \cdot \frac{\varepsilon_{app}}{\varepsilon_{Si}}. \quad (2)$$

For GF = 43 at an applied strain $\varepsilon = 0.1\%$, the true strain in silicon $\varepsilon_{Si} = 0.045\%$, such that GF_{Si} is found to be ∼97. The intrinsic GF of [110] Si can be analytically calculated by the following equation [17]:

$$\begin{aligned} GF_{Si[110]} &= \alpha \pi_{Si[110]} E_{Si[110]} \\ &= 0.8 \times 71.8 \times 10^{-11} \times 168 \times 10^{9} \\ &= 96.49 \end{aligned} \quad (3)$$

where α is a correction coefficient accounting for different doping concentrations [16], π is the piezoresistive coefficient, and E represents Young's modulus. This calculated GF_{Si} value is in excellent agreement with our experiment and modeling result.

Fig. 2(c) shows the change in the output voltage of a WB strain gauge under ±3 V input bias as a function of applied uniaxial tensile strain [see the inset in Fig. 2(c)]. To model the voltage, we use the well-known equation

$$\frac{V_{out}}{V_{in}} = \frac{R_4}{R_3 + R_4} - \frac{R_2}{R_1 + R_2} \quad (4)$$

where R denotes the resistance of each bridge (i.e., each μs-Si resistor) and can be calculated by

$$R = R_0(1 + GF \cdot \varepsilon) \quad (5)$$

where ε is the applied strain, and R_0 is the initial resistance of each bridge. These gauges are sensitive to both in-plane and bending strains. For samples under uniaxial tension, ε is the applied tensile strain; for samples under pure bending (i.e., bent around a cylindrical tube),

$$\varepsilon = \frac{h}{2r} \quad (6)$$

where h is the sample sheet thickness, and r is the bending radius. Simulation based on (4) and (5) result agrees well with measured results, as illustrated in Fig. 2(c).

The mechanical fatigue properties of these devices are important to understand due to the mechanically brittle nature of silicon and to the stresses that concentrate at the interface between silicon and the underlying polyimide. For this purpose, we measured the change in output voltage for many cycles of bending to various radii. The results in Fig. 2(d) show that the changes in output voltages do not vary in any appreciable way to bending radii from 25 to 12 mm with up to 1000 cycles. These data suggest mechanically robust construction and stable operation. Another parameter of practical concern is sensitivity to variations in temperature. Fig. 2(e) presents the resistance of a μs-Si resistor as a function of temperature. The extracted TCR of $1.5 \times 10^{-3}/°C$ is comparable to literature values for p-type silicon with $\sim 10^{18}/cm^3$ dopant concentration [15]. The value

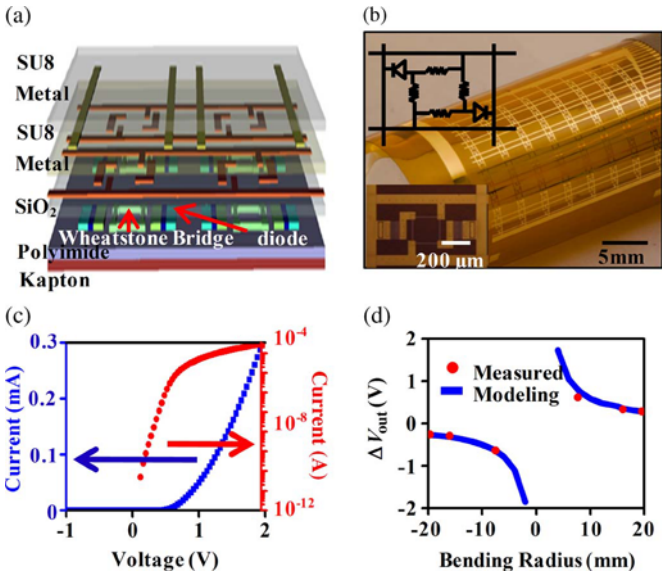

Fig. 3. (a) Schematic of a mapping array of μs-Si strain gauges, with μs-Si p-n diodes for multiplexed addressing. (b) Optical image of a representative array on a plastic substrate (Kapton); the inset on top and bottom left gives a circuit diagram and a top view of a single unit cell, respectively. (c) Current–voltage characteristics of a p-n diode with dimensions of 180 × 180 μm^2 and a thickness of 300 nm. The blue and red curves correspond to linear and semilog plots. (d) Change in output voltage ΔV_{out} from a WB as a function of bending radius; positive and negative radii correspond to bending in the outward and inward directions, respectively. The red dots and blue lines correspond to experimental measurements and modeling results, respectively.

reduces to $7.0 \times 10^{-3}/°C$, perhaps due to the carrier repopulation induced by valence band splitting [18], for a device bent to a radius of 25 mm. The reduction of GF in high temperature, as a consequence, is comparable to silicon piezoresistors reported elsewhere [19]. For strain gauges in WB configurations, same TCR associated with four μs-Si resistors yields minimal temperature effect in the unstrained condition, although the temperature can affect the device performance in the strained state. According to Fig. 2(c) and (f), the voltage induced by bending to a radius of 25 mm or, equivalently, by applying 0.15% tensile strain overwhelms the voltage induced by changes in temperature for an operating range from 40 °C to 80 °C.

Electrically integrating these strain gauges with p-n diodes can yield distributed networks of sensors with multiplexed readout for large area applications. An additional ILD layer (SU-8 2; MicroChem Corporation) resides between the first and second metal layers to separate the bias and data lines. For multiplexing, we chose p-n diodes over transistors due to their relative simplicity in construction and operation. Fig. 3(a) shows the layout of such a system, where anodes of two p-n diodes are connected at the output nodes of each WB. In this structure, all WBs in each row share a single bias line for one of their two input nodes, and all WBs in an array share a −3 V bias line for their other input node (e.g., six rows require a total of seven bias lines, i.e., six bias line for each row and one −3 V bias line for the entire set.). Each column also shares a line that is connected to the cathodes of the p-n diodes in that column. Multiplexing operates by applying +3 V to the input bias line of each row, in turn, while holding the bias of all the

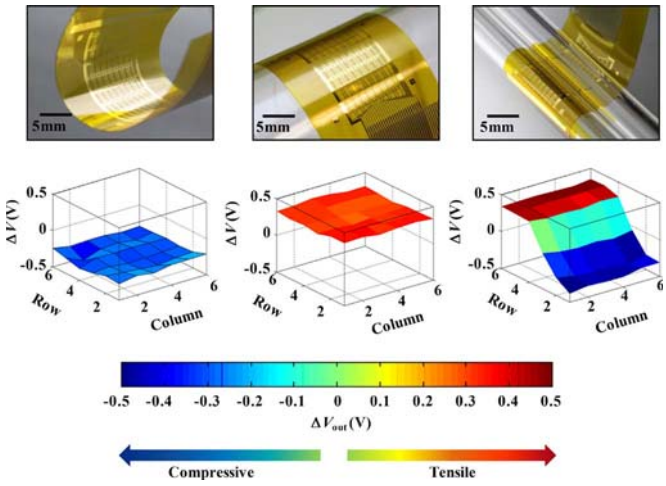

Fig. 4. Operation of the integrated array of μs-Si strain sensors, with μs-Si p-n diodes for multiplexed addressing, showing responses to bending in configurations, which induce uniform tensile and compressive strains, and a combination of these two. The bending radius is $\sim$18 mm.

other rows at -3 V. Voltages at the output nodes of all WBs in this condition result in -3 V, except the one that indicates the strain-induced voltage, for the WBs in a row with $+3$ V input line. This condition causes the diodes in all columns, except the one at the "on" row, to be reverse biased. As a result, the output from each column only has a contribution from the WB that is biased "on" in that column. Fig. 3(b) shows the optical image of the array, and the inset provides an image of a single unit cell. Fig. 3(c) presents the electrical characteristic of integrated p-n diodes. The off current is 85 nA at a reverse bias of 1 V; the value passes 0 A at a forward bias of 0.1 V.

Fig. 3(d) shows the operation of a multiplexed 6×6 array of sensors, measured at various bending radii. The red dots indicate the average output value from the array; the blue lines represent the output voltage derived from (1). The sign of the output voltage depends on the stress condition (i.e., tensile or compressive), as shown in the graph where positive and negative bending radii corresponding to tensile and compressive states, respectively, are indicated. Fig. 4 shows the operation of the array, operated in a spatial mapping mode, under tensile and compressive, and a combination of these two conditions, achieved by different bending configurations.

IV. Conclusion

This paper has presented a flexible strain mapping technology and multiplexing strategy that uses printed micro/nanostructures for single-crystalline silicon for gauges and p-n diodes on plastic substrates. Mechanical and electrical measurements show good stability and high sensitivity well suited for many applications in structural health monitoring and others. Extensions of these ideas can be used with stretchable or curvilinear substrates to address demanding requirements in strain mapping in biomedical applications.

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References

[1] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, Apr. 1954.
[2] J. P. Lynch, A. Partridge, K. H. Law, T. W. Kenny, A. S. Kiremidjian, and E. Carryer, "Design of piezoresistive MEMS-based accelerometer for integration with wireless sensing unit for structural monitoring," *J. Aerosp. Eng.*, vol. 16, no. 3, pp. 108–114, Jul. 2003.
[3] S. Sugiyama, K. Kawahata, M. Yoneda, and I. Igarashi, "Tactile image detection using a 1k-element silicon pressure sensor array," *Sens. Actuators A, Phys.*, vol. 22, no. 1–3, pp. 397–400, Jun. 1989.
[4] H.-L. Chau and K. D. Wise, "An ultraminiature solid-state pressure sensor for a cardiovascular catheter," *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 2355–2362, Dec. 1988.
[5] R. Bogue, "MEMS sensors: Past, present and future," *Sens. Rev.*, vol. 27, no. 1, pp. 7–13, 2007.
[6] A. L. Window, *Strain Gauge Technology*. New York: Springer-Verlag, 1992.
[7] D. Caputo, G. de Cesare, M. Gavesi, and F. Palma, "a-Si:H alloy for stress sensor application," *J. Non-Cryst. Solids*, vol. 338–340, pp. 725–728, Jun. 2004.
[8] L. Zhou, S. Jung, E. Brandon, and T. N. Jackson, "Flexible substrate micro-crystalline silicon and gated amorphous silicon strain sensors," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 380–385, Feb. 2006.
[9] E. S. Hwang and Y. J. Kim, "Flexible polysilicon strain gauge array," *Jpn. J. Appl. Phys.*, vol. 42, no. 7B, pp. 810–813, Jul. 2003.
[10] P. Dharap, Z. Li, S. Nagarajaish, and E. V. Barrera, "Nanotube film based on single-wall carbon nanotubes for strain sensing," *Nanotechnology*, vol. 15, no. 3, pp. 379–382, Mar. 2004.
[11] A. Sakhaee-Pour, M. T. Ahmadian, and A. Vafai, "Potential application of single-layered graphene sheet as strain sensor," *Solid State Commun.*, vol. 147, no. 7/8, pp. 336–340, Aug. 2008.
[12] J.-H. Ahn, H.-S. Kim, K. J. Lee, S. Jeon, S. J. Kang, Y. Sun, R. G. Nuzzo, and J. A. Rogers, "Heterogeneous three-dimensional electronics by use of printed semiconductor nanomaterials," *Science*, vol. 314, no. 5806, pp. 1754–1757, Dec. 2006.
[13] J.-H. Ahn, H.-S. Kim, E. Menard, K. J. Lee, Z. Zhu, D.-H. Kim, R. G. Nuzzo, and J. A. Rogers, "Bendable integrated circuits on plastic substrates by use of printed ribbons of single-crystalline silicon," *Appl. Phys. Lett.*, vol. 90, no. 21, pp. 213501-1–213501-3, May 2007.
[14] D.-H. Kim, W. M. Choi, J.-H. Ahn, H.-S. Kim, J. Song, Y. Huang, Z. Liu, C. Lu, C. G. Koh, and J. A. Rogers, "Complementary logic gates and ring oscillators on plastic substrates by use of printed ribbons of single-crystalline silicon," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 73–76, Jan. 2008.
[15] P. Norton and J. Brandt, "Temperature coefficient of resistance for p- and n-type silicon," *Solid State Electron.*, vol. 21, no. 7, pp. 969–974, Jul. 1978.
[16] R. Hull, *Properties of Crystalline Silicon*. London, U.K.: IET, 1999, pp. 425–427.
[17] C. Liu, *Foundations of MEMS*. Englewood Cliffs, NJ: Prentice-Hall, 2006, pp. 214–215.
[18] S. Middelhoek and S. A. Audet, *Silicon Sensors*. London, U.K.: Academic, 1989.
[19] Y. Kanda, "A graphical representation of the piezoresistance coefficients in silicon," *IEEE Trans. Electron Devices*, vol. ED-29, no. 1, pp. 64–70, Jan. 1982.

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