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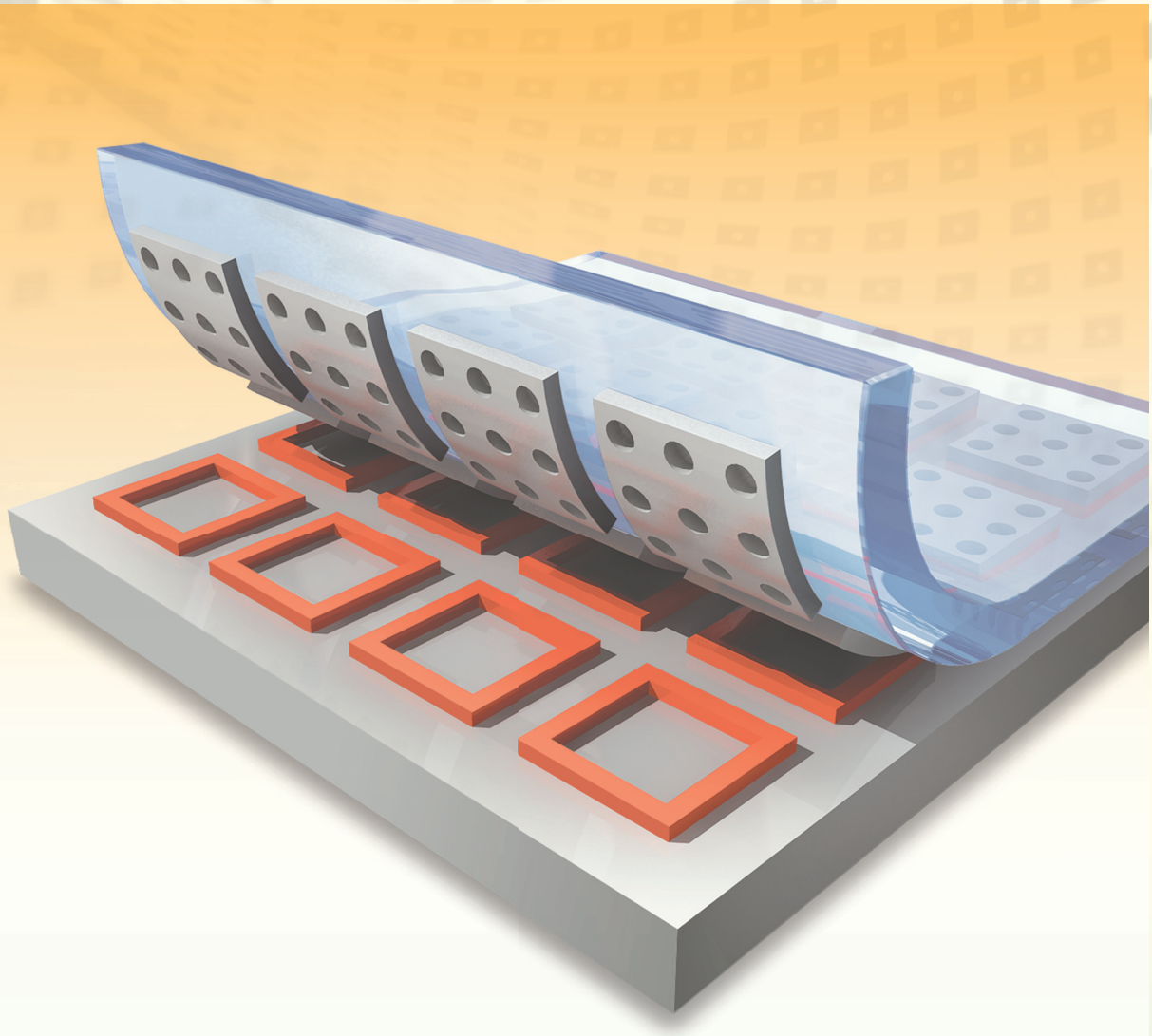

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Arrays of Silicon Micro/Nanostructures Formed in Suspended Configurations for Deterministic Assembly Using Flat and Roller-Type Stamps

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The ability to create and manipulate large arrays of inorganic semiconductor micro/nanostructures for integration on unconventional substrates provides new possibilities in device engineering. Here, simple methods are described for the preparation of structures of single crystalline silicon in suspended and tethered configurations that facilitate their deterministic assembly using transfer-printing techniques. Diverse shapes (e.g., straight or curved edges), thicknesses (between 55 nm and 3 μm), and sizes (areas of 4000 μm^2 to 117 mm^2) of structures in varied layouts (regular or irregular arrays, with dense or sparse coverages) can be achieved, using either flat or cylindrical roller-type stamps. To demonstrate the technique, printing with 100% yield onto curved, rigid supports of glass and ceramics and onto thin sheets of plastic is shown. The fabrication of a printed array of silicon p^+–i–n^+ junction photodiodes on plastic is representative of device-printing capabilities.

1. Introduction

Recent research suggests that flexible electronic/optoelectronic devices based on monocrystalline silicon and other inorganic semiconductors in micro/nanostructured forms offer capabilities that complement those available with organic active materials. The structures are typically formed directly from vapor or liquid phase growth[1] or from lithographic procedures applied to wafer-based sources of materials (e.g., layered epitaxial materials,[2] silicon-on-insulator substrates,[3] or bulk silicon,[4] GaAs, or InP wafers[5]). In both cases, the most successful methods for high-yield assembly into desired arrangements (e.g., aligned arrays) rely on deterministic approaches such as transfer printing. Here, strategies for maintaining organization in structures formed on a source substrate and for optimizing their subsequent release are critically important, yet both aspects have received relatively little attention in the literature. In the following, we demonstrate a set of procedures that is well suited for this purpose, with applicability to wafer-derived as well as synthesized materials.

Large collections of micro/nanostructures of silicon with thicknesses and lateral dimensions ranging from tens of nanometers to tens of millimeters can be derived from silicon-on-insulator (SOI) wafers by photolithography, reactive-ion etching (RIE), and then release by selective removal of the buried SiO_2 with HF.[3] Anisotropic etching of bulk silicon wafers with (111) orientation is also possible as a lower cost alternative.[4] In both cases, lightly pressing an elastomeric slab against the processed wafer and then peeling it back can lift off the silicon structures.[6] Release from the stamp to a target substrate in a printing-like step completes the process.[6] High-yield operation in this transfer printing procedure relies critically on methods to control

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adhesion to the critical surfaces (i.e., source and target substrate, and stamp). A less well explored but equally important aspect is in preparation of the silicon structures in ways that both preserve their spatial order and enhance their yields in release onto the stamp. Here, we describe a solution that uses polymer features (i.e., pedestals) beneath the near-edge regions of the perimeter of each structure, as supports and tethers. Optimized versions achieve freely suspended or partially collapsed formats, to minimize adhesion with the underlying substrate and to facilitate crack formation at their bottom interfaces during retrieval onto a stamp. This physics, combined with minimal area contact between the polymer and the structures and substrate, ensures high-yield operations in printing, even with the most basic stamp designs. To demonstrate the efficacy, we prepared and printed arrays of silicon structures with thicknesses from 55 nm to 3 μm, diverse lateral geometries (i.e., straight and curved edges with dimensions between 50 μm × 80 μm to 10.8 mm × 10.8 mm) and various layouts (i.e., regular, dense arrays to sparse, irregular geometries) onto various flat and curved substrates, using flat as well as roller-type stamps. As a device example we fabricated arrays of p^+–i–n^+ junction photodiode on a plastic substrate.

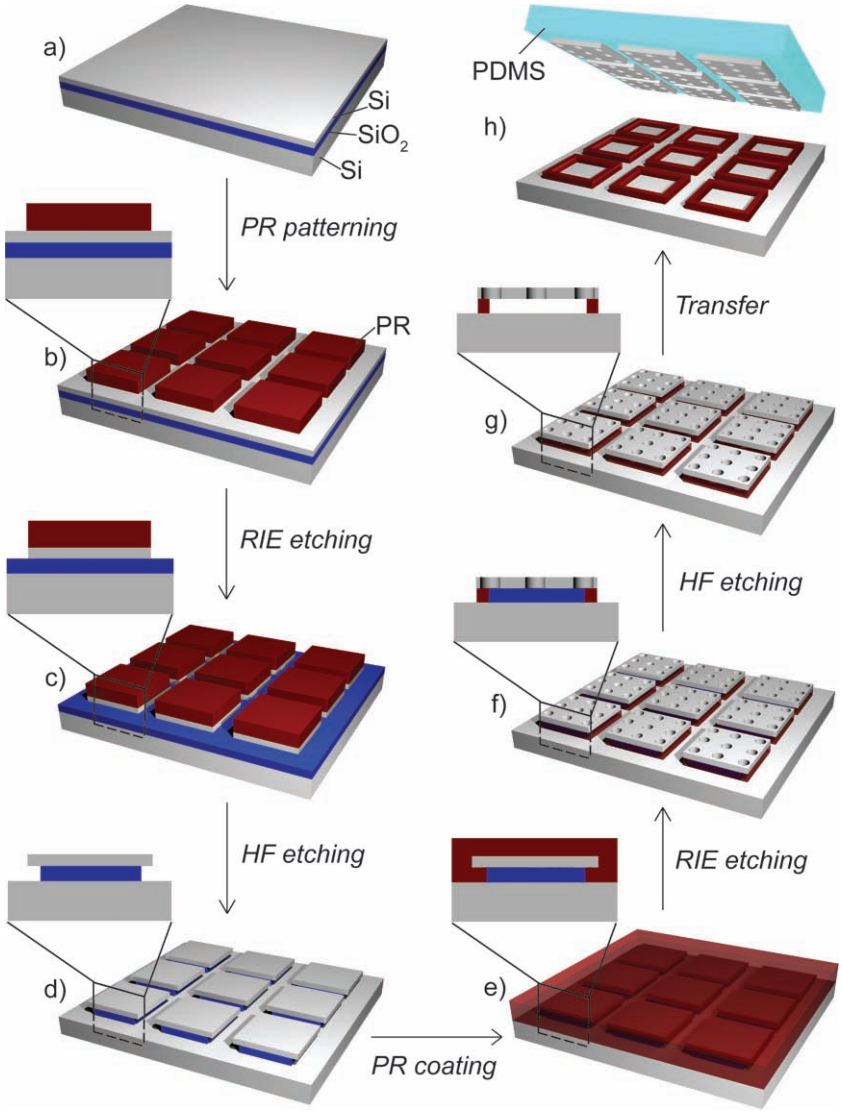

Figure 1. Schematic illustration of steps for fabricating printable single-crystal silicon platelets from an SOI wafer, and subsequent dry-transfer printing. The process uses contact mode photolithography and conventional etching procedures to generate isolated silicon patterns, and partial anisotropic wet etching followed by filling photoresist inside the undercut region and complete wet etching. The platelets can be printed onto a polymer slab. The zoomed cartoons in (b–g) illustrate cross-sectional views of the selected box regions.

2. Results and Discussion

Figure 1 presents a schematic illustration of the fabrication sequence. The process begins with coating an adhesion promoter, 1,1,1,3,3,3-hexamethyldisilazane (HMDS, AZ Electronic Materials Ltd.) and patterning photoresist (PR) (AZ 1512 and AZ 500 MIF developer) through contact-mode photolithography using a silicon-on-insulator wafer chip (SOI wafer, Soitec, thicknesses of top silicon/SiO_2: 55 nm/1000 nm, 260 nm/1000 nm, 700 nm/1000 nm, 1.25 μm/400 nm, and 3 μm/1.1 μm) (Figure 1a,b). RIE (SF_6 = 40 standard cubic centimeters per minute (sccm), 50 mTorr where 1 Torr ≈ 133 Pa, 50 W, 10 min for 1.25 μm thick top silicon) removes the unprotected top silicon to define the lateral dimensions of the desired micro/nanostructures (Figure 1c). Brief etching in hydrofluoric acid (HF 49%, DC Chemical Co., Ltd.; 20 s–2 min) removes the exposed SiO_2 layer between the structures and also, through undercut etching, in narrow (≈1–5 μm) regions beneath their edges (Figure 1d). Increasing the duration of the etching increases the widths of these regions. Next, spin-casting PR onto the entire substrate forms a coating that also penetrates and fills the edge undercuts (Figure 1e). After defining an array of holes through the PR and silicon by photolithography and RIE (see previous parameters), an additional uniform RIE process (O_2 = 20 sccm, 50 mTorr, 100 W, 10 min) removes the PR everywhere except the regions underneath the silicon, thereby forming a structure that we call a "perimeter pedestal" (Figure 1f). Further etching with HF removes the remaining SiO_2 via penetration through the etched holes in the silicon (Figure 1g). Longer distances between holes increases the etching time (30 min for our samples). Since the hole pattern reduces the area of the silicon and might affect function in electronic devices, careful design is required for certain applications. Finally, contacting a slab of poly(dimethylsiloxane) (PDMS, Dow Corning) against the substrate and then peeling it back lifts the silicon structures from the wafer in a high-yield

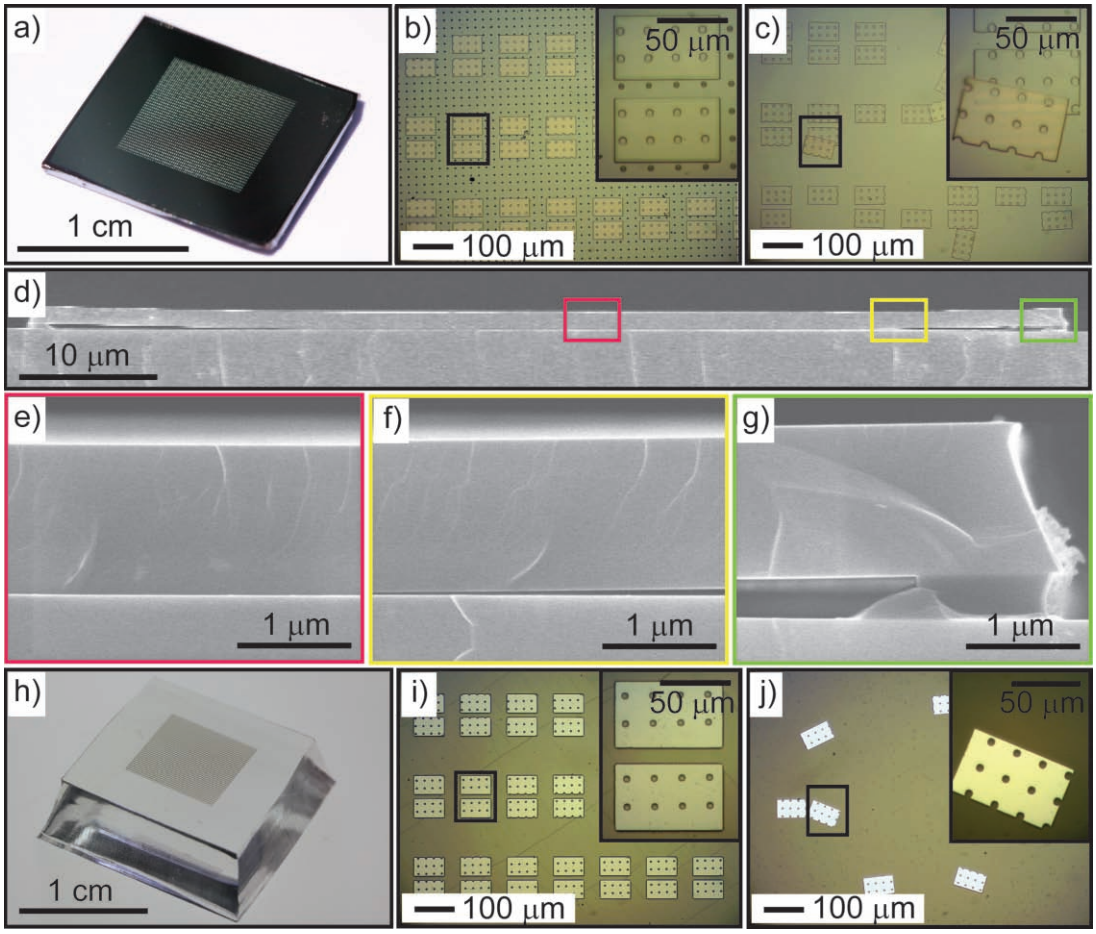

Figure 2. a,b,d) Photograph, optical microscope (OM), and SEM images of printable rectangular silicon islands with perimeter pedestals after Figure 1g process. h,i) Photograph and OM images of rectangular silicon islands transferred on a PDMS slab after Figure 1h process. c,j) OM images of rectangular silicon islands with no perimeter pedestal, on a chip before transfer and a PDMS slab after transfer, respectively. The insets of (b), (c), (i), and (j) are the magnified images of the selected black rectangular areas. e–g) The magnified images of selected areas of (d). The thickness of top single-crystal silicon used here is 1.25 μm.

manner via fracture at the interface between the perimeter pedestals and the silicon, driven by van der Waals adhesion to the PDMS (Figure 1h).[7] Pedestals that are transferred with the silicon structures can be removed by gentle washing with acetone (Figure 1h omits the partial transfer of PR pedestals for simplicity). This strategy holds the silicon structures in their lithographically defined positions, in a manner that involves minimal adhesion to the underlying substrate. (Fabrication details appear in the Supporting Information (SI).)

Figure 2a–c shows an array of silicon structures (50 μm × 80 μm, thickness: 1.25 μm) formed using the procedures above, with and without perimeter pedestals but with otherwise identical steps. In the former case (Figure 2a,b), the lithographically defined layouts are maintained even after complete removal of the SiO_2 (step g in Figure 1). Without the pedestals, the silicon islands often move slightly due to fluid flows during HF etching, washing and/or drying (Figure 2c). Cross-sectional scanning electron microscope (SEM) images of a representative silicon structure with perimeter pedestal (width: 1 μm, thickness: 400 nm) appears in Figure 2d–g. In this instance, the center region of the silicon sags into contact with the underlying substrate but the regions near the perimeter do not. This configuration results in reduced adhesion to the substrate, and it also facilitates crack formation at the silicon–silicon interface during retrieval with a PDMS stamp (Figure 2h,i). The ease with which fracture initiates at the silicon–silicon interface is related to the competition between adhesion at the silicon–silicon interface and van der Waals interactions at the PDMS–silicon interface. In the case of no pedestal, sagging occurs across the entire area of the silicon structures and induces strong interactions at the silicon–silicon interface, thereby leading to low transfer yield, as shown in Figure 2j. On the other hand, perimeter pedestals prevent the top silicon from sagging down completely; the interaction at the silicon–silicon interface is reduced, and the nonsagged regions provide locations for crack initiation. These effects lead to high yields in lifting the top silicon structure onto PDMS slabs or roller-type films. Results show that this approach results in ≈100% yields, with no significant misalignment, for all geometries and layouts investigated (see SI).

The widths and thicknesses of the perimeter pedestals depend on the etching time (Figure 1c,d) and the thickness of

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the SiO_2 layer. To examine the effect of width on alignment and transfer yield, we conducted systematic experiments with various etching times (see SI). In general, reducing the time decreases the widths and, therefore, the strength of adhesion between the silicon and the underlying wafer. Although beneficial for liftoff during the printing step, narrow pedestals of ≈0.5 μm or less lower adhesion, leading to unwanted motion or release of the silicon structures during the HF etching process (see SI). Pedestal widths of ≈8 μm or larger yields adhesion that exceeds levels compatible with high yields in liftoff (see SI). We find that widths between 1 and 5 μm, for silicon with 1.25 μm thickness and flat PDMS stamps, results in both perfect yield and alignment.

Another important parameter is the time delay between complete undercut HF etching and transfer printing (Figure 1g,h and SI). Without perimeter pedestals, the yield significantly decreases with the delay. For example, when the delay reaches 3 days, the top silicon cannot be transferred even by use of a commercially available tape (Scotch magic tape, 3M), which is much more adhesive than a slab of PDMS. During this time, it is likely that the silanol (–Si–OH) groups on the smooth surfaces contact each other and react to form –Si–O–Si linkages, resulting in strong adhesion. The chemical bonding between polished silicon surfaces at room temperature has been reported elsewhere, in the context of wafer scale contacts.[8] We observe that the perimeter pedestals minimize the influence of such mechanisms, thereby resulting in no observable change in transfer yield even after time delays of 3 days. For all results in this paper, the delay is less than ≈10 min, unless otherwise stated.

To demonstrate the versatility of the ideas, we demonstrated perimeter-pedestal-assisted transfer with various structures of silicon, including long ribbons (200 μm × 4 mm, **Figure 3**a), oriental Yin/Yang symbols (Figure 3b), traditional Korean patterns and alphabetic characters (Figure 3c), large area platelets (10.8 mm × 10.8 mm, fill factor: 95%, Figure 3d), all with thicknesses of 1.25 μm. Figure 3e,f show images of silicon mesh patterns with 55 nm thickness on PDMS. We often

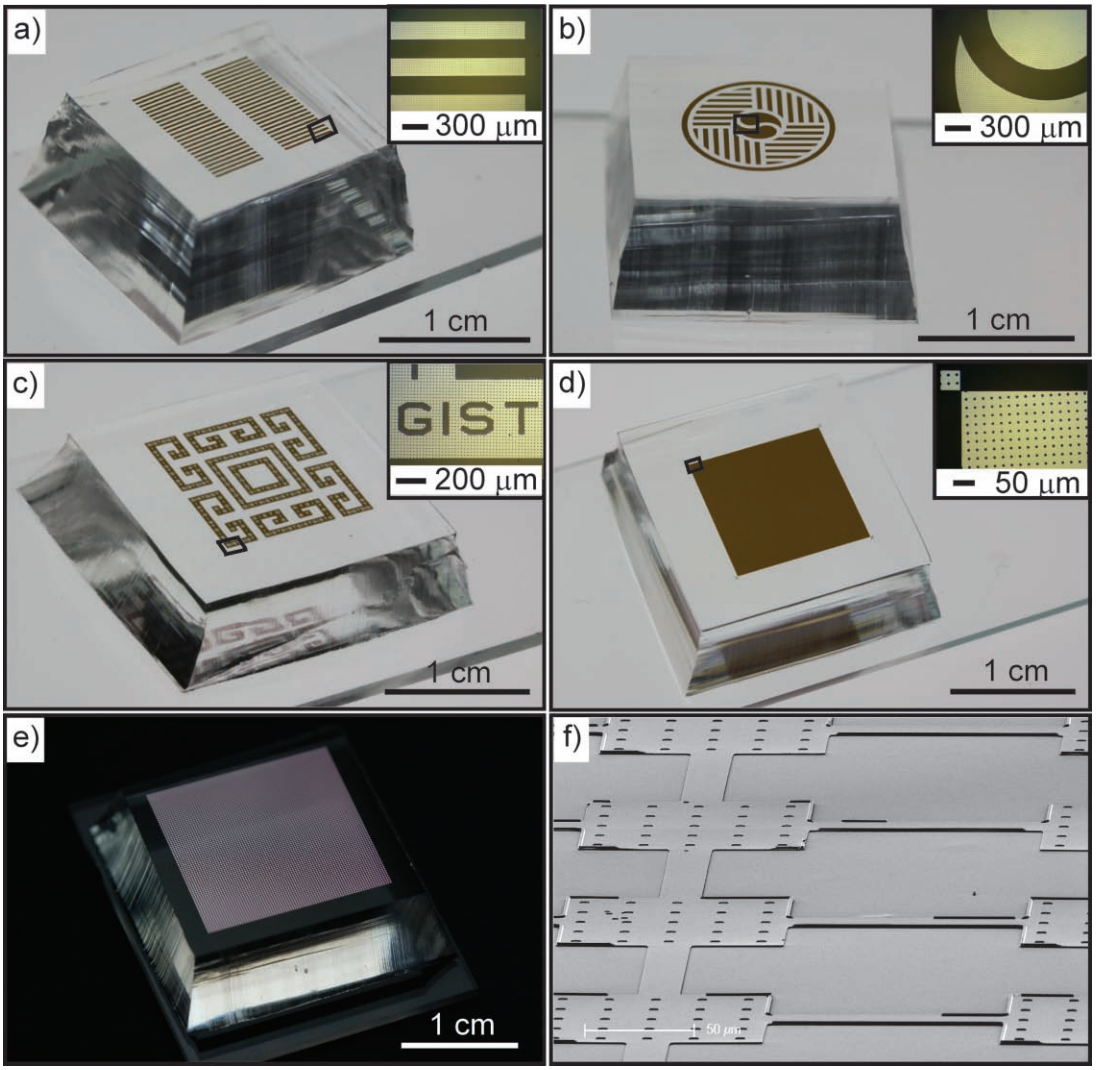

Figure 3. a–e) Photographs of various silicon patterns transferred on PDMS slabs. The insets are magnified OM images of the selected areas of (a–d). f) An SEM image of sample (e). The thicknesses of top single-crystal silicon used in (a–d) and (e) is 1.25 μm and 55 nm, respectively.

observed that part of the PR pedestal (width = 1 μm, height = 1 μm) remained adhered to the silicon, with the residual material on the silicon substrate (Figure 3f). The PR can be removed by acetone, gently using a squeeze bottle, prior to printing (see SI).

The extremely high yields of the reported process allow exploration of modes for transfer printing that have previously been impossible. For example, a continuous type of printing mode, via cylindrical roller-type stamps, could be appealing in some envisioned manufacturing sequences.[9] To demonstrate this mode, we formed a cylindrical piece of PDMS (length ≈ 2 cm, diameter = 8 mm) and performed printing by first rolling this stamp over an array of silicon ribbons (200 μm × 4 mm, thickness: 1.25 μm, with perimeter pedestals) at a speed of ≈1 cm s^{-1}. **Figure 4**a shows 100% transfer yield. Cylindrical stamps can also be constructed by wrapping thin (0.5 mm) PDMS layers on a soft rubber roller (length = 5 cm, diameter = 3.2 cm, HwaHong Industrial Co.). Figure 4b shows such a stamp after liftoff of arrays of square silicon structures (500 μm × 500 μm) by rolling the stamp in sequence against multiple SOI wafer chips (two chips were used) under a pressure range of ≈200–250 kPa. The thin PDMS film can be peeled from the roller and attached on a mug or wrapped on a curvilinear surface as shown in Figure 4c,d. Reprinting the silicon patterns is also possible by rolling the stamp against a different target substrate such as a paper (e.g., a gift card in Figure 4e) using a spray adhesive (77 Graphic Art spray adhesive, 3M) under a pressure range of ≈50–100 kPa. In this case, the sprayed layer of glue was further rubbed to smoothen the surface: contact was maintained for 30 s at room temperature to ensure good adhesion before transfer, to achieve overall yields of 100%. We note that the average pitch of the silicon islands increased by 2.9% and 2% in directions along and perpendicular to the rolling direction, respectively, likely due

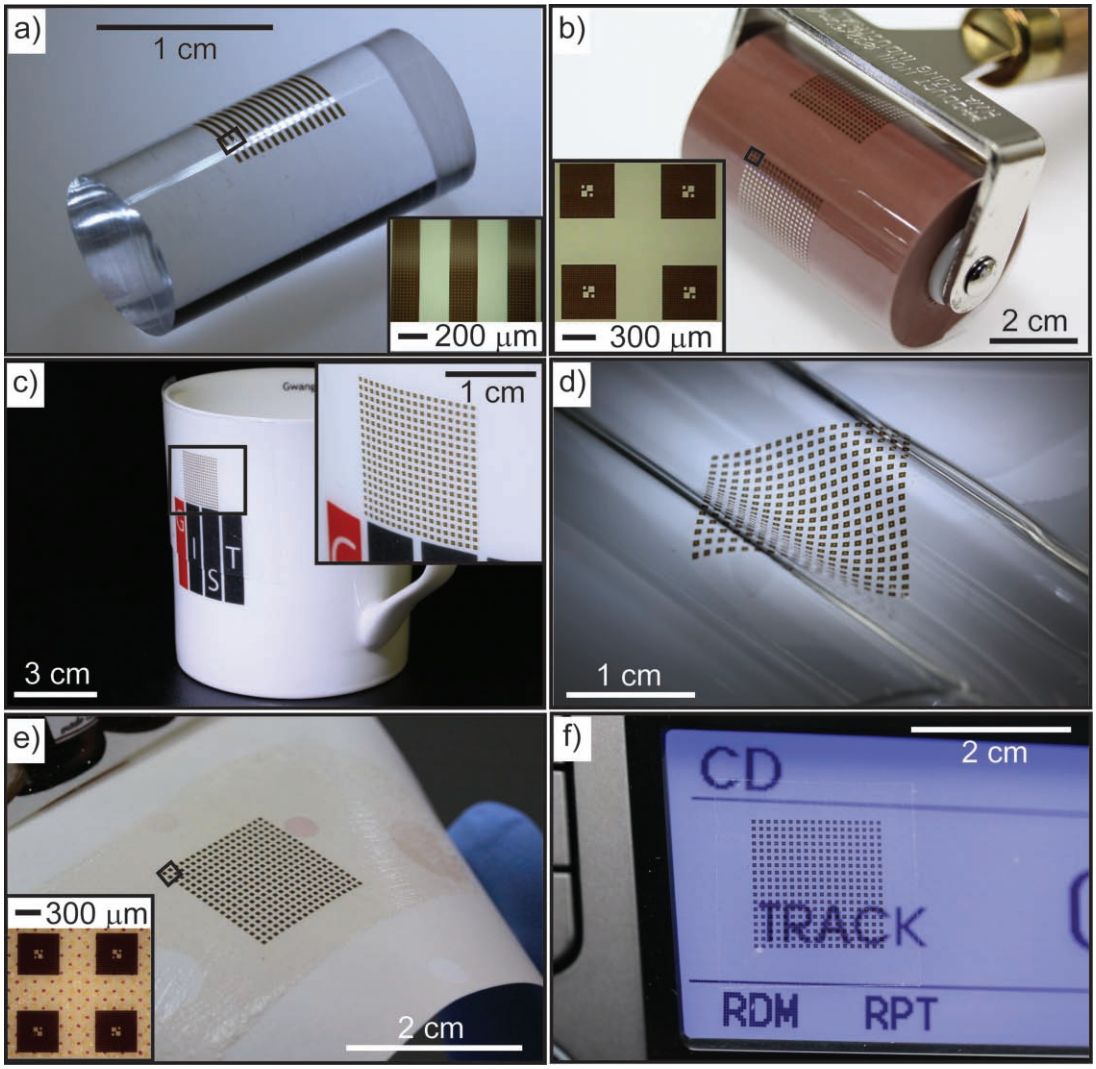

Figure 4. a,b) Photographs of single-crystal silicon ribbons transferred onto a PDMS cylinder (a) and square island arrays on a thin PDMS film attached on a roller (b). c,d) a thin PDMS film from sample (b) attached on a mug (c) and wrapped on two disposable pipettes (d). e,f) Photographs of the single-crystal silicon secondly transferred onto a gift card using a spray adhesive (e) and a car audio player (f) using an adhesive tape from sample (b). The thickness of top single-crystal silicon used here is 1.25 μm.

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to slight deformations in the PDMS induced by the printing process. Another example of roll printing is to transfer the silicon pattern from the PDMS to a commercial transparent tape (e.g., label tape, YEEHYUN) under a pressure range of ≈50–100 kPa. The tape can be attached on various substrates: for example, the surface of a car audio player (Figure 4f), and a paper (see SI). The overall transfer yield is 100% and the average pitches, in this case, increased by 2.8% and 0.8% in

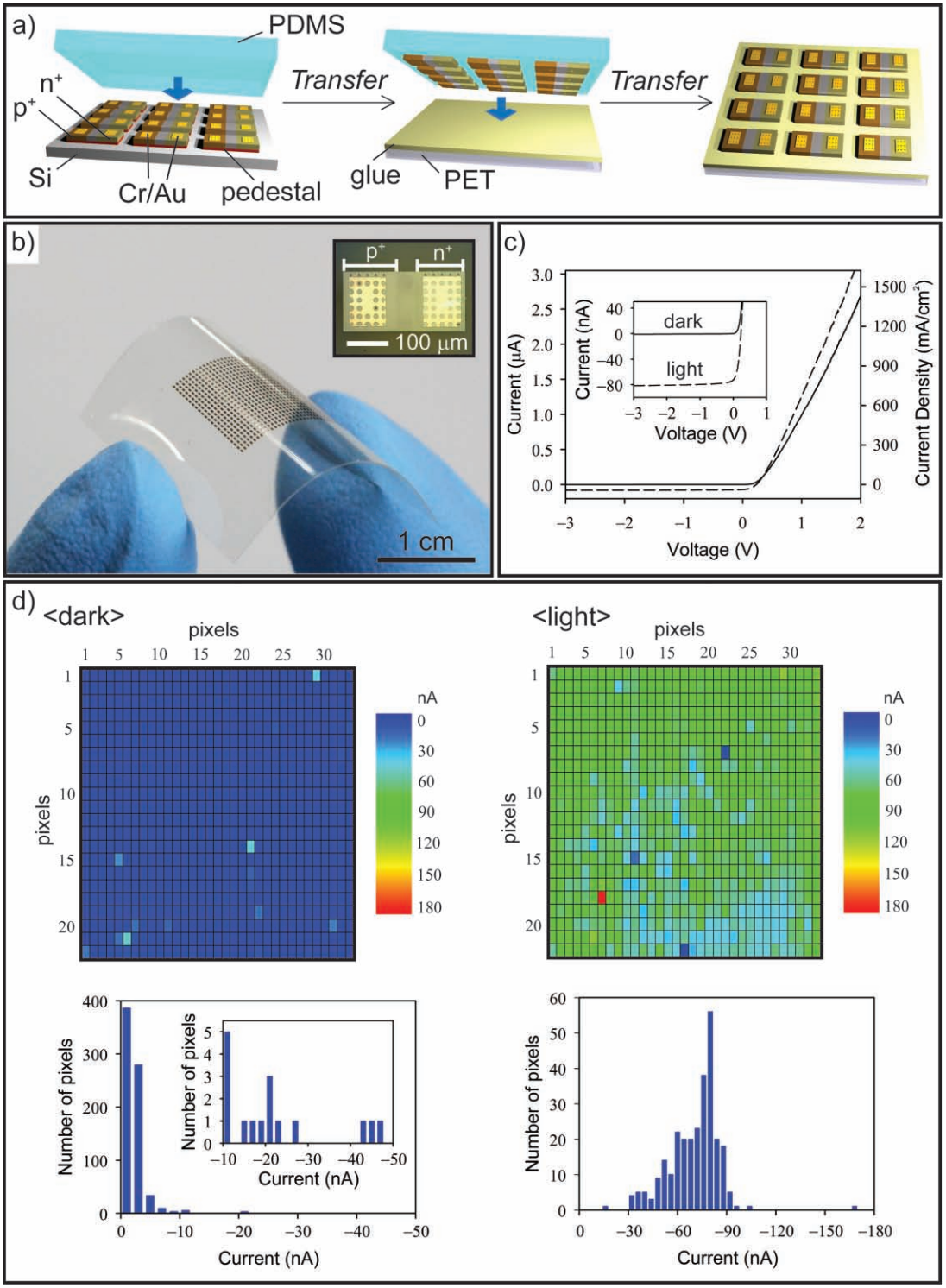

Figure 5. a) Schematic illustration of steps for transferring a p^+–i–n^+ single-crystal silicon photodiode array from a donor wafer to a flexible plastic substrate. The arrays of silicon diodes were firstly transferred through the process of Figure 1 and then retransferred onto a PET film. b) The photograph of the photodiode array on a flexible plastic substrate. The inset is the OM image of a representative photodiode. c) The representative *I*–*V* curves of a photodiode in light and dark. The thickness of top single-crystal silicon used here is 1.25 μm. d) Current levels in all cells at –3 V in light and dark.

directions along and perpendicular to the rolling direction (see SI). The larger increase in pitch in the rolling direction might include effects of slight slippage during rolling.

As an example of a device, we prepared p^+–i–n^+ junction diodes (33 pixels × 22 pixels, with dimensions of 150 μm × 300 μm and thicknesses of 1.25 μm) on a polyester film (thickness: 110 μm, LAMI-ACE Corporation) as shown in **Figure 5**a,b. Doping by a thermal diffusion process in a gas flow of oxygen and nitrogen (see Experimental Section)[10] and defining Cr/Au (3 nm/150 nm) electrodes by photolithography and wet etching were performed with other steps identical to those shown in Figure 1. To facilitate adhesion to the PET, we used a thin layer of polyurethane (Norland Optical Adhesive), photocured by passing UV through the PET film (see Experimental Section). The overall transfer yield is 100%, with just one cell exhibiting any significant misalignment. The average pitches in the *x* and *y* directions of the diodes on the PET film increased slightly by 0.9% and 0.7% compared to those on the silicon chip before the transfer (see SI). The difference is presumably due to the slight thermal expansion of the PDMS slab during the optical curing of the adhesive layer. We observed no significant difference between current-voltage (*I–V*) characteristics of diode arrays of a SOI wafer chip before etching SiO_2 layer and final device on a PET film (see SI). Representative *I–V* characteristics measured in light and dark conditions [solid curve: in the dark; dashed curve: exposed to halogen bulb light source (LG-PS2, 12 V, 100 W)] show expected diode and photovoltaic behavior, suitable for use in rectifying devices, photodetectors or solar cells (Figure 5c). In the forward bias of five cells selected randomly, an average diode ideality factor at room temperature is ≈2.2, which is very similar to that (≈2.3) in the diodes on a SOI wafer chip before transfer (see SI). We observed a slightly higher current level of the diodes on the PET film in reverse bias in the dark, possibly due to contaminants from the fabrication process and/or different materials (the buried oxide layer[11] with a volume resistivity of $\approx 10^{16}$ Ω cm on the wafer chip and the adhesive layer[12] with a volume resistivity of $\approx 10^{15}$ Ω cm on the PET film) underneath the diodes. Figure 5d shows current levels in all cells before and after the light illumination at –3 V shown in Figure 5c. The average current of the all diodes on the PET film in light and dark are –69.5 nA and –2.54 nA with standard deviations of 15.4 nA and 3.66 nA, respectively. The yield with good photovoltaic characteristics is ≈99.4% (722 out of 726 cells). The failure of the 4 cells is likely due to inhomogeneity in doping or contaminants acquired during the fabrication process.

3. Conclusion

This research addresses important aspects of the printing-based assembly of micro/nanomaterials that relate to the preparation of the structures, rather than the printing process itself. The ideas focus on the formation of suspended and tethered configurations, optimized to maintain organized layouts and to minimize adhesion to the source/growth substrate. The simplicity of these procedures, their effectiveness and their ability to enable new modes of printing with cylindrical roller-type stamps suggest their potential for use in sensors, photodetectors, solar cells, diodes, transistors, and systems that include these components.

4. Experimental Section

The SOI wafers were cleaned by washing with acetone, IPA, and deionized water (Millipore, resistance ≈18 MΩ); drying occurred at 110 °C for 1 min, just before use. A mask aligner (CA-6M, SHINU MST) was used for contact mode lithography. Details of the experimental procedures for Figure 1–4 appear in the SI.

Preparing the SOI wafers for arrays of photodiodes began with p^+ and n^+ doping. Depositing a SiO_2 layer (thickness = 600 nm) using PECVD (Oxford, gas flow: SiH_4 = 160 sccm, N_2O = 730 sccm, 300 °C) and patterning the oxide layer by photolithography and etching (buffered oxide etchant, BOE 6:1, J. T. Baker) formed masks for boron and phosphorus doping. Spin-coating a layer of spin-on-dopant (p-type, Boron, B 216, 3000 rpm, 30 s, Filmtronics), annealing it at 1050 °C under gas flow (N_2 = 0.5 L min^{-1}, O_2 = 0.125 L min^{-1}) for 30 min using an rapid thermal annealing (Ajoen Heating Industrial Co., Ltd.) furnace, that then removing this layer (HF for 30 s, piranha for 5 min, BOE for 1 min) completed the p^+ doping. The same procedures were used for n^+ doping, except for the spin-on-dopant type (n-type, Phosphorus, P 506, 3000 rpm, 30 s, Filmtronics), annealing (950 °C for 20 min) and cleaning (BOE for 4 min, piranha for 3 min, BOE for 1 min) processes. Forming metal contacts involved depositing Cr/Au (3 nm/150 nm) by sputtering (Cr: Ar 15 sccm, 5 mTorr, 350 V; Au: Ar 15 sccm, 15 mTorr, 400 V; Korea Vacuum Tech., Ltd.) and back-etching (Cr etchant: CR-7, OMG; Au etchant: Gold Etch, Transene Company, Inc.) through a lithographically defined mask of PR. The procedures for release and formation of perimeter pedestals appear in Figure 1. The printing involved contacting a piece of PDMS with the array of diodes on its surface against a film of PET film coated with an adhesive layer (Norland Optical Adhesive 61, Norland Products, Inc.) and then curing the adhesive by passing UV light (low pressure mercury vapor grid lamp, AH1700, AHTECH LTS, power: 28 mW cm^{-2}, distance: 6 mm) through the PET film for 30 min. Finally, the device was cleaned by rubbing the surface using a cotton brush soaked in acetone. *I–V* curves were measured using a probe station (Agilent Technologies, B1500A). SEM images were collected with a Hitachi S-4700 after coating platinum about 7 nm on the samples.

Supporting Information

Supporting information is available from the Wiley Online Library or from the author.

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