Monolithic Integration of Arrays of Single-Walled Carbon Nanotubes and Sheets of Graphene

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Single-walled carbon nanotubes (SWNTs) and graphene are of great interest due to their exceptional electrical, thermal, and mechanical properties.[1–3] Thus far, extensive research has explored the use of these carbon nanomaterials in field-effect transistors, sensors, and transparent conductors.[4,5] As a first step toward all-carbon-based electronics, the monolithic integration of nanotubes and graphene in ultrathin-film type devices and test structures represents a natural possibility that could be important both for scientific study and applications. A key technical challenge is that graphene and SWNTs, particularly in array formats, are typically formed using incompatible growth conditions, catalysts, and substrates. A potential solution lies in the emergence of methods,[6–8] some with exceptionally high levels of engineering sophistication,[9] for transferring these and other classes of nanomaterials from one substrate to another.

Here, we describe transfer printing strategies to fabricate transistors that incorporate perfectly aligned arrays of SWNTs[10–12] for the semiconductor and sheets of graphene for the source, drain, and gate electrodes. This process involves optimized growth conditions for each material separately because integration occurs in a subsequent step. The resulting devices have ultrathin layouts with high levels of optical transparency throughout the visible range. Furthermore, we directly compare graphene and Pd as electrodes for SWNT devices by fabricating two-terminal test structures with asymmetric contacts. Characterization of the electrical responses reveals the key properties and provides some preliminary insights into physics and materials aspects of electrical contacts between graphene and SWNTs.

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DOI: 10.1002/adma.201101955

To form sheets of graphene and arrays of SWNTs, we used chemical vapor deposition (CVD) with uniform films of Ni (300 nm; electron beam evaporation) on thermally grown SiO_2 (300 nm)/Si substrates and narrow stripes of Fe (1–5 Å; electron beam evaporation) on pre-annealed (8 h, 900 °C in air) stable temperature (ST)-cut quartz substrates (Hoffman Materials, Inc.), respectively. For the former, flowing a mixture of Ar (900 sccm) and H_2 (700 sccm) through a quartz reaction chamber (1 in. diameter) containing the substrate at 950 °C for 30 min removes any surface oxide layer and promotes grain growth and a reduction in surface roughness. Next, flowing a mixture of Ar (300 sccm), H_2 (200 sccm), and methane (10 sccm) for 3 min at 965 °C followed by cooling at ≈8 °C s^{-1} leads to precipitation of graphene on the surface of the Ni. For the SWNT arrays, annealing the substrate at 900 °C for 1 h in a quartz reaction chamber oxidizes the Fe catalyst. Cooling the substrate to room temperature and then heating to 925 °C with H_2 (400 sccm) for 10 min reduces the catalyst. CVD for 20 min with a flow of Ar (20 sccm) and H_2 (20 sccm) introduced through an ethanol bubbler yields aligned arrays of SWNTs. For both graphene and SWNTs, the growth techniques follow recent reports.[13–18]

Figure 1 provides a schematic illustration of the integration process. Here, the quartz growth wafer forms the device substrate. The first step involves photolithography and etching with an oxygen plasma to define patterns of graphene electrodes on the Ni/SiO_2/Si growth substrate. Next, a commercial etchant (Transene, Inc.) eliminates the Ni, thereby leaving the patterned graphene supported directly on the SiO_2/Si substrate. Uniformly evaporating a thin layer of Au (100 nm) and spin casting a film of polyimide (PI; 1.5 μm) forms a bilayer that serves as a backing support for the graphene. Lifting the entire sheet with a soft, elastomeric stamp of poly(dimethylsiloxane) (PDMS), followed by aligned transfer printing delivers the sheet onto the SWNTs, with the electrode patterns placed in the regions between adjacent Fe catalyst lines (Figure 1b). Wet and dry etching of the Au and PI with a commercial etchant (Transene Inc.) and an oxygen plasma, respectively, completes this first level of graphene/SWNT integration. Oxygen plasma etching through a photolithographically defined mask removes the SWNTs not located in the gaps between adjacent pairs of graphene electrodes (Figure 1c), to provide electrical isolation. A summary of electrical measurements on the resulting arrays of two terminal graphene/SWNT devices appears subsequently. Fabrication of transistors proceeds with deposition of a gate dielectric of HfO_2, consisting of a bilayer of material deposited by atomic layer deposition (ALD) and electron beam evaporation to thicknesses of 5 nm and 45 nm, respectively. Transfer printing a uniform sheet of graphene on top of the HfO_2 and then patterning it by photolithography and etching defines

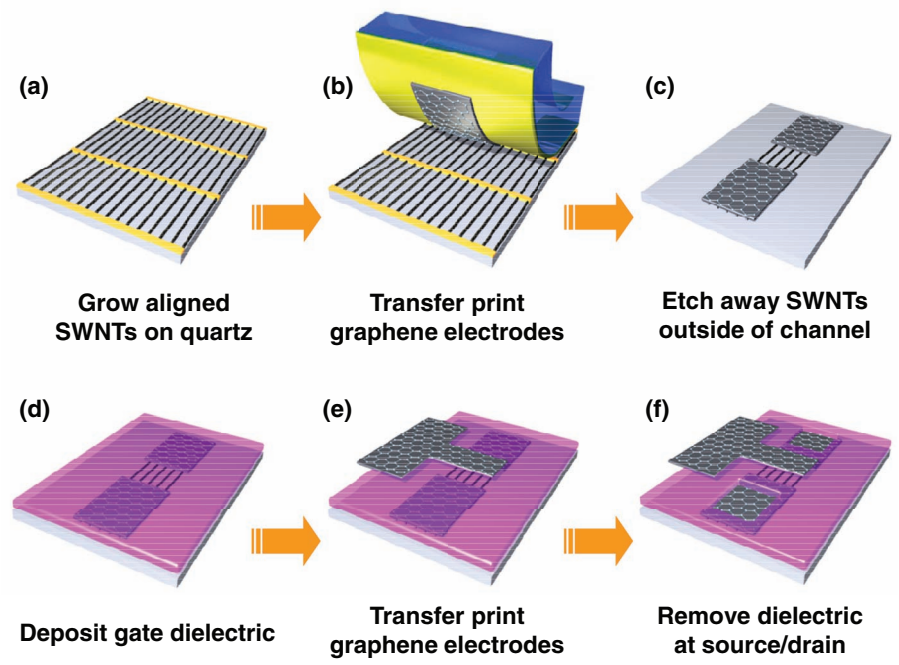

Figure 1. Schematic illustration of a process for integrating sheets of graphene and aligned arrays of SWNTs into devices and test structures. The first step, not shown explicitly here, involves the separate growth of graphene and SWNTs on SiO_2/Si and quartz substrates, respectively. Next, an aligned transfer printing procedure delivers patterned electrodes of graphene, along with the supporting layers of Au/PI, onto the SWNTs in the regions between adjacent catalyst lines. Wet and dry etching removes the Au and PI, respectively, to complete this first level of graphene/SWNT integration. Electrical isolation by patterned removal of the SWNTs with an oxygen plasma yields arrays of two terminal electrical devices. To fabricate transistors, a dielectric layer (HfO_2) is formed by electron beam evaporation and atomic layer deposition (ALD), and graphene gate electrodes are then transfer printed onto the channel region. Lastly, removing regions of the HfO_2 exposes the graphene source/drain electrodes for electrical probing.

the gate electrodes (Figure 1d,e). Patterned removal of HfO_2 exposes parts of the source/drain electrodes to enable electrical probing, thereby completing the fabrication (Figure 1f).

Figure 2a,b provide optical and atomic force microscopy (AFM) images of graphene transferred onto substrates of SiO_2/Si. All observed properties, ranging from the total thickness (0.6–2.0 nm) to the presence of small wrinkles, are consistent with previous reports.[16,17] The Raman spectra (Figure 2c, λ = 532 nm) exhibit typical features, including small D band intensity consistent with low levels of defects and local disorder. Figure 2d shows an optical microscopy image of such graphene in the form of patterned electrodes transferred onto aligned SWNTs on quartz. A representative channel region appears in the scanning electron microscopy (SEM) image of Figure 2e. Close examination by AFM (Figure 2f,g) suggests that the individual SWNT are conformally wrapped by the overlying graphene electrodes (Figure 2f) and that the SWNTs maintain excellent alignment throughout the process (Figure 2g). A pair of representative results of electrical measurements of these two channel devices at room temperature, before (solid circles) and after (open circles) thermal annealing at 1000 °C for 1 h in an Ar environment appear in Figure 2h, along with linear fits. To within measurement uncertainty, the structures exhibit a purely Ohmic response, with moderately reduced resistance for the annealed device. From such data, the inverse of the average conductance of an individual SWNT was found to be ≈200 kΩ μm^{-1}, which is comparable to previous reports.[11,20] A histogram of device resistances inferred from the slopes of curves such as those in Figure 2h appears in Figure 2i. The variations observed here result from differences in contact properties as well as variations in the number of SWNTs in each device, due to spatial non-uniformities in the densities of the SWNTs. The local density of SWNTs, determined by analysis of SEM images collected at various locations, ranged from ≈0.7 to ≈1.1 SWNT μm^{-1}. These variations account for most of the observed trends in the electrical data, where the deviations in resistance are ≈15% as shown in Figure 2i.

In particular, two-terminal devices with Pd–Pd, Pd–graphene, and graphene–graphene contacts were fabricated on the same set of aligned SWNTs as shown in Figure 2j. Pd contacts (Ti(1 nm)/Pd(40 nm)) were formed directly, using electron beam evaporated material and photolithography. Oxygen plasma etching of SWNTs through a photolithographically defined mask provided electrical isolation. An SEM image of the channel regions of all three devices appears in Figure 2k (Pd–Pd, Pd–graphene, graphene–graphene, each with channel lengths of ≈20 μm). Electrical measurements of a representative set of devices are presented in Figure 2l. Additional data can be found in the Supporting Information. In a study of seven sets of devices, those with graphene–graphene electrodes generated ≈10% higher current levels than their Pd–Pd counterparts utilizing identical SWNTs, indicating graphene as a slightly superior contact material.

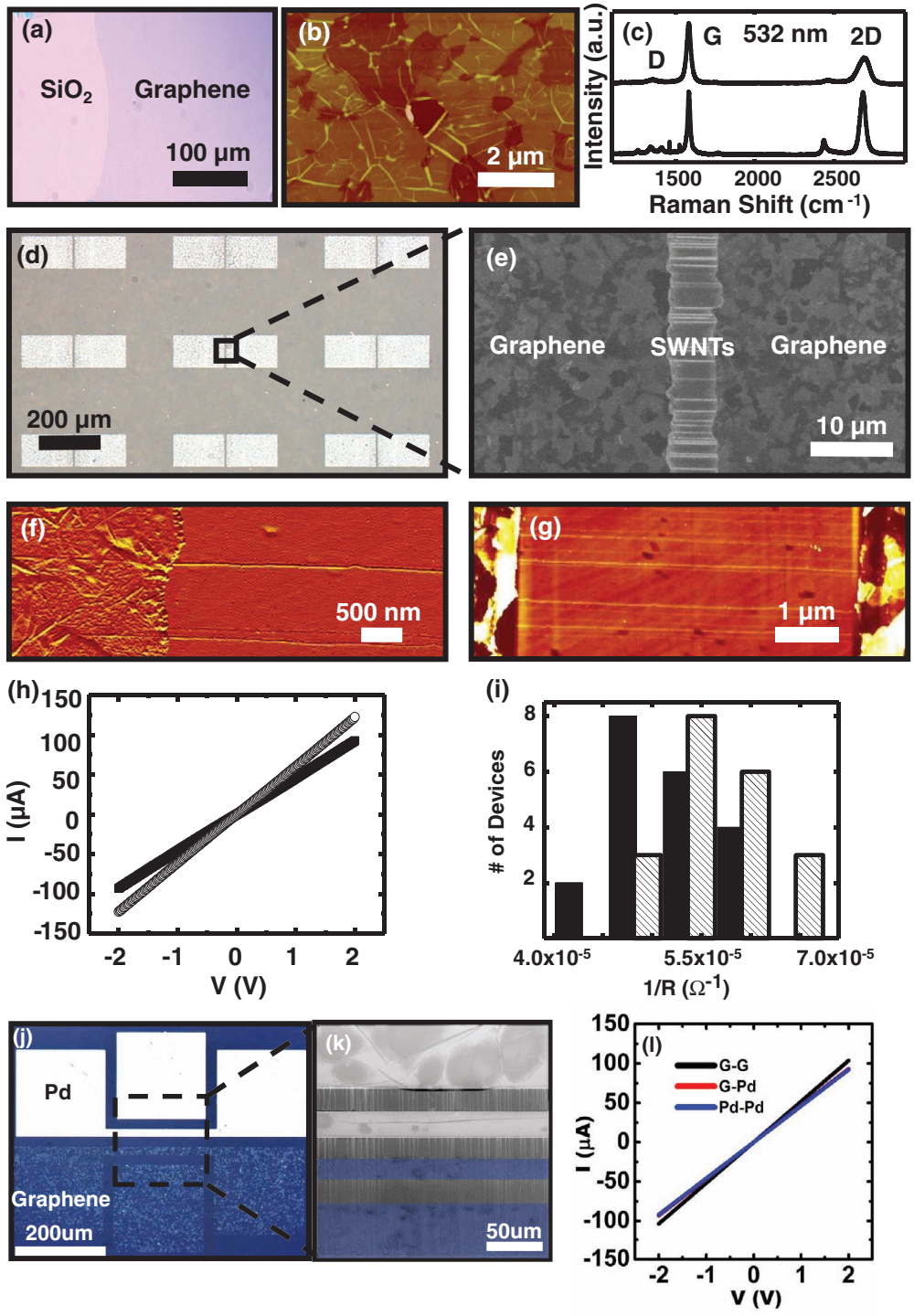

Figure 2. a) Optical image of a sheet of graphene on a SiO_2 (300 nm)/Si substrate, showing an edge and the underlying SiO_2 surface. b) AFM image, illustrating wrinkles. c) Raman spectra in the range of 1100–3000 cm^{-1}; the excitation wavelength is 532 nm. d) Reflection-mode optical image of pairs of graphene electrodes on aligned arrays of SWNTs on a quartz substrate. e) A magnified SEM image, marked in (d), provides a view of individual aligned SWNTs between two graphene electrodes. f) AFM image of junctions between graphene electrodes and SWNTs; the left side in the graphene region clearly shows the SWNTs embedded underneath the graphene electrode. g) AFM image of SWNTs between two graphene electrodes. h) Current density–voltage (*I–V*) characteristics for representative devices; linear fits define the effective resistance. i) Histogram of the resistance between pairs of graphene electrodes for devices before (black bars) and after (white bars) thermal annealing. j) Optical microscopy image of three, two-terminal devices with Pd–Pd, Pd–graphene, and graphene–graphene electrodes fabricated on the same set of aligned SWNTs. k) Colorized SEM image of the channel regions in which graphene and Pd appear blue and white, respectively. All devices have approximately 20 μm channel lengths. l) Representative *I–V* characteristics for devices similar to those shown on the left.

Figure 3a presents transfer characteristics of a representative transistor, without (solid circles) and with (open circles) thermal annealing (as described previously, performed before definition of the gate electrode and gate dielectric). The graph shows the drain current (I_d) as a function of gate voltage (V_g), for V_g between –3 and 3 V with a source/drain bias (V_{ds}) of 0.05 V. Here, the channel length, L_C, and the channel width, W, are 5 μm and 100 μm, respectively. The inset shows typical output characteristics (V_g: –3 to –1 V from the top, 0.5 V step). Consistent with the two terminal devices, transistors that were annealed exhibit improved currents, throughout the entire range of voltages. A potentially relevant aspect of these transistors for applications in display and other areas is that they are transparent over the entire visible range, as illustrated by the transmittance measurements in Figure 3b. The inset provides a picture of an array of devices positioned above printed characters on a white paper; the dashed box highlights the location of the transistors.

From the transfer curves, the linear-regime mobilities, μ can be calculated using the peak transconductance at a source/drain bias (V_{ds}) of 0.05 V and a rigorous capacitance model. Here, we define the effective field-effect mobility, μ as

$$\mu = \frac{L}{V_d C_w W} \cdot \frac{dI_d}{dV_g} \quad (1)$$

where C_W is the specific capacitance per unit area for the electrostatic coupling of the aligned arrays of SWNTs to the planar gate, according to the following expression[8,15]

$$C_w = \frac{D}{\left[C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_s} \cdot \log\left[\frac{\sinh(2\pi t D)}{\pi r D}\right]\right]} \quad (2)$$

where D is the density of the arrays of SWNTs per unit width, C_Q is the quantum capacitance, t is the distance to the gate dielectric, ε_0 is the permittivity of free space, ε_s is the dielectric constant of the gate dielectric, and r is the radius of the SWNTs. We consider only the semiconducting SWNTs for the estimation of D. For the dielectric constant of the hafnium oxide and the quantum capacitance of nanotubes, we used 10 and ≈3.2 × 10^{-10} F m^{-1}, respectively. Figure 3c shows calculated mobilities from devices with different channel lengths (i.e., L_C = 5, 10, 20; and 40 μm; 10 devices for each dimension) and W = 100 μm for all devices. The values are as high as ≈1000 cm^2 V^{-1} s^{-1} (median ≈800 cm^2 V^{-1} s^{-1}) and ≈900 cm^2 V^{-1} s^{-1} (median ≈ 780 cm^2 V^{-1} s^{-1}) with (open circles) and without (solid circles) thermal annealing, respectively.

The monotonic decrease in mobility with channel length evident in Figure 3c suggests non-negligible role of contacts in the device operation. However, since the electrodes correspond to relatively thick (≈2 nm), multilayer graphene films, electrostatic screening is expected to result in negligible field effect modulation of the sheet resistance, consistent with previous reports.[19] The ability to make large arrays of devices enables the study of this aspect, via scaling properties. Figure 3d provides a set of plots that correspond to transmission-line method (TLM) analysis of measured transfer curves. This analysis considers only scaling of the resistances associated with the semiconducting

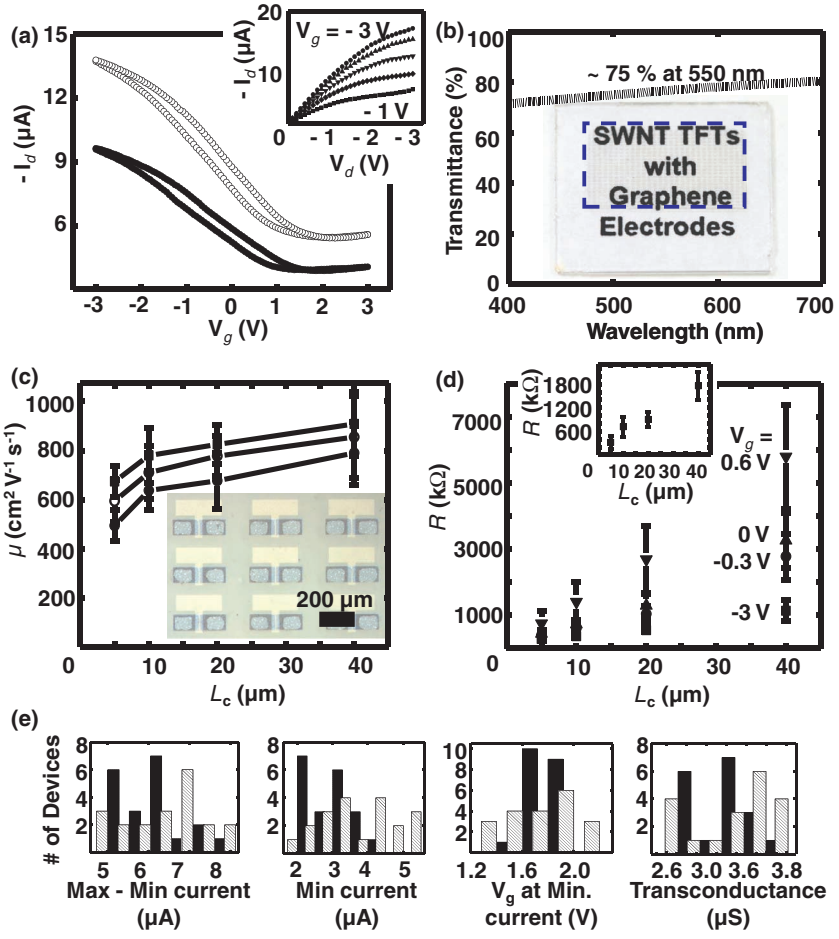

Figure 3. a) Drain current (I_d) as a function of gate voltage (V_g) for a source/drain bias (V_{ds}) of 0.05 V, measured on a transistor (L_C = 5 μm, W = 100 μm) that incorporates aligned arrays of SWNTs and graphene electrodes without (solid circles) and with (open circles) thermal annealing. The inset shows typical output characteristics (V_g: –3 to –1 V from the top, 0.5 V step). b) Optical transmittance of integrated SWNT–graphene transistors on a quartz substrate. The transmittance is ≈75% at a wavelength of 550 nm. The inset shows a picture; the dashed box area with faint grey color indicates the location of the arrays of transistors. c) Mobility versus channel length for such transistors, determined from measured transfer curves (open and solid circles for without and with thermal annealing, respectively) and rigorous capacitance models; channel widths of all devices are 100 μm. The inset shows an optical microscopy image (reflection-mode) of arrays of transistors on a quartz substrate with enhanced contrast. d) TLM plots extracted from the estimated contribution of semiconducting SWNTs to measured transfer curves, for L_C of 5, 10, 20, and 40 μm at V_g of –3, –0.3, 0, and 0.6 V. The inset shows a similar scaling plot for contributions from metallic SWNTs. e) Histograms of the difference in the maximum current (V_g = –3 V) and minimum current, minimum current, V_g at minimum current and transconductance extracted from the linear regime of transfer curves from each of 20 devices without (black bars) and with (white bars) thermal annealing.

SWNTs, for devices with a range of channel lengths (i.e., L_C = 5, 10, 20; and 40 μm; ten devices for each dimension) at different gate voltages (i.e., V_g = –3, –0.3, 0, and 0.6 V). Since the metallic SWNTs are, nominally, not modulated by the gate, we consider only semiconducting SWNTs in an approximate procedure that involves subtracting the minimum current (I_{off}), which occurs at V_g near 1.6 V for devices reported here, from the measured currents used in the TLM analysis.[20] The inset shows of the channel length dependence of resistances associated with the metallic SWNTs, inferred in this manner. The approximately zero intercept in this plot is consistent with negligible contact resistances to the metallic tubes. The slope and the estimated density of metallic SWNTs yield a resistance per unit length of ≈50 kΩ μm^{-1}, similar to previous reports.[14,20] Linear fits to the data of Figure 3d can be used to determine the graphene/SWNT contact resistance (from the intercept) and the effective mobility (from the slope) of the devices. Uncertainties in the data, resulting primarily from device to device variations in properties, frustrate precise determination of the contact resistances. We can conclude, however, that the gate modulation of the contacts plays a negligible role in device operation, and that the resistance is in the same range as that observed in otherwise similar devices that use Pd for contacts.[20] The slopes of the curves in Figure 3d yield an estimate of the mobility that accounts for the effects of contacts. The value determined in this manner, ≈1200 cm^2 V^{-1} s^{-1}, is consistent with values in the long channel length limit (Figure 3c) and previous reports.[20]

The histograms in Figure 3e summarize statistical properties for 20 devices (L_C = 5 μm; W = 100 μm) without (black bars) and with (white bars) thermal annealing. Metrics for comparison include the difference in the maximum and minimum current levels (corresponding, approximately, to current through the semiconducting SWNTs), the minimum current (corresponding, approximately, to current through the metallic SWNTs), V_g at minimum current and the transconductance. As for the two terminal devices, most of the variations observed here can be associated with spatial variations in the density of the SWNTs. Also, annealing tends to increase contributions of current flow through metallic and semiconducting tubes by roughly the same amount, ≈25%. We observe no significant change for V_g at minimum current or transconductance.

In summary, this paper demonstrates the use of transfer printing techniques to achieve monolithic integration of graphene sheets and aligned arrays of SWNTs, including demonstrations in transistors and two terminal devices. These results suggest that SWNTs and graphene films can be combined effectively to yield functioning devices, useful for study of basic properties and with some potential for applications. In addition, graphene/SWNT transistors can exploit the unique optical (i.e., transparency) and mechanical (i.e., high strain at fracture) properties of graphene without any significant sacrifice in performance compared to more conventional devices built with Pd electrodes. The same procedures should also be applicable to multilayer configurations, crossed junctions, and other layouts that incorporate graphene and SWNTs in integrated forms that are more complex than those illustrated here.

Experimental Section

Synthesis of Aligned Arrays of SWNTs: ST-cut single crystal quartz substrates (Hoffman Materials, Inc.) were thermally annealed in air at 900 °C for 8 h. Narrow stripes of Fe catalysts (1–5 Å) were deposited by electron beam evaporation (Temescal BJD1800) and patterned using photolithography (AZ 5214). Heating the prepared substrate at 900 °C for 1 h in quartz reaction chamber oxidized the Fe catalysts. After slowly cooling the substrate to room temperature, heating to 925 °C under hydrogen gas flow with 400 sccm for 10 min fully reduced the catalyst. CVD growth was performed for 20 min with a mixture gas flow of Ar (20 sccm) and H_2 (20 sccm), introduced through an ethanol bubbler at 925 °C, yielded aligned arrays of SWNTs.

Synthesis of Graphene and Transfer Printing Process: Catalytic Ni films (300 nm) were prepared by electron beam evaporation (Temescal BJD1800) on thermally grown SiO_2 on silicon wafers. Substrates prepared in this manner were annealed at 950 °C for 30 min under the gas flow condition of Ar (900 sccm) and H_2 (700 sccm) through a quartz reaction chamber. Next, CVD growth was performed for 3 min at 965 °C with a mixture gas flow of Ar (300 sccm), H_2 (200 sccm), and methane (10 sccm) followed by fast cooling at ≈8 °C s^{-1} to precipitate graphene on the surface of the Ni film.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

S.W.H. and F.D. contributed equally to this work. The authors thank T. Banks for help with processing using facilities at the Frederick Seitz Materials Research Laboratory. This material is based upon work supported by the U.S. Department of Energy (DE-FG02-07ER46471), MITRE Corp., Northrop Grumman, the Frederick Seitz Materials Research Lab and the Center for Microanalysis of Materials (DE-FG02-07ER46453 and DE-FG02-07ER46471) at the University of Illinois. This research was supported by a grant from Center for Nanoscale Mechatronics & Manufacturing, one of the 21st Century Frontier Research Programs, which are supported by Ministry of Science and Technology, Korea.

Received: May 25, 2011
Published online: July 22, 2011

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