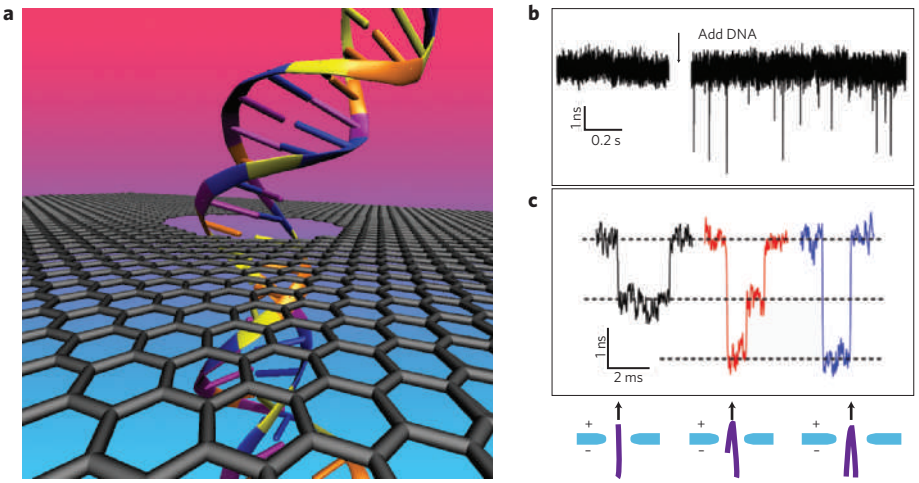

Figure 2 | Translocation of DNA through a graphene nanopore. **a**, Double-stranded DNA threading a graphene nanopore. Each coloured segment represents a different nucleotide. The software VMD 1.8.7, PyMOL1.2r1, and TubeGen 3.3 was used in preparation of the image. **b**, Characteristic conductance versus time signals of a graphene nanopore before and after the addition of DNA. **c**, The conductance signature (top) of various DNA conformations (bottom) as they translocate through a graphene nanopore. Parts **b** and **c** reproduced with permission from ref. 7, © 2010 ACS.

MIT team observed that although the ion permeability of an intact graphene membrane was negligible compared with that of a membrane that contained a nanopore, it was not zero and it was different for different cations, which indicates that electrolyte–graphene interactions need to be taken into account[6]. Evidence of DNA–graphene interactions was also observed[6–8]. These interactions will need to be carefully understood if an ionic-current-based DNA sequencing algorithm is to be employed.

Perhaps the most striking question that arises from these reports relates to the dimensionality of the graphene pore: the pore was seen to behave as both a cylinder of finite length (with its conductance being proportional to the square of the diameter)[7] and as an infinitesimally thin circular aperture (with conductance proportional to diameter)[6].

This work on graphene nanopores is certain to be the precursor to further studies in a variety of fields. Within the scope of nanopore sensing, there are numerous avenues to explore using the graphene itself as an electrode to control the local electric potential and translocation rates, or to monitor the transverse conductance of individual nucleotides as they pass through a pore[9]. Previous theoretical work suggests that the latter technique, if used in the proper geometry, could provide DNA sequencing with a 0% error rate[10]. Combined with recent advances in the production of large-area high-quality graphene (sheets with up to a 30-inch diagonal)[4], the results open the door to a host of interesting explorations including the development of new membrane systems for biosensing. ❐

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NANOELECTRONICS

Nanoribbons on the edge

Arrays of graphene nanoribbons are fabricated on structured silicon carbide substrates using self-organized growth, without lithography and with well-controlled widths.

John A. Rogers

Graphene is attractive for electronics because of its exceptional properties and the relative ease with which it can be integrated into transistors and circuits. In the form of large-area planar sheets, it can be processed using straightforward adaptations of methods that are already in widespread use by the semiconductor industry. However, graphene in its native single-layer form has zero electronic bandgap, which prevents transistor devices made with it from being turned off completely. This makes graphene unusable in power-efficient digital circuits (though it can still be used in radio frequency electronics)[1]. Narrow graphene ribbons have better switching capabilities, but they are difficult to manufacture owing to the very small widths that are required. Writing in *Nature Nanotechnology*, Michael Sprinkle, Walter de Heer and colleagues at the Georgia Institute of Technology and the Institut Néel in Grenoble report a clever growth technique that yields organized, aligned arrays of narrow ribbons of graphene on structured substrates of silicon carbide (SiC), with the potential to enable switching properties suitable for broad classes of electronic systems[2].

Early theoretical work suggested that graphene ribbons would have bandgaps large enough to allow efficient transistor switching[3]. However, practical circuits require very narrow widths (less than ~10 nm), with exceptional uniformity in the lateral dimension, and well-ordered edges. Recent reports suggest that such ribbons can be achieved by ultrasonic tearing and exfoliation of larger sheets[4], chemical 'unzipping' of carbon nanotubes[5] and covalent linking of assemblies of molecular building blocks[6]. In their present state of development, however, these strategies do not offer the levels of engineering control over dimensions or spatial layouts needed for realistic applications. Lithographic

etching of large sheets represents an attractive alternative because it is able to achieve uniform, organized arrays[7]. Unfortunately, the complexity of the tools necessary for sub-10-nm patterning and an inability to control edge roughness represent significant limitations to this technique.

Sprinkle, de Heer and colleagues report progress towards a very different approach, in which ribbons are grown directly into the desired layout and with a controlled width[2]. Their methods build on techniques that they pioneered, wherein thermal decomposition of silicon-terminated SiC wafers yields uniform sheets of graphene[8]. This team now incorporates two new steps that exploit subtle aspects of the crystalline SiC substrates. First, they etch shallow trenches into the surface of a SiC wafer along a particular crystal axis. On thermal annealing, the vertical sidewall edges of these trenches reconstruct into smooth facets, angled at ~25° above the substrate surface. The key feature of this transformation is that the depth of the trench determines the width of its facets: for example, trench depths of 20 nm yield facet widths of 40 nm. This converts the difficult problem of sub-50-nm lithography into the comparatively easy task of controlling etch depth.

The next step exploits the fact that graphene grows at different rates on different crystal faces of SiC. By orientating their trenches in an appropriate direction, Sprinkle and colleagues create facets that form graphene more quickly than surrounding regions do, possibly owing to different bonding of the silicon atoms. As a result, for short growth times, graphene forms predominantly on the facets. Combined with a fine control over facet width, this process allows the formation, in a single growth step, of organized arrays of graphene ribbons with widths that begin to approach those needed for applications in digital electronics, and with edges that are unaltered by etching processes.

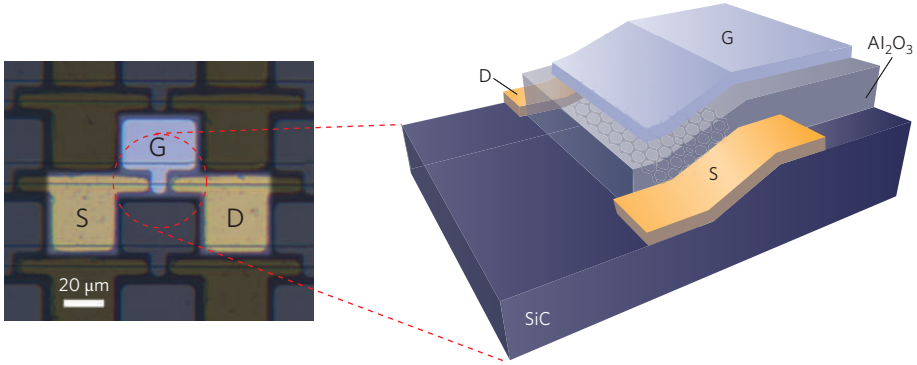

Figure 1 | An array of transistors that use graphene nanoribbons grown directly into place on the faceted step edges of a SiC wafer. Etching a shallow trench followed by annealing yields a smooth, angled facet on which graphene (shown here as a grey hexagonal lattice) grows more quickly than on adjacent surfaces (right). Adding a gate insulator (Al_2O_3) and source (S), drain (D) and gate (G) contacts completes the transistor.

The research team use their new technique[2] to build an array of 10,000 transistors, arranged in practical circuit geometries. Although the measured field-effect mobility is in the same range as other published ribbon devices, it is less than a tenth of the best substrate-supported graphene-sheet devices. Also, the smallest achieved widths are still much too wide for practical use, giving on/off switching ratios that are too low by several orders of magnitude. Sprinkle and colleagues suggest that these shortcomings can be addressed by optimizing their technique.

Future work in this direction looks very promising because the procedure seems to be scalable to much finer feature sizes, and optimized device designs are likely to lead to improvements. Meanwhile, other approaches to graphene ribbon fabrication are becoming more sophisticated, and techniques to produce aligned arrays of single-walled carbon nanotubes continue to develop (also using tricks enabled by substrate crystallinity[9–12]). The diversity of fabrication ideas together with the potential for important applications guarantees that the field of carbon nanomaterial electronics will remain an active one for years to come. ❐

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NANOMATERIALS

Graphene rests easy

Samples of graphene supported on boron nitride demonstrate superior electrical properties, achieving levels of performance that are comparable to those observed with suspended samples.

R. Thomas Weitz and Amir Yacoby

The impressive electronic properties of graphene result from the perfection of its hexagonal crystal lattice. However, the interaction of this pristine lattice with a disordered environment can alter its properties. For example, even the simple act of resting graphene on a substrate causes a precipitous decline in its mobility. As a result, measuring its intrinsic properties remains very much an art, and the highest mobilities have been observed in samples suspended in free space between pairs of electrodes. Writing in *Nature Nanotechnology*, Cory Dean, Jim Hone and colleagues at Columbia University in the