Electrically interconnected assemblies of microscale device components by printing and molding

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This letter presents approaches for assembly and electrical interconnection of micro/nanoscale devices into functional systems with useful characteristics. Transfer printing techniques provide deterministic control over an assembly process that occurs prior to or simultaneously with a soft lithographic molding step that defines relief features in a receiving polymer. Filling these features with conducting materials that are processable in the form of liquids or pastes yields integrated interconnects and contacts aligned to the devices. Studies of the underlying aspects and application to representative systems in photovoltaics and solid state lighting indicators provide insights into the process and its practical use. © *2009 American Institute of Physics*. [doi:10.1063/1.3268464]

Unusual microsystems for electronics/optoelectronics, solid state lighting, and photovoltaics can be formed with assemblies of micro/nanoscale components or material elements to achieve system level outcomes that are not possible using conventional approaches. Examples include flexible/stretchable designs,[1,2] curvilinear layouts,[3,4] and systems that exploit heterogeneous materials integration[5,6] in two- or three-dimensional layouts.[5–7] The assembly process can occur either by deterministic methods based on transfer printing[8,9] or guided approaches based on fluidic delivery and surface/shape recognition.[10,11] In all cases, electrically interconnecting the assembled devices to form integrated systems represents a practically challenging aspect of the fabrication, particularly for systems in solid state lighting and photovoltaics, where long interconnect wiring traces with minimal resistances are required. The most straightforward and widely explored approaches rely on conventional techniques, such as photolithography, to pattern uniform layers of metal formed by vacuum deposition (possibly followed by electroplating). The cost structures, however, preclude their use in many systems of interest. Conventional soft lithographic methods can be used, but their application over surface topography associated with assembled device components can be difficult. Screen printing[12] or ink jet printing[13,14] of pastes or liquid suspensions of conductive particles provide alternatives but their modest resolution limits the utility. Recent techniques that rely on electrohydrodynamic jet printing[15,16] or direct writing[17] avoid these problems. Achieving adequate throughput with these serial methods and developing them into forms suitable for realistic application are subjects of current work. The research described here provides a simple scheme designed specifically to address the classes of systems described above; it combines aspects of transfer printing for assembly,[8,9] with soft imprint lithography[18] and certain features of screen printing[12] for contacts and interconnect. In the following, we examine the basic features of this method, and demonstrate its application to representative systems of interest in monocrystalline silicon photovoltaics and AlInGaP lighting indicators.

Figure 1 presents a schematic illustration of the process, in which transfer printing for device placement and molding for electrical interconnect occur simultaneously. The initial step involves fabricating the devices [i.e., square blocks with rectangular electrode pads; Fig. 1(a)] on a source substrate using procedures discussed subsequently in the context of different demonstration examples. Next, techniques for trans-

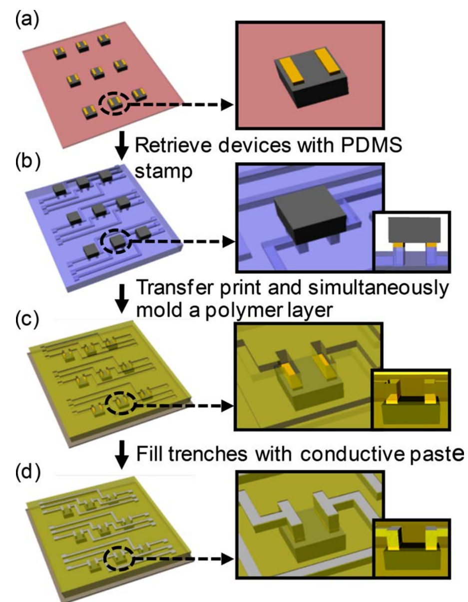

FIG. 1. (Color online) Schematic illustration of procedures for printing and interconnecting microscale device components. (a) Fabrication of devices (square blocks with rectangular electrodes) on a source substrate. (b) An elastomeric stamp retrieves a collection of these devices. (c) Bringing the stamp, "inked" with devices in this manner, into contact with a layer of liquid prepolymer, followed by curing to a solid form yields a molded structure with integrated, embedded devices. (d) Scraping a conductive paste over this structure fills the molded features.

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fer printing[8,9] lift these devices onto an elastomeric stamp/mold with relief that defines contacts to the electrode regions and trenches for interconnect. In this example [Fig. 1(b)], the relief consists of two different levels such that the devices rest with their electrodes in contact with the highest features; the others are associated with interconnect. The stamp/mold "inked" with devices then contacts a thin layer of a liquid prepolymer cast on a target substrate. Allowing this liquid to flow and conform to the relief, photochemically or thermally curing it into a solid form and then removing the stamp/mold yields the structure illustrated in Fig. 1(c). The polymer acts as an adhesive and an encapsulant for the devices, with molded features that define the geometry of the interconnect wiring. Scraping a conductive paste over the top surface using methods operationally similar to those for screen printing[12] fills the recessed regions in the molded polymer to form these interconnects [Fig. 1(d)]. For the experiments described in the following, a photocurable polyurethane (PU; NOA61, Norland Products Inc.) and a silver epoxy (H20E Epo-Tek®, Ted Pella Inc.) served as the mold material and the conductive paste, respectively. We used the casting and curing procedures of soft lithography to form stamps/molds of the elastomer poly(dimethylsiloxane) (PDMS; Sylgard, Dow Corning).

The molding step relies on established methods for soft imprint lithography, as described elsewhere.[18] Concepts for using the molded features as trenches to be filled with conductive pastes, and accomplishing the molding at the same time as printing are both unusual aspects of the process reported here. The filling procedures involve dispensing a line of silver epoxy along one edge of a flat region of the substrate. As an implement for scraping this epoxy over the surface, we used a slab of PDMS roughly 3 cm long, 1 cm thick, and with a width somewhat larger than that of the molded substrate. This element has a ~45° beveled edge, similar to squeegees used for screen printing. Scraping this edge across the substrate at an angle of ~30° several times filled the trenches with epoxy and left only small amounts of residue on the top surfaces. Scraping several additional times with another PDMS element soaked in acetone removed these residues. Figure 2(a) shows a pattern of conducting features formed in this fashion on a molded layer of PU (20 μm depth) on a substrate of polyethylene terephthalate (PET). These results illustrate the range of feature sizes (linewidths 20–200 μm, lengths 0.2–2.0 mm, in straight, curved and zigzag geometries) and shapes that can be formed easily, and the good levels of uniformity that are possible. The limit of resolution is determined by the sizes of particles in the silver epoxy (10–15 μm), rather than by the fidelity in the molding step. Figure 2(b) shows cross sectional views of lines formed with aspect ratios (depth to width) of 1 and 0.1. The limits at the high and low ends of this range are defined, respectively, by inability to push epoxy into deep, narrow features, and tendency to scrape it completely away from the center regions of shallow, wide features. Decreasing the viscosity and particle sizes in the epoxy can extend the former limit; increasing the stiffness of the slab of material (PDMS in this case) used to scrape the epoxy into the grooves can improve the latter. Independent of dimension in the acceptable range, we found values of electrical resistivity ($3.0–6.0 \times 10^{-4}$ Ω cm) roughly two orders of magnitude higher than bulk silver (1.6×10^{-6} Ω cm), for curing tem-

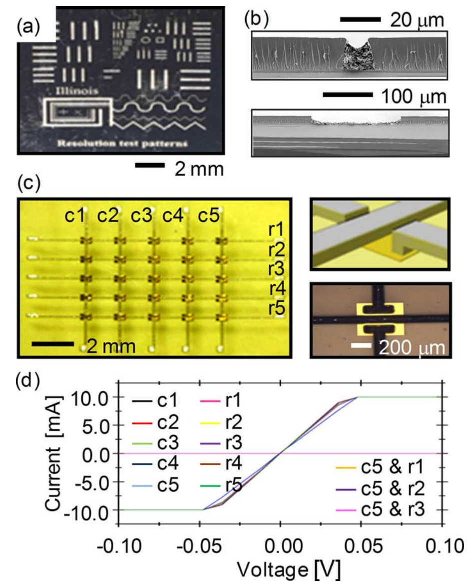

FIG. 2. (Color online) (a) Optical image of a collection of conducting features formed by molding a layer of PU on a PET substrate, and then filling the resulting trenches with silver epoxy. (b) Cross-sectional SEM images of filled lines with depths of 20 μm and widths of 20 μm (top) and 200 μm (bottom). (c) Interconnected arrays of metal pads with crossed but electrically isolated conducting lines on a PET substrate. The right top and bottom frames provide a schematic cartoon illustration and a top view optical micrograph, respectively, of the structure near a representative pad. (d) Current/voltage data collected by probing contact pads to different combinations of row (r1, r2, etc) and column (c1, c2, etc) interconnect lines verifies electrical continuity along columns and rows and electrical isolation between columns and rows.

peratures of 150 °C and times of 5 min, consistent with specifications from the vendor. Contacts to devices and electrical crossovers can be formed in the manner of Fig. 1. Figure 2(c) shows such an example, where metal pads (Cr/Au, 100/1000 nm; 500×500 μm) formed in a square array (1.5 mm pitch) on a PET substrate provide an equivalent of the devices in Fig. 1. Defining trenches in PU using a stamp/mold with a design similar to that of Fig. 1 followed by filling with silver epoxy yielded the structure shown in the image of Fig. 2(c). The right top and bottom frames provide a schematic cartoon illustration and a top view optical micrograph, respectively. The lines here have widths of 100 μm and depths of 20 μm. The contacts to the electrode pads are defined by molded features with depths of 40 μm and lateral dimensions of 100×300 μm. Current/voltage data [Fig. 2(d)] collected by probing contact pads to different combinations of row (r1, r2, etc) and column (c1, c2, etc) electrodes verify electrical continuity along given columns and rows and electrical isolation (i.e., >gigaohm) between all other pairs of lines.

To demonstrate this concept in real devices, we used AlInGaP light emitting diodes (LEDs; 250×250 μm) formed in ultrathin (2.5 μm thick) layouts using procedures described elsewhere.[19] Here, the printing step to transfer these devices from a GaAs wafer to a glass substrate occurred first, followed by molding to define contacts and interconnect. Figure 3(a) shows a set of nine such LEDs, with an independent pair of electrical leads to each. The top inset provides a top view optical micrograph. The three devices in the middle were connected to a power supply to induce light emission, for the purpose of illustration. The current/voltage characteristics are similar to those observed in devices

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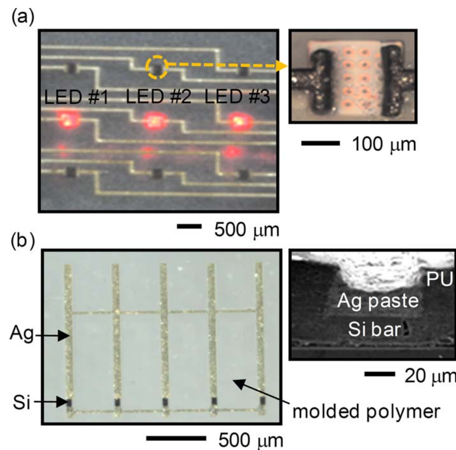

FIG. 3. (Color online) (a) Optical image of a set of nine AlInGaP light emitting diodes formed in ultrathin layouts and pairs of molded interconnect lines leading to each. Selective printing formed the arrays; aligned molding followed by filling with silver epoxy formed the interconnects. The top inset provides a top view optical micrograph. The three devices in the middle were connected to a power supply to cause light emission. (b) Optical image of a photovoltaic minimodule consisting of five monocrystalline bars of silicon with integrated contacts. The inset shows a cross sectional view of part of the structure.

(nonohmic contacts) interconnected with conventional procedures of photolithography and liftoff described elsewhere.[19]

Microscale monocrystalline silicon solar cells provide another device example. Here, a collection of five such cells were formed into an interconnected array for a minimodule using the schemes as shown in Fig. 1, where printing and molding occurred simultaneously. The process steps for fabricating the cells appear elsewhere.[20] Each cell consists of a bar of monocrystalline silicon (width, length, and thickness of 50 μm, 1.55 mm, and 20 μm, respectively) with ohmic contacts of metal (Cr/Au, 100/1000 nm; 50 μm width, and 100 μm length for the p contact; 50 μm width, and 1.4 mm length for the n contact). Figure 3(b) shows a sample, with an inset that provides a cross sectional view of part of the structure. In these systems, illumination occurs through the backside surface of the transparent substrate; the interconnect lines and metal layers serve as reflectors. The efficiency (E_{ff}) and fill factor (FF) of this solar cell, corresponding to measurement on all five interconnected cells in the module, were 6.5% and 0.61, respectively, obtained using standard procedures and considering only the geometrical sizes of the cells (not explicitly separating flux from the sidewalls). These properties are in the same range as those of arrays of similar devices interconnected using conventional procedures.[20]

In summary, the procedures reported here might provide an attractive solution to electrical interconnection of classes of systems that incorporate assemblies of micro/nanoscale devices or material elements. Although their use in prototype devices for photovoltaics and lighting indicators demonstrates the key aspects, the same methods can also be used to establish electrodes and/or interconnects in related systems that use other micro/nanoscale material elements, such as nanowires, nanomembranes, and nanotubes.[5–7] The printing and molding can occur either sequentially or simultaneously, depending on requirements. The final, embedded configurations of the devices that result from this process have practical advantages for encapsulation. The ultimate limits in the resolution are defined by the soft imprint molding procedures (e.g., ~1–2 nm for PDMS molds)[18] and the conductive pastes (e.g., 5–100 nm for Au or Ag nanoparticles).[21] Use in realistic applications will also be limited by achievable registration of the stamp/mold elements to the device components or material elements. Flexible sheets of plastic or glass can form support structures for thin layers of PDMS, to reduce distortions to one or two micron levels over areas of hundreds of square centimeters, or larger.[22] The characteristics of the methods reported here, their simplicity and potential for low cost operation over large areas, and the diversity of materials and devices with which they can be applied suggest a potential for broad utility.

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