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Flexible electronics

Optimized Structural Designs for Stretchable Silicon Integrated Circuits

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***M**aterials and design strategies for stretchable silicon integrated circuits that use non-coplanar mesh layouts and elastomeric substrates are presented. Detailed experimental and theoretical studies reveal many of the key underlying aspects of these systems. The results show, as an example, optimized mechanics and materials for circuits that exhibit maximum principal strains less than 0.2% even for applied strains of up to ≈90%. Simple circuits, including complementary metal–oxide–semiconductor inverters and n-type metal–oxide–semiconductor differential amplifiers, validate these designs. The results suggest practical routes to high-performance electronics with linear elastic responses to large strain deformations, suitable for diverse applications that are not readily addressed with conventional wafer-based technologies.*

Keywords:
- flexible electronics
- nanomaterials
- nanomechanics
- semiconductors
- stretchable electronics

1. Introduction

Electronic circuits that offer the performance of conventional wafer-based devices but with the mechanical properties of a rubber band have the potential to open up many new application possibilities, most prominently those that involve intimate integration of electronics with the human body[1] for health monitoring or therapeutic purposes. Several schemes

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have been demonstrated to achieve stretchable circuits, as defined by reversible, elastic mechanical responses to large ($\gg$1%) compressive or tensile strains.[2–11] Those that exploit single-crystalline semiconductor nanomaterials, in the form of nanoribbons or nanomembranes, are attractive due to the excellent electrical properties that can be achieved. The most advanced strategies use single crystal silicon for the active materials of ultrathin devices (e.g., transistors) that are interconnected (mechanically and/or electrically) with non-coplanar bridges to provide stretchability up to ≈100% in a manner that maintains small material strains for linear, reversible response and good fatigue properties.[11] In the present paper, we study theoretically and experimentally many of the key design variables including aspects of bridge design and encapsulation. The results reveal important features of the underlying materials and micro-/nanomechanics and provide design rules for this class of stretchable electronics technology.

2. Results and Discussion

The process for fabricating stretchable silicon circuits is similar to that of recent reports.[8,11] Figure 1 provides an overview for systems that use non-coplanar serpentine bridge structures. The sequence begins with high-temperature doping processes, starting with an n-type silicon on insulator(SOI) wafer wafer (260-nm top silicon, 1-μm buried oxide; SOITEC, France), as shown in Figure 1a. Doped silicon nanomembranes prepared in this manner are transfer-printed onto a carrier wafer coated with poly(methyl methacrylate)/polyimide (PMMA/PI, 100 nm/1.2 μm, MicroChem/Sigma Aldrich, USA) and then processed to yield ultrathin circuits (Figure 1b). Details appear in the experimental section. Another transfer printing step lifts the ultrathin circuits from the carrier wafer to expose their back surfaces for selective area deposition of Cr/SiO_2 (3 nm/30 nm) through an aligned shadow mask (Figure 1c) and then delivers them to a biaxially pre-strained piece of poly(dimethyl siloxane) (PDMS, Dow Corning, USA) bearing –OH groups on its surface. Strong covalent bonding forms between the PDMS and the SiO_2 on the circuits upon contact and mild heating (Figure 1d). This bonding, together with the comparatively weak van der Waals adhesion between the PDMS and other regions of the circuits, leads to a controlled non-coplanar layout in which the bridge structures lift out of contact with the PDMS upon release of the pre-strain (Figure 1d).

Systematic study of this system began with investigations of the dependence of the mechanics on the bridge design, as shown in Figure 2. Figure 2a shows a standard serpentine structure of low amplitude (A)-to-wavelength (λ) ratio and wide width (w) formed with a pre-strain value of ≈30%. The pre-strain is estimated using the change of distance between each island. For an applied strain of ≈90%, the bridge changes shape to first reach its original layout when the applied strain equals the pre-strain, followed by further deformation at higher strains without fracture. This ability to accommodate strains larger than the pre-strain is absent from straight bridge designs explored previously.[10,11] Nevertheless, the serpentine layout

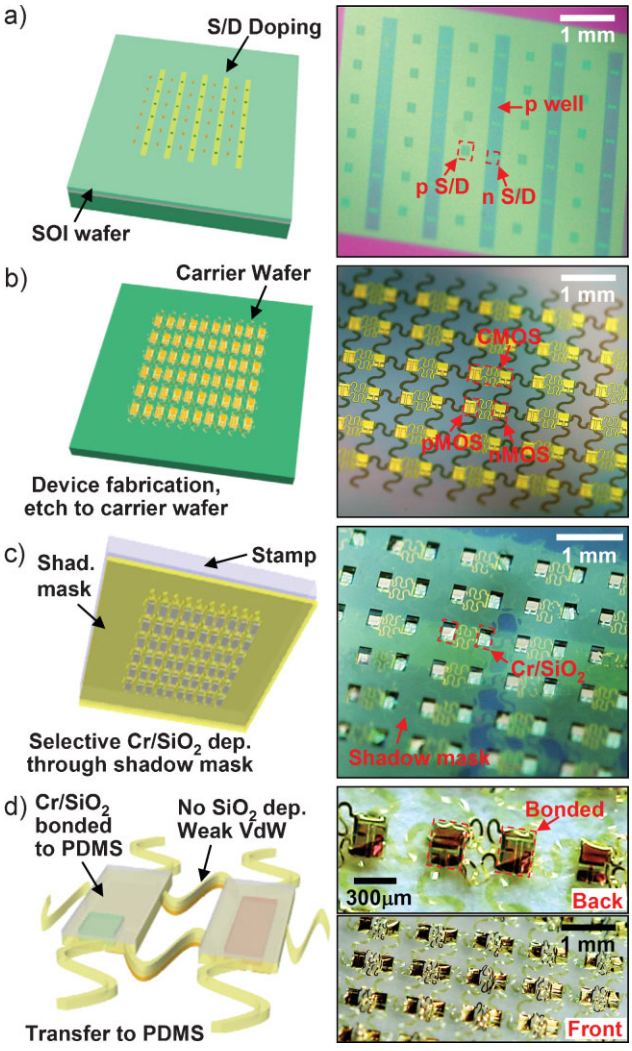

Figure 1. Schematic illustrations (left) and corresponding optical images (right) of a) doped silicon, b) interconnected arrays of CMOS inverters, c) lifted inverters covered with a shadow mask for selective deposition of Cr/SiO_2, and d) magnified views of an inverter.

of Figure 2a exhibits stress concentrations near the corners of the points of highest curvature, suggesting the possibility for mechanical failure in these regions. Full 3D finite element modeling (FEM) analysis (bottom frames in Figure 2a) indicates a maximum principal strain of ≈1.7% for an applied strain of ≈90%. A different design, (Figure 2b), which increases the A-to-λ ratio of the serpentine structure, reduces the maximum principal strain to 1.26% under the same applied strain. Extending this strategy by decreasing w of the lines and increasing the number of "coils" in the serpentines while maintaining the A-to-λ ratio (Figure 2c) dramatically reduces the maximum principal strain to 0.13% for the same conditions. This simple sequence of structural modifications illustrates the extent to which design influences the micromechanics. Further reduction in bridge thickness and longer serpentine interconnects can decrease the maximum principal strain. Detailed quantitative scaling with such variables can be determined by FEM. Results depend, however, on many details associated with system design and layouts.

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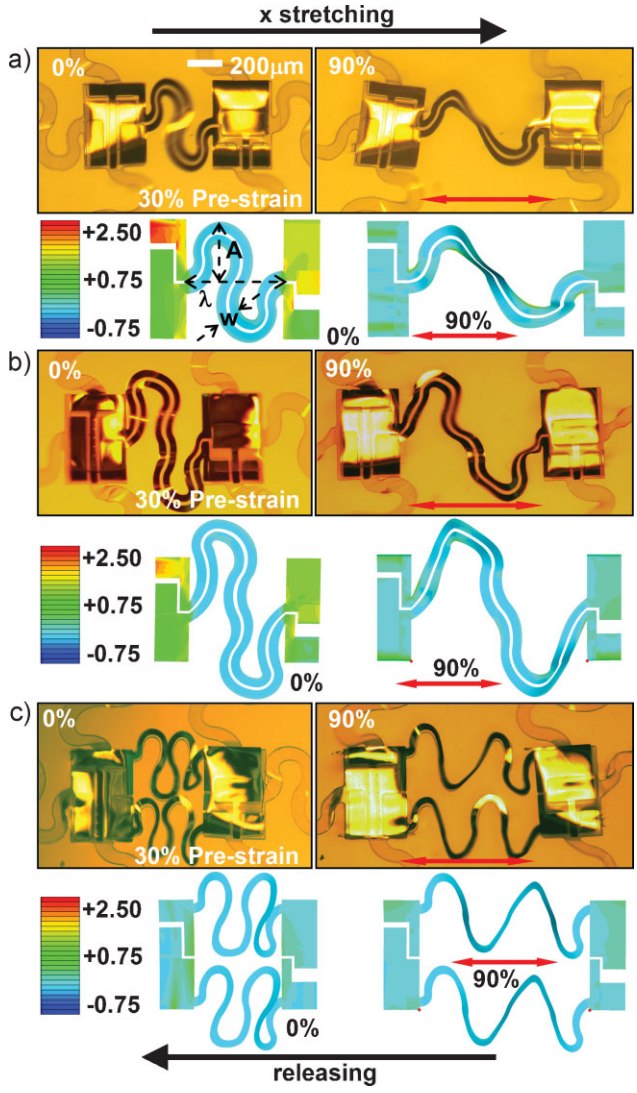

Figure 2. Optical microscopy images and maximum principal strain distributions (in percent) evaluated by FEM simulation for a CMOS inverter with a) a standard serpentine interconnect, b) an interconnect with large *A*, and c) an interconnect with large *A*-to-λ ratio, narrow *w*, and large number of curves. Red arrows in right figure denote the stretching direction.

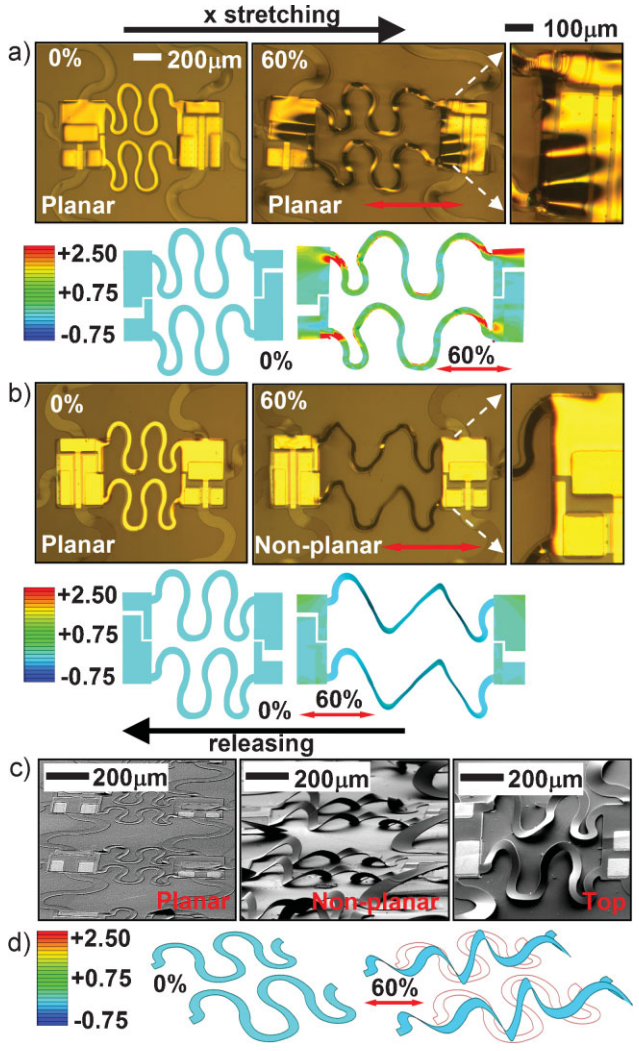

Figure 3. Optical microscopy images and maximum principal strain distributions (in percent) computed by FEM simulation for a CMOS inverter with a) coplanar and b) non-coplanar structure, c) SEM images for (b) before (left) and after (center and right) applying external strain, d) FEM simulation for (b) before (left) and after (right) applying external strain.

Another critically important feature of systems of this type is the non-coplanar layout of the serpentines. To reveal the effects Figure 3 compares coplanar (formed with the Cr/SiO_2 adhesion layer deposited uniformly on the backsides of the circuits to bond the serpentines as well as the islands to the PDMS) and non-coplanar systems with the bridge design of Figure 2c. For simplicity of comparison, the pre-strain was zero for both cases, leading to identical strain distributions for the unstrained cases shown in the left frames of Figure 3a and b. With an applied tensile strain of ≈60%, the bridges in the coplanar case remain largely flat due to their adhesion to the PDMS substrate. By contrast, the bridges of the non-coplanar case delaminate from the PDMS and move out of the plane to accommodate more effectively the applied strain. Figure 3c shows this behavior in scanning electron microscopy (SEM) images. The left frame (60° tilted) corresponds to the system without applied strain; the center (60° tilted) and right (top view) frames are for strains of 60%. In the case of coplanar bridges, the constrained motion leads to much higher peak strains in the circuits compared to the non-coplanar design. As a result, cracks and wrinkles appear inside the active device regions, unlike the non-coplanar system, as shown in the center and right images of Figure 3a and b. The strain distributions and maximum principal strains calculated by FEM analysis confirm these experimental observations (bottom frames of Figure 3a and b). The maximum principal strains under applied strains of ≈60% for coplanar and non-coplanar structures are 6.8% and 0.177%, respectively. Figure 3d shows tilted views of the FEM simulation results for the non-coplanar structure before and after applying strain.

To illustrate the value of these simple, optimized designs, we built complementary metal–oxide–semiconductor (CMOS) inverters and n-type metal–oxide–semiconductor (NMOS) differential amplifiers. The inverters exhibited gains as high as

≈130, consistent with PSPICE simulation based on separate measurements of individual transistors (Figure 4b, left) that showed mobilities of ≈400 and ≈160 $cm^2\ V^{-1}s^{-1}$ for NMOS and PMOS devices, respectively, and on/off ratios $>10^5$ for both types of devices (Figure 4c, inset). The inverters incorporated devices with channel lengths and widths of 13 μm and 100 μm for NMOS and 13 μm and 300 μm for PMOS, respectively. For both devices, 40-nm plasma-enhanced chemical vapor deposition (PECVD) SiO_2 was used for the gate dielectric layer. Under large applied strains the electrical properties showed little variation due to the strain isolation effects of the bridges. For example, the inverter threshold voltage changed by less than ≈0.5 V for strains of ≈90% in *x* and *y* directions, as shown in the right frame of Figure 4b. The pre-strain value was ≈30%. To explore fatigue, we cycled the strain from 0% to ≈90% in the *x* direction 2000 times (Figure 4b). The inverters showed little change in properties (gain and threshold voltage, V_M) throughout these tests. Some slight variations were observed, likely due to limits in repeatability in probing devices on soft PDMS substrates. This non-coplanar serpentine bridge strategy can be applied not only to inverters, but also to more complex circuits. Figure 4d shows, as an example, a differential amplifier with circuit layouts and properties reported elsewhere.[8,11] The pre-strain value of amplifier was ≈20%. We divided the device into four sections, each of which forms an island, and connected them by non-coplanar serpentine bridges. Figure 4d shows magnified images of stretching in the *x* and *y* directions. Electrical measurements verify that the amplifiers work well under these deformations (see bottom-right frame of Figure 4d). The gains for 0% and 50% *x* stretching and 50% *y* stretching were 1.19, 1.17, and 1.16 (design value 1.2), respectively. Similar strategies should be applicable also to more complex systems.

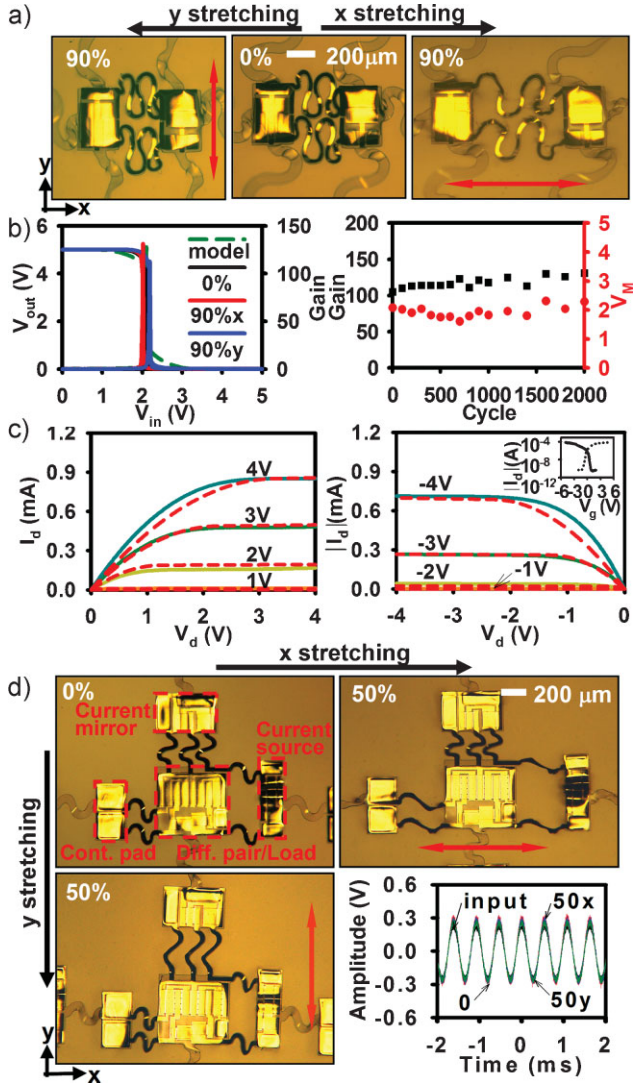

Figure 4. a) Optical images of a CMOS inverter with non-coplanar serpentine interconnects before and after applying 90% external strain in the *x* (right) and *y* (left) direction and b) corresponding voltage transfer curves (left) and cycling test results (right). c) Current–voltage response and PSPICE simulation result for NMOS (left) and PMOS (right) transistors; the inset shows the transfer curve on a semilog scale. d) Optical images and electrical characteristics of a differential amplifier with non-coplanar serpentine interconnects.

In practice, and especially for non-coplanar device designs, electronic circuits require top surface encapsulation layers to provide mechanical and environmental protection. An ideal material for this purpose is an elastomer with properties not too dissimilar from the substrate. For optimized mechanical response, this layer should provide minimal restriction of the free deformation of the non-coplanar serpentine bridges. The extent of restriction is controlled, in large part, by the modulus of the encapsulant. To provide insights into the materials and mechanics aspects, and to allow analytical calculation, we studied the behavior of straight bridge structures. After fabricating corresponding non-coplanar circuits, we encapsulated the system by casting and curing PDMS with different moduli (1.8 and 0.1 MPa) on top (Figure 5a), formed by mixing the prepolymer and curing agent (catalyst) at ratios of 10:1 and 45:1, respectively.[12] To examine the stretchability, we applied tensile strains up to the fracture point observable by optical microscope (Figure 5a). With a pre-strain of ≈60%, the inverter with no encapsulation can be stretched up to ≈59% without fracture. By contrast, for similar inverters encapsulated using PDMS with moduli of 0.1 and 1.8 MPa, the maximum stretchability decreased to 55% and 49%, respectively (Figure 5b). The error range is ≈2%. Combined with the amplitude change in Figure 5c, the differences between each encapsulation are apparent.

To understand these changes, we developed an analytical model and performed numerical FEM simulation. Consider first a straight bridge of length $2L$ that buckles upon release of the pre-strain in the PDMS. The buckle amplitude A_0 is related to the pre-strain ε_{pre} by[13,14]

$$A_0 = \frac{4L}{\pi}\sqrt{\frac{\varepsilon_{pre}}{1+\varepsilon_{pre}}} \quad (1)$$

After encapsulation, the energy of the system subject to the applied strain $\varepsilon_{applied}$ consists of four parts: i) bending energy in the bridge[14]

$$U_{bending} = \frac{\pi^4 (EI)_{bridge} A^2}{8L^3} \quad (2)$$

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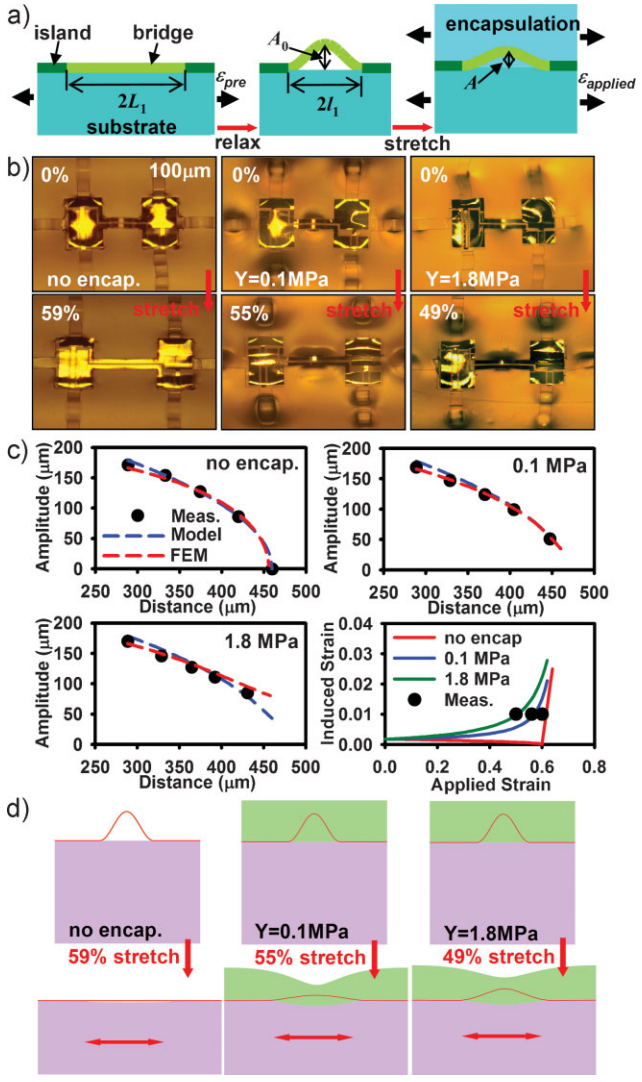

Figure 5. a) Schematic illustration of stretching test procedures for an encapsulated, straight bridge non-coplanar interconnect, b) optical microscopy images of the structure for the cases of zero strain (top) and maximum stretching before visible cracking (bottom) for no encapsulation (left), soft encapsulation (0.1 MPa, center) and hard encapsulation (1.8 MPa, right), c) height of the bridge as a function of distance between the two islands determined by experiment, analytical modeling, and FEM simulation; right bottom graph shows maximum strain before cracking estimated by theoretical modeling, d) deformation geometries at maximum stretching before cracking, simulated by FEM.

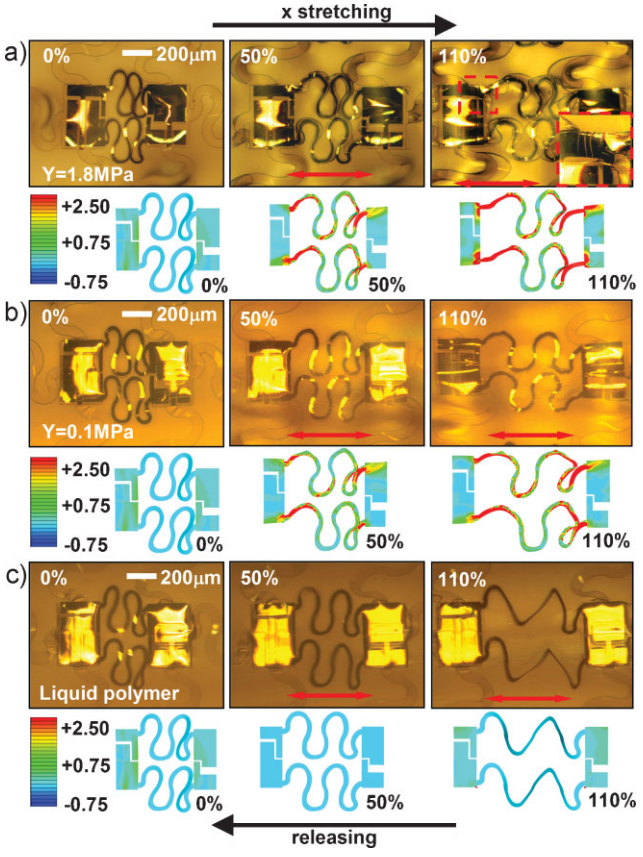

Figure 6. Optical microscopy images and strain distributions determined by FEM simulation for zero strain (left), ≈50% strain (center), and ≈110% strain (right), a) hard PDMS (modulus ≈1.8 MPa) encapsulation, b) soft PDMS (modulus ≈0.1MPa) encapsulation, and c) uncured PDMS prepolymer (viscous liquid) encapsulation covered by a thin, solid layer of PDMS.

where $(EI)_{\text{bridge}}$ is the bending stiffness of the bridge and A is the new amplitude under stretch; ii) membrane energy in the bridge[14]

$$U_{\text{membrane}} = (Eh)_{\text{bridge}} L \left(\frac{\varepsilon_{\text{applied}} - \varepsilon_{\text{pre}}}{1+\varepsilon_{\text{pre}}} + \frac{\pi^2 A^2}{16 L^2} \right)^2 \quad (3)$$

where $(Eh)_{\text{bridge}}$ is the tensile stiffness of the bridge; iii) elastic energy in the substrate $U_{\text{substrate}}$, which is proportional to the Young's modulus $E_{\text{substrate}}$ of the substrate, and is obtained from the linear elastic solution of a half space subject to normal surface displacement that is either sinusoidal (over the buckled bridge) or zero (over the island); and iv) elastic energy in the encapsulation $U_{\text{encapsulation}}$, which is proportional to the Young's modulus $E_{\text{encapsulation}}$ of the encapsulating materials. A is then obtained analytically by minimizing the total energy, which results in the following cubic equation for A that can be solved analytically:

$$\left(\frac{A}{L}\right)^3 + 16\left[\frac{1}{\pi^2}\frac{\varepsilon_{\text{appl}} - \varepsilon_{\text{pre}}}{1+\varepsilon_{\text{pre}}} + \frac{(EI)_{\text{bridge}}}{(Eh)_{\text{bridge}} L^2} + \frac{(E_{\text{substrate}} + E_{\text{encapsulation}})L}{2\pi^3 (Eh)_{\text{bridge}}}\right]\frac{A}{L} - \frac{32(E_{\text{substrate}} + E_{\text{encapsulation}})L}{\pi^4 (Eh)_{\text{bridge}}}\sqrt{\frac{\varepsilon_{\text{pre}}}{1+\varepsilon_{\text{pre}}}} = 0 \quad (4)$$

The strain in the bridge is given by

$$\varepsilon = \frac{\pi^2 A}{2L^2} y \quad (5)$$

where y is the distance to the neutral axis. Once the strain in the metal or silicon layer in the bridge reaches the fracture strain (1%), the corresponding applied strain gives the maximum stretchability.

To validate these models, we measured the amplitudes of the non-coplanar bridges during stretching for each case and compared to modeling and FEM values. In particular, the amplitude of a pop-up bridge was determined from the distance between the focal position on the top of the bridge to the surface of a neighboring island. The results exhibit good agreement with the theory, as shown in the top frames and bottom left frame of Figure 5c. The stretchability decreases as we use the high modulus encapsulation, consistent with experiments (right bottom frame of Figure 5c) and FEM simulation. Figure 5d shows FEM simulation images for no stretching and maximum stretching of each encapsulation case.

On the basis of insight from the simple cases of Figure 5, we applied PDMS encapsulation to CMOS inverters with non-coplanar serpentine bridges where the pre-strain is ≈30% to examine responses for PDMS with moduli of 1.8 and 0.1 MPa, and also for the case of uncured liquid PDMS. For the 1.8 MPa case, large applied strains (≈110%, right frame of Figure 6a) cause cracks while small strains (≈50%, center frame of Figure 6a) do not. Although 0.1 MPa PDMS avoids visible cracks at ≈110% strain, the images suggest significant strains, as also indicated by FEM simulation (bottom frames of Figure 6b), with significant wrinkling in the device islands. For further improvement, an uncured liquid prepolymer to PDMS without curing agent can be injected between the circuit level and an additional thin, top solid encapsulation layer of PDMS. As might be expected, the liquid PDMS has negligible effects on the essential mechanics, even after ≈110% external strain (Figure 6c). These three cases are supported by the theoretical analysis through FEM simulation.

3. Conclusions

Systematic studies of key effects of materials and design layouts on the mechanical properties of stretchable silicon integrated circuits reveal basic strategies for engineering these systems. Using simple strategies, circuits with excellent electrical performance and reversible, elastic mechanical responses to applied strains in the range of 100% are possible. In more sophisticated approaches of the future, automated design tools, conceptually similar to those in current use for design of electrical properties in circuits, might enable optimized mechanical properties and materials choices for desired applications. Such efforts appear important to the development of a technology foundation for stretchable electronics.

4. Experimental Section

The first step in fabricating stretchable silicon CMOS circuits is high-temperature diffusion for source-, drain-, and well-doping. In this paper, n-type SOI wafer (SOITEC, France) with 260-nm top silicon and 1-μm buried oxide provided the source of silicon nanoribbons/membranes. Since the mother wafer is n-type, the p-type well is formed first. For p-well, ≈550–600 °C diffusion of boron from a spin-on-dopant (B153, Filmtronics, USA) was performed. Next, successive high-temperature source- and drain-doping for p-type MOS (≈1000–1050 °C) and n-type MOS (≈950–1000 °C) was accomplished with boron (B153, Filmtronics, USA) and phosphorous (P509, Filmtronics, USA) spin-on-dopants, respectively. After high-temperature doping, doped nanoribbons/membranes were transfer-printed onto a carrier wafer coated with layers of PMMA (≈100 nm) and PI (≈1.2 μm). Electrical isolation of each transistor by reactive ion etching (RIE) followed by deposition of gate dielectrics using PECVD SiO_2 (≈40 nm) and metal electrodes (Cr/Au, ≈5 nm/≈1500 nm) using electron-beam evaporation formed the CMOS circuits. Coating a thin layer of PI (1.2 μm) as a passivation layer and forming a segmented, mesh structure by RIE completed the device fabrication. Dissolving the underlying PMMA layer released the ultrathin circuits. Lifting them to a pre-strained PDMS exposed their back surfaces for selective deposition of SiO_2 onto the active device regions. Transferring to a pre-strained substrate of PDMS completed the process. Electrical measurements were carried out using a probe station (Agilent, 4155C). Mechanical tests, including fatigue cycling, were performed with custom-made bending and stretching stages. For the substrates, the stamps, and the encapsulation layers, commercial PDMS kits (Sylgard 184, Dow Corning, USA) were used. After mixing the PDMS prepolymer and curing agent (catalyst) with an appropriate ratio, the samples were degassed for 1 h to remove bubbles generated during mixing. Curing was performed in an oven at 70 °C for 2 h.

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