Transfer of graphene layers grown on SiC wafers to other substrates and their integration into field effect transistors

Sakulsuk Unarunotai,[1,2] Yuya Murata,[2] Cesar E. Chialvo,[2,3] Hoon-sik Kim,[2,4] Scott MacLaren,[2] Nadya Mason,[2,3] Ivan Petrov,[2,4] and John A. Rogers[1,2,4,5,a)]
[1]*Department of Chemistry, University of Illinois at Urbana-Champaign, 505 South Mathews Avenue, Urbana, Illinois 61801, USA*
[2]*Frederick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, 104 South Goodwin Avenue, Urbana, Illinois 61801, USA*
[3]*Department of Physics, University of Illinois at Urbana-Champaign, 1110 West Green Street, Urbana, Illinois 61801, USA*
[4]*Department of Materials Science and Engineering, University of Illinois at Urbana-Champaign, 1304 West Green Street, Urbana, Illinois 61801, USA*
[5]*Department of Mechanical Science and Engineering, Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, USA*

(Received 3 August 2009; accepted 20 October 2009; published online 16 November 2009)

This letter presents a simple method for transferring epitaxial sheets of graphene on silicon carbide to other substrates. The graphene was grown on the (0001) face of 6H-SiC by thermal annealing at 1550 °C in a hydrogen atmosphere. Transfer was accomplished using a peeling process with a bilayer film of gold/polyimide, to yield graphene with square millimeters of coverage on the target substrate. Raman spectroscopy provided evidence that the transferred material is single layer. Back gated field-effect transistors fabricated on oxidized silicon substrates with Cr/Au as source-drain electrodes exhibited ambipolar characteristics with hole mobilities of ~100 cm^2/V-s, and negligible influence of resistance at the contacts. © *2009 American Institute of Physics*. [doi:10.1063/1.3263942]

Graphene[1] is a promising material for high speed electronics due to its exceptionally high carrier mobilities,[2] and ballistic transport characteristics.[3] Some of the earliest works involved graphene derived by mechanical exfoliation from bulk pieces of highly ordered pyrolytic graphite (HOPG).[1,2] Although pristine quality films can be achieved this way, the samples are small, typically below 100 μm^2, the yields are low and the ability to control the positions, shapes, and orientations are limited. Other approaches for mass production of graphene are under active investigation; these include epitaxial growth on SiC substrates,[4,5] chemical vapor deposition growth on metal surfaces,[6,7] and chemical reduction of graphene oxide.[8,9] The first method relies on Si sublimation and graphization of C atoms on the SiC by annealing at high temperature under ultrahigh vacuum (UHV). This approach is promising but its current implementation requires the use of SiC as the device substrate. This feature frustrates integration with silicon technologies, and requires the use of top gate transistor device geometries. Here, we report procedures for transferring graphene films epitaxially grown on SiC to other substrates. Fabrication of field effect transistors using graphene transferred onto Si wafers with layers of SiO_2 on their surfaces reveals the properties of the materials and suggests the possibility for integration with silicon electronics.

For growth, we used 5×25 mm^2 rectangular pieces of (0001) face 6H-SiC cut from a wafer (II-VI, Inc.) and coated with 200 nm Ta on their back sides (electron beam evaporation; Temescal BJD1800). Such samples were installed in a UHV chamber with a base pressure 10^{-10} Torr and heated to 1550 °C by passing current through the Ta layer for 6 h in a hydrogen atmosphere of 2×10^{-7} Torr while the temperature was monitored by a radiation thermometer (CHINO IR-CAQ). Inspection of the resulting samples by low energy electron diffraction (LEED) revealed a characteristic pattern of multilayer graphene.[10] XPS and Raman spectroscopy confirmed this result.[10] These observations are consistent with previous reports using related growth techniques.

Transfer of graphene from the SiC growth wafer to another substrate followed procedures similar to those recently reported for carbon nanotubes.[11] See Fig. 1. In the first step, the graphene/SiC sample was coated with a layer of Au (~100 nm; electron beam evaporation; Temescal BJD1800) and then with a layer of polyimide (~1.4 μm; poly(pyromellitic dianhydride-co-4,4′-oxydianiline) amic acid solution (Sigma-Aldrich, Inc.); 3000 rpm for 30 s, baked at 110 °C for 2 min to remove the solvent and partially cure the polymer). Peeling this bilayer film away from the SiC wafers lifted some of the graphene from the SiC wafer. Delivering the film to a target substrate (silicon wafer with thermal oxide, for the work reported here) and then removing the PI and the Au with oxygen plasma reactive ion etching (Plas-

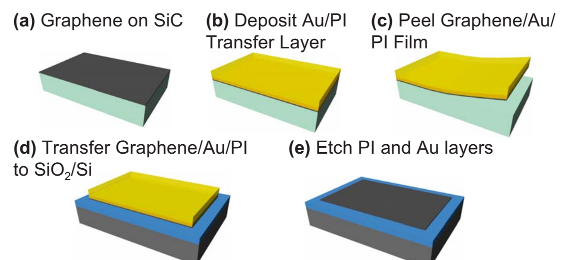

FIG. 1. (Color online) Schematic illustration of the steps for transferring graphene grown on a SiC wafer to another substrate (SiO_2/Si in this case).

[a)]Author to whom correspondence should be addressed. Electronic mail: jrogers@uiuc.edu.

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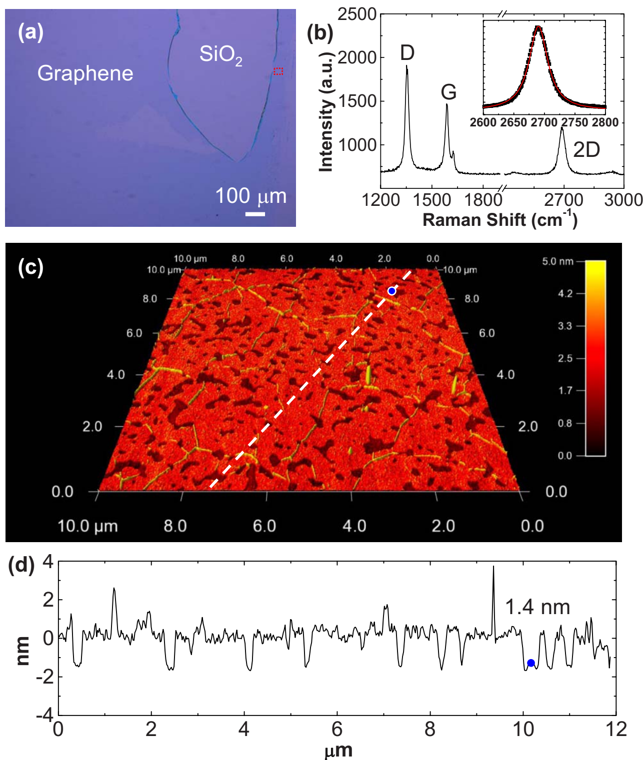

FIG. 2. (Color online) Properties of graphene transferred from SiC to SiO_2(300 nm)/Si. (a) Optical image of a piece of graphene covering square millimeters. (b) Raman spectrum showing the expected D, G, and 2D peaks. Inset shows 2D peak data, and a fit to a single Lorentzian form. (c) AFM image of a representative region, corresponding to the dotted square area of (a). This image reveals tears, holes, and wrinkles in the film, many of which are at least partly associated with the transfer process. (d) AFM section line scan across the film, indicating a uniform thickness of ~1.4 nm, for the region in proximity to the circled area.

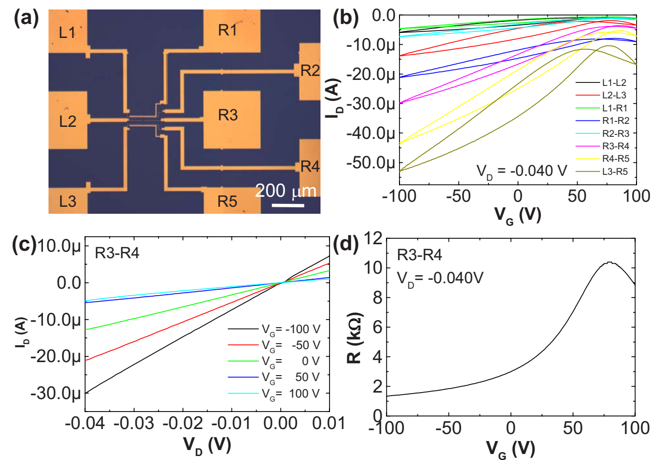

FIG. 3. (Color online) Field effect transistors that use transferred graphene. (a) Optical image of a collection of devices, with notation identifying the metal contacts. (b) Transfer characteristics (i.e., drain current, I_D, as a function of gate voltage, V_G) of devices corresponding to different metal contact pairs, at a drain voltage (V_D) of −0.04 V. Forward and reverse sweeps reveal some small level of gate voltage induced hysteresis. (c) I_D-V_D characteristics at various V_G for the graphene device that uses R3 and R4 as source and drain electrodes. (d) Plot of device resistance (R) as a function of V_G for the device in (c) and V_D=−0.04 V.

maTherm; 100 mTorr, O_2 20 sccm, 100 W, and 30 min) and wet chemical etching (Transene, Inc.), respectively, completed the process. We examined the transferred graphene layers by optical microscopy, Raman spectroscopy and atomic force microscopy (AFM). Figure 2(a) shows a low magnification optical image of a transferred layer of graphene on a SiO_2 (300 nm)/Si substrate. Here, well known contrast mechanisms enable direct visualization of the graphene,[12] to reveal large areas (i.e., square millimeters) of transferred material, with good uniformity. These areas exceed significantly those of previous reports, either of transferred material from a bulk piece of HOPG[1–3] or from SiC.[13] Raman spectroscopy (488 nm excitation) revealed expected peaks at the D, G, and 2D bands, 1355, 1586, and 2689 cm^{-1}, respectively [Fig. 2(b)]. The positions of G and 2D peaks are redshifted, compared with those observed on the SiC substrate immediately after growth, to values closer to those of exfoliated graphene. This result is consistent with relaxation of compressive strains that can exist in graphene on SiC. The shape of the 2D peak is symmetric, narrow, and well described by a single Lorentzian curve, suggesting that the film is single layer graphene.[13,14] The relatively large D peak implies a substantial content of defects and disorder, associated at least in part with edges in the transferred material.[15] The AFM image in Fig. 2(c) indicates that the film contains holes with sizes, densities, and shapes that vary with position. In many cases, the shapes and orientations correlate well with steps observed on the SiC substrate. Figure 2(d) shows a section line scan from the AFM image [Fig. 2(c)]. These data indicate that the film thickness is uniform, although the value exceeds that expected for single layer graphene, possibly due to residue from the transfer process. Because we did not observe a substantial density of holes in the graphene on SiC before transfer, we speculate that these and related imperfections are, at least partly, introduced in the transfer process. In addition to holes, the AFM scan of Fig. 2(c) shows wrinkles in certain regions, likely also generated during the transfer process but also known to be present in graphene grown on SiC.[16]

Back gated field effect transistor devices were fabricated on graphene transferred to a 300 nm thick, thermally grown layer of SiO_2 on a Si substrate with source and drain electrodes (Cr/Au, 5 nm/50 nm) patterned by electron beam lithography, electron beam evaporation, and lift-off, as depicted in the optical image of Fig. 3(a). The source/drain electrodes are labeled as L1, L2, L3 and R1, R2, R3, R4, R5, which correspond to structures visible on the left and right sides of the image, respectively. The channel widths (W) and lengths (L) vary from 10 to 250 μm and from 10 to 200 μm, respectively, although in several cases the coverage of the graphene itself defines the effective width. Transfer curves and I_D-V_D characteristics were measured at room temperature using a semiconductor parameter analyzer (Agilent Technologies). Figure 3(b) shows plots of the drain current (I_D) as a function of the applied gate voltage (V_G) for various devices. (We note that not all of these devices were electrically isolated from one another by patterned etching of the graphene, but many were effectively isolated due to the geometry of coverage in the transferred material). These transfer curves indicate ambipolar modulation characteristics consistent with the expected semimetallic character of graphene. The Dirac points occur at positive gate voltages, likely due to atmospheric doping.[17] Some mild level of hysteresis was typically observed, as shown in Fig. 3(b). Qualitatively, we found that the magnitudes of I_D generally scale in the expected manner with W/L, with discrepancies that

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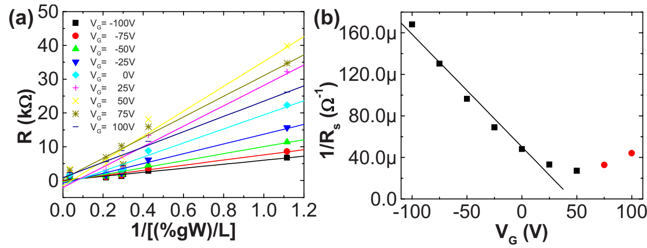

FIG. 4. (Color online) Scaling analysis of the behavior of graphene field effect transistors. (a) Plot of device resistance as a function of scaled channel geometry. The small y-intercept is consistent with a contact resistance that is small (<1 kΩ) and, to within uncertainties, independent of V_G. (b) Plot of sheet conductance, evaluated from the slopes of linear fits to the data of (a), as a function of V_G. Linear fits determine the Dirac voltage (x intercept) and the apparent mobility (slope).

can be accounted for by different densities of holes in the graphene.

To analyze these results quantitatively, neglecting fringing fields, possible anisotropies in the transport and effects of neighboring electrodes, we extracted the field effect mobility from a selected device that incorporated a region of graphene with a relatively low level of holes (3% of total area, i.e., device with electrodes R3 and R4). The I_D-V_D characteristics and the dependence of R, the total resistance of the device (i.e., V_D/I_D at $V_D=-0.04$ V) on V_G appear in Figs. 3(c) and 3(d), respectively. The Dirac point is ~80 V. The slope of the transfer curve near this point, dI_D/dV_G, is $\sim -5\times 10^{-8}$ A/V, corresponding to a hole mobility of ~ 100 cm^2/V-s calculated using a standard metal-oxide-semiconductor field-effect transistor model with a parallel plate gate dielectric capacitance of 1.15×10^{-8} F/cm^2. This mobility is certainly influenced by the presence of holes and related defects, none of which is accounted for in this simple analysis. Other reports of transistors based on graphene derived from SiC involve top gate geometries, all built on the SiC wafer. The mobilities in those cases range from ~500 to 5000 cm^2/V-s with Dirac points near zero.[18–20] Additionally, the on/off ratios for each device can be directly derived from each transfer curve shown in Fig. 3(b). In particular, the device with electrodes R3 and R4 has a value of ~8.

To examine the role of contacts in devices such as the one of Fig. 3, we performed a scaling analysis, shown in Fig. 4(a). This analysis used all measured devices, with a simple procedure to account for the different densities of holes. In particular, we used a scaled resistance defined by $R = R_S[1/(\%gW/L)] + 2R_C$ where R is total resistance of device, R_S is sheet resistance of the conducting layer, R_C is the contact resistance and %g, the percentage of graphene coverage, as determined from the SEM image analysis. The contact resistance, extracted from the y intercept of the plot in Fig. 4(a), is below 1 kΩ indicating a negligible role of contacts in the device operation for the range of channel lengths examined here. The inverse of the slope defines the sheet conductance $(1/R_S)$ at different gate voltages. Figure 4(b) shows the scaling of this quantity with the L, revealing a hole mobility of ~90 cm^2/V-s, roughly consistent with the device of Fig. 3. Although the large positive value of the Dirac point prevents accurate determination of the electron mobility, its magnitude appears comparable to that for holes.

In summary, graphene films epitaxially grown on SiC substrate were transferred to oxidized Si wafers for the fabrication of bottom gate field effect transistors. AFM, Raman, LEED, and electrical measurements revealed the essential features of the materials. Key attractive aspects of these procedures are the scalability to large areas and possibly area selective transfer, the apparent ability to remove single layers of graphene from multilayer films, and the applicability to wide ranging classes of substrates, due to room temperature operation. Directions for further study include reducing the level of defects in the films, achieving improved transport properties and developing procedures for SiC substrate reuse.

The authors thank R. T. Haasch for technical supports on XPS. This work is supported by the U.S. Department of Energy, Division of Materials Sciences under Award No. DE-FG02-07ER46471, through the Materials Research Laboratory and Center for Microanalysis of Materials (Grant No. DE-FG02-07ER46453) at the University of Illinois at Urbana-Champaign. S.U. was supported, in part, by the Anandamahidol Foundation.

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