Vol. 21 • No. 36 • September 25 • 2009

D10488

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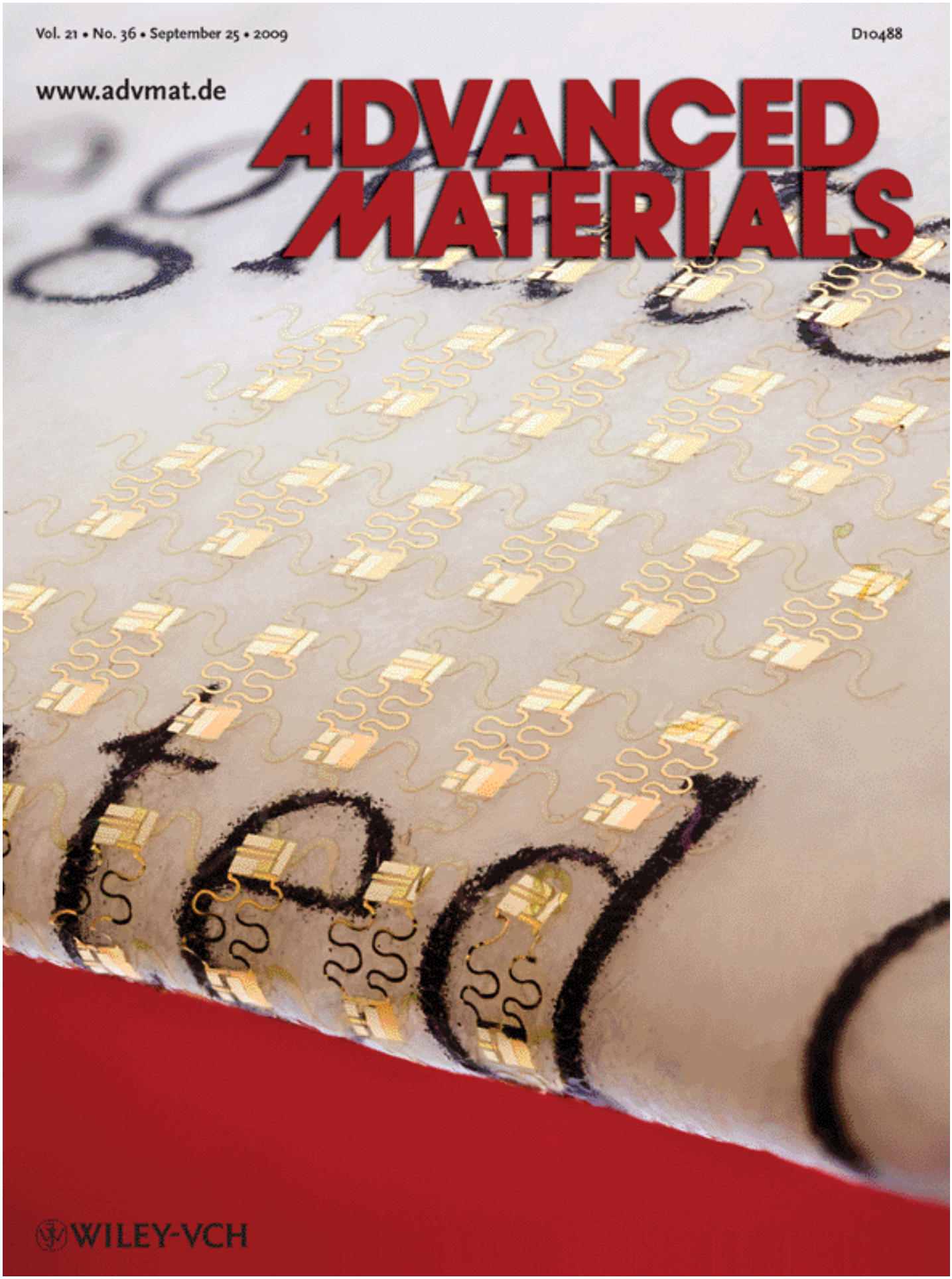

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Ultrathin Silicon Circuits With Strain-Isolation Layers and Mesh Layouts for High-Performance Electronics on Fabric, Vinyl, Leather, and Paper

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Electronic systems built on plastic sheets, metal foils, rubber slabs and other unusual substrates have great potential for use in conformal image sensors, flexible displays, biomedical devices and other emerging applications.[1–8] Research in this area includes the development of organic conductors and semiconductors materials[4–8] whose excellent mechanical flexibility and low temperature processability are attractive for these systems. The characteristics of devices that can be achieved with such materials enable electronic paper displays and other important products, but not readily those that require, for example, radio frequency operation.[1,9] Newer research aims to avoid this limitation by exploiting thin films of inorganic materials or assemblies of carbon nanotubes, graphene platelets, nanoparticles, nanowires, nanoribbons or nanomembranes for the semiconductor.[9–14] With certain of these materials, it is possible to build high performance circuits that are not only bendable but are also, in some cases, reversibly stretchable, with elastic responses to compressive and tensile strains of 100% or more.[15,16] One approach to stretchability relies on semiconductor membranes or ribbons in buckled or wavy shapes that accommodate applied strains with a physics similar to an accordion bellows.[17,18] High-performance transistors and their use in logic gates, ring oscillators and differential amplifiers suggest the possibility for realistic applications;[19] hemispherical arrays of photodiodes for electronic eye cameras provide an example of a system level demonstration.[20] Here, we extend these concepts and implement them with a new technique that involves thin, low modulus elastomers to isolate the active circuit materials from applied strains. The result is a path to high performance silicon complementary metal oxide semiconductor (CMOS) circuits[21] (or other device technologies) capable of integration on diverse classes of substrates that might be interesting for electronics, ranging from paper to fabric, leather and vinyl, as examples presented here. Data indicate that the electrical performance of representative CMOS components and logic gates on these substrates can approach those of similar devices on silicon wafers, without degradation upon bending, folding, draping and other modes of deformation.[15,19,21] Experimental and theoretical studies described in the following support these outcomes and reveal essential features of the materials and mechanics.

The fabrication begins with the formation of ultrathin CMOS circuits in planar, serpentine mesh geometries using procedures closely related to those reported recently.[15] Releasing the circuits

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DOI: 10.1002/adma.200900405

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from the carrier wafer on which they are formed (Fig. 1A) by dissolving an underlying layer of poly(methylmethacrylate) (PMMA, MicroChem, USA), lifting them onto the surface of a polydimethylsiloxane (PDMS, Dow Corning, USA) stamp, depositing a bilayer of Cr/SiO_2 (3 nm/30 nm) selectively onto the backsides of regions of the circuit that correspond to the active device islands by evaporation through an aligned shadow mask and, finally, transfer printing onto a substrate coated with a thin layer of cured PDMS completes the process (Fig. 1B). Details appear in the Experimental Section. Measurements of individual transistors formed in this manner (Fig. 1C) indicate electron and hole mobilities of ≈530 and ≈150 $cm^2\ V^{-1}\ s^{-1}$ for n-type MOS (nMOS) and p-type MOS (pMOS) transistors, respectively, and on/off ratios $>10^5$ in both cases. The channel lengths and widths for all devices reported here were 13 μm and 100 μm for nMOS and 13 μm and 300 μm for pMOS. Connecting nMOS and pMOS devices via serpentine interconnects yields inverters with gains as high as 150, consistent with PSPICE simulations (Fig. 1C). Full integrated circuits can be achieved with similar layouts.

The thin layer of PDMS described above serves two critically important roles. First, and most simply, it provides an adhesive that bonds certain strategic regions of the circuits to a wide range of surfaces including fabric, vinyl, leather and paper, as reported here, in either flat or curved, balloon-like shapes. In particular, –OH groups associated with the SiO_2 on the backsides of the islands covalently react with the PDMS to form Si–O–Si linkages. Such –OH groups exist naturally on the SiO_2[22] and PDMS.[23] Their density can be increased by exposure to ozone, oxygen plasma or other related procedures.[10,23] This bonding approach yields strong interfaces; we do not observe adhesive failure modes in our devices. The absence of SiO_2 on the serpentine interconnects leads to only weak Van der Waals (VdW) interactions in these regions.[10] As a result, upon stretching, compressing or extreme bending, the interconnects lift out of contact with the PDMS to adopt non-coplanar geometries, as shown in the scanning electron microscopy (SEM) image (inset of right frame of Fig. 1B). This motion accommodates large tensile or compressive strains in a manner that avoids fracture of the interconnects or significant strains in the islands. Similar circuit layouts bonded to the PDMS in all regions show much reduced (2–3 times lower) ability to withstand applied strain. The approach of Figure 1 provides large stretchability while avoiding steps that use prestrain to create the non-coplanar layouts.[15]

The second important role of the PDMS layer is illuminated by examining the mechanics. Figure 1D shows optical microscopy images and finite element modeling for the response of a system similar to the one shown in Figure 1 to uniaxial tensile strain. At maximum extension explored here, the modeling indicates peak strains in the metal layer of the interconnects and in the silicon of the active islands are 0.20% and 0.46%, respectively, i.e., >200 times smaller than the applied strain. This behavior provides utility for stretching/compressing on length scales larger than a pair of islands; it cannot accommodate strain localized on individual islands generated, for example, by a sharp folding deformation with a paper substrate. The low modulus PDMS adhesive layer solves this problem, by providing strain isolation. To gain a qualitative understanding, consider limiting cases where the modulus of this layer is equal to the underlying substrate and when it is arbitrarily small. In the first situation,

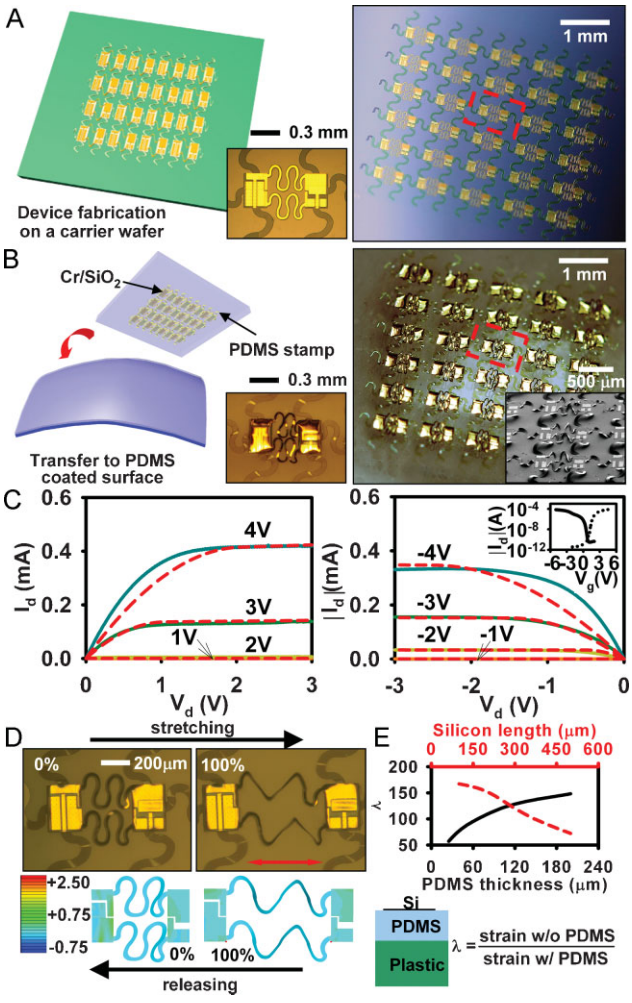

Figure 1. A) Schematic illustration of an ultrathin silicon circuit fabricated in a serpentine mesh geometry on a handle wafer (left) and an optical image (right). The inset at the center shows an optical microscopy image of a CMOS inverter, corresponding to the red dotted box in the right frame. B) Schematic illustration of the process for transfer printing the circuit after patterned depositon of Cr/SiO_2 (left) and an optical image after transfer (right). The inset at the center shows an optical microscopy image of a transferred CMOS inverter, corresponding to the red dotted box on the right frame. The inset of the right frame shows a scanning electron microscopy image of the system in a bent configuration. C) Current (I_d; drain current), voltage (V_d; drain voltage) measurements on representative nMOS (left) and pMOS (right) transistors collected from a circuit similar to those shown in the other frames. The solid and dashed lines correspond to measurement and PSPICE simulation. The labels on the curves correspond to gate voltages (V_g). The inset in the right frame shows transfer curves plotted on a semilog scale for nMOS (dotted) and pMOS (solid) devices. D) Optical microscopy images (upper frames) of a CMOS inverter circuit under various levels of tensile strain (upper left) and finite element modeling of the corresponding mechanics (lower frames). The colors indicate peak strains (in percent) in the metal interconnect level of the circuit. E) Computed ratio of the surface strain in the silicon of the system schematically illustrated in the lower left as a function of thickness of this layer (black solid line) and length of the silicon (red dotted line; PDMS thickness is 100 μm for this case). The PDMS provides strain isolation for the silicon, with increasing effectiveness as the silicon length decreases and the PDMS thickness increases.

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bend induced strains in surface mounted circuits depend, approximately, on the ratio of the total thickness of the system divided by the radius of curvature of the bend. For a sharp folding deformation, this radius can be very small. As a result, the strain in an island located at the position of such a fold can exceed the fracture point of the electronic materials for all but the thinnest systems (or those with sandwich type neutral mechanical plane layouts).[19] In the second case, the substrate is weakly mechanically coupled to the circuit components, such that bending the substrate leads to only relatively small bending of the islands. As a result of this mechanics, bend induced strains in the electronic materials are much lower than would otherwise be expected. It is in this sense, the low modulus layer provides strain isolation. Similar arguments can be used to understand the dependence of the strain on the thickness of this layer. In an actual system, the moduli and thicknesses of all layers are important variables. The key dependencies can be illustrated in a simplified system that consists of a plastic substrate, a PDMS adhesive layer and a thin silicon layer. The elastic modulus of PDMS is several orders of magnitude smaller than those of plastics and silicon. Salient findings of analytical calculations that include all of the mechanics in a rigorous way appear in Figure 1E. This plot shows the ratio of the surface strain for a two dimensional system composed of an island of silicon (300 nm thick) on a layer of PDMS on a sheet of plastic (100 μm thick), as a function of the width of the silicon and the thickness of the PDMS. The results indicate that the isolation efficiency increases with increasing PDMS thickness and decreasing silicon width, as might be expected intuitively. For parameters comparable to those of the circuits studied here, the isolation provides ≈100× reduction in strain, thereby enabling extreme degrees of bending even without ultrathin layouts or neutral mechanical plane designs. Details of the modeling will be reported separately. The use of this strategy with serpentine meshes simultaneously achieves high bendability and stretchability.

Figure 2A shows the response of the serpentines to spatially non-uniform strains generated by bending a circuit on a thin sheet of PDMS. Variable levels of deformation can be seen at the folded corner (right top SEM image) and at the sides (right bottom SEM image). Bonding the circuit to a thin, low modulus strain isolation and adhesion layer as described above provides a strategy for integration with various other kinds of substrates. The top and left bottom frame of Figure 2B show images and schematic diagrams of CMOS inverters on fabric. The inset shows a magnified view. Even after bending to radii of ≈5 mm, the inverter functions well, as shown in the right bottom frame of Figure 2B. Although this kind electronic textile offers much better performance than alternatives based on active threads or fibers,[24–27] it does not offer the potentially attractive weaving mode of manufacturing. In this sense, the systems presented here might complement such fiber based approaches.

A key feature of the example of Figure 2B is that the PDMS adhesion layer penetrates into the fibers of the fabric to yield strong adhesion without chemical bonding, thereby providing a route to integration that does not depend critically on chemistry. The left frames of Figure 3 show SEM images of surfaces of vinyl (Fig. 3A), leather (Fig. 3B), paper (Fig. 3C) and fabric (Fig. 3D). The porosity and roughness increase from Figure 3A to D. The right frames of Figure 3 show fracture cross-sections of each

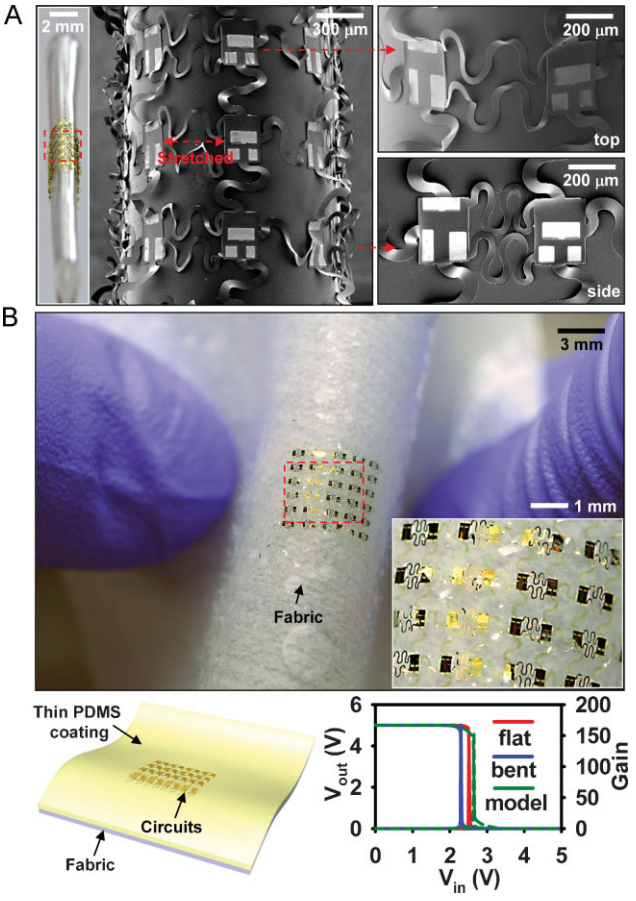

Figure 2. A) Optical image of a folded circuit (left) consisting of an array of CMOS inverters and scanning electron microscopy image (center). The images on the right provide views at the folded edge (right top) and side (right bottom). B) Optical image of a similar circuit integrated on a fabric substrate coated with a thin layer of PDMS (top) and magnified view (top right). The bottom left frame provides a schematic illustration. The bottom right shows transfer curves of a representative inverter in flat and bent states, and PSPICE simulation (model).

surface after coating with PDMS (the approximate thickness of PDMS is ≈200 μm, ≈100 μm, ≈80 μm, and ≈50 μm for vinyl, leather, paper and fabric, respectively), in a dip casting and thermal curing process. As the surface porosity increases, the degree of penetration of PDMS into the substrate increases, thereby improving the strength of adhesion. In the case of vinyl, the PDMS coating delaminates upon freeze fracture (Fig. 3A). In the case of fabric, the constituent fibers are completely embedded by the PDMS, leading to strong bonding as indicated by the fracture surface in Figure 3D. The intermediate cases of leather and paper exhibit strong adhesion.

As a demonstration of CMOS circuits on leather and vinyl, we integrated arrays of inverters at finger joints in gloves made of these materials, as shown in the Figure 4A and B. Moving the fingers causes the circuits to stretch and release, with no noticable change in the electronic properties. To examine fatigue, we cycled through such motion 1000 times (See Experimental Sec.), and measured the electrical properties at various stages of the test, as shown in Figure 4C. For this example, the inverter threshold

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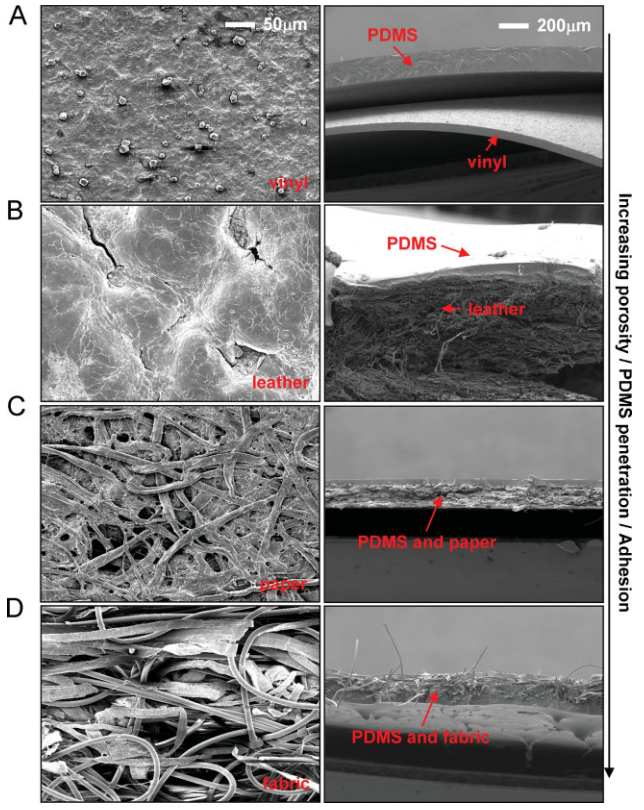

Figure 3. SEM images of the surfaces of various substrates before coating with PDMS (left) and corresponding tilted views of freeze fractured edges after PDMS coating (right) for A) vinyl, B) leather, C) paper, and D) fabric substrates.

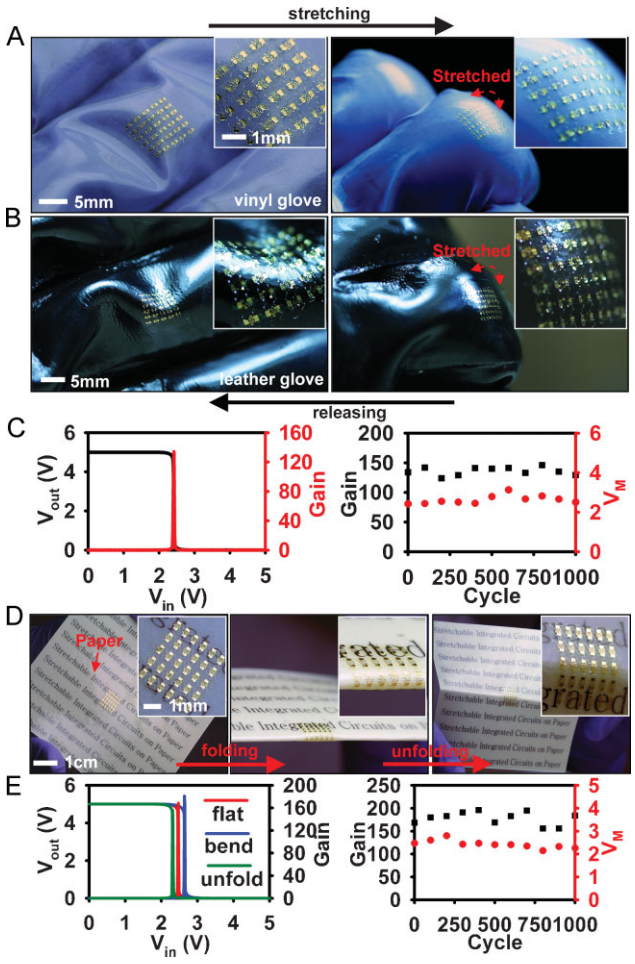

Figure 4. Optical images of CMOS circuits on finger joints of vinyl (A) and leather (B) gloves in released (left) and stretched (right) states. The insets provide magnified views. C) Voltage transfer curve (left) and cycling test results that show the gain and threshold voltage of the inverter (V_M) measured in the flat states after various numbers of bending cycles (right). D) Optical images of CMOS inverters on paper, in flat (left), folded (center) and unfolded (right) states. The insets provide magnified views. E) Voltage transfer curve (left) and cycling test results that show the gain and threshold voltage of the inverter (V_M) measured in the flat states after various numbers of folding/unfolding cycles (right).

voltage and gain change by less than ±0.4 V and ±5%, respectively. Similar circuits on paper are particularly interesting, not only for applications in smart cards and related but also for their capacity to add functionality to paper-based microfluidic diagnostic devices.[28] Figure 4D and the left frame of Figure 4E show CMOS inverters on paper and their properties, in a series of bending, folding and unfolding tests. Electrical measurements associated with 1000 cycles of these deformations (See Experimental Sec.) indicate stable, high performance operation (inverter threshold voltage change < ±0.4 V, gain change < ±10%.) and even good characteristics upon folding and extreme bending (right frame of Fig. 4B). This approach to electronics on paper provides an alternative to those that rely on direct thin film deposition of organic[29–32] or inorganic[33–35] electronic materials.

In summary, the combined use of circuits with non-coplanar serpentine mesh designs and thin, low modulus strain isolation layers allows integration of high performance silicon CMOS integrated circuits on diverse substrates. From a practical point of view, such devices, like any other class of electronics technology, require a top encapsulation layer to provide mechanical protection and an environmental barrier. Although these layers do not affect significantly the mechanics of non-copolanar interconnects at modest strains (<50%), they can have important influence at high strain (>50%). Encapsulants with low moduli provide the most freedom of motion and, therefore, the highest levels of stretchability. Low modulus (≈0.5 MPa) formulations of PDMS, for example, increase the range of stretchability from 60%, corresponding to the case of PDMS like that used for the adhesive/isolation layer (1–2 MPa), to 120%. Further optimization of the encapsulant materials and serpentine geometries have the potential to yield additional improvements.

Experimental

Fabrication of Ultrathin, Stretchable CMOS Circuits: The fabrication of CMOS circuits starts with the doping of single crystalline silicon nanoribbons (260nm) derived from n-type SOI wafers (SOITEC, France). P-well, pMOS and nMOS source/drain doping was accomplished by using

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a 300 nm layer of silicon dioxide (SiO_2) formed by plasma enhanced chemical vapor deposition (PECVD) as a diffusion mask and Boron (B153, Filmtronics, USA) and Phosphorous (P509, Filmtronics, USA) spin-on-dopants. Diffusion was carried out at 550–600 °C, 1000–1050 °C, and 950–1000 °C for pwell, p-type source/drain and n-type source/drain doping. The doped ribbons were released from the SOI wafer by etching the buried oxide, and then sequentially transfer printing onto a carrier wafer coated with thin layers of PMMA (≈100 nm) as a sacrificial layer and PI (≈1.2 μm) as an ultrathin substrate. Isolated nMOS and pMOS source/drain patterns were defined with photolithography and reactive ion etching (RIE). Patterned etching of PECVD SiO_2 (≈40 nm) provided the gate dielectric; metal electrodes (Cr/Au, ≈5 nm/≈1500 nm) deposited by electron beam evaporation and patterned by wet etching defined source, drain, gate and interconnects for the circuits. Spin coating PI (1.2 μm) on top of the resulting circuits formed a passivation layer and also located the neutral mechanical plane near the brittle electronic materials. Finally, oxygen RIE through a patterned mask defined the serpentine bridges.

Transfer Printing: Dissolving the PMMA layer with acetone released the circuits from the carrier wafer. Lifting the circuits onto a PDMS stamp exposed their backsides for deposition of a thin layer of Cr/SiO_2 (3 nm/30 nm) at the islands by electron beam evaporation through an aligned shadow mask. Transfer printing the circuit to a PDMS coated surface (paper, vinyl, leather or fabric) activated by exposure to UV/ozone led to –O–Si–O– bonding at the positions of the islands.

Cycling Test and Measurement: Cycling tests for gloves were performed through repetitive bending of joints after wearing gloves on which CMOS circuits were transferred. The electrical measurement was carried out using a probe station (Agilent, 4155C) after a series of cycling tests. The cycling for paper was similar. The paper was folded and unfolded repetitively and measured with the probe station.

Acknowledgements

We thank for various helps of T. Banks in processing by use of facilities at the Frederick Seitz Materials Research Laboratory. This material is based upon work supported by the National Science Foundation under grant ECCS-0824129, NSFC, and the U.S. Department of Energy, Division of Materials Sciences under Award No. DE-FG02-07ER46471, through the Materials Research Laboratory and Center for Microanalysis of Materials (DE-FG02-07ER46453) at the University of Illinois at Urbana-Champaign.

Received: February 5, 2009
Revised: March 20, 2009
Published online: July 6, 2009

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