LETTERS

Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates

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The ability to form integrated circuits on flexible sheets of plastic enables attributes (for example conformal and flexible formats and lightweight and shock resistant construction) in electronic devices that are difficult or impossible to achieve with technologies that use semiconductor wafers or glass plates as substrates[1]. Organic small-molecule and polymer-based materials represent the most widely explored types of semiconductors for such flexible circuitry[2]. Although these materials and those that use films or nanostructures of inorganics have promise for certain applications, existing demonstrations of them in circuits on plastic indicate modest performance characteristics that might restrict the application possibilities. Here we report implementations of a comparatively high-performance carbon-based semiconductor consisting of sub-monolayer, random networks of single-walled carbon nanotubes to yield small- to medium-scale integrated digital circuits, composed of up to nearly 100 transistors on plastic substrates. Transistors in these integrated circuits have excellent properties: mobilities as high as 80 $cm^2 V^{-1} s^{-1}$, subthreshold slopes as low as 140 m V dec^{-1}, operating voltages less than 5 V together with deterministic control over the threshold voltages, on/off ratios as high as 10^5, switching speeds in the kilohertz range even for coarse (~100-μm) device geometries, and good mechanical flexibility—all with levels of uniformity and reproducibility that enable high-yield fabrication of integrated circuits. Theoretical calculations, in contexts ranging from heterogeneous percolative transport through the networks to compact models for the transistors to circuit level simulations, provide quantitative and predictive understanding of these systems. Taken together, these results suggest that sub-monolayer films of single-walled carbon nanotubes are attractive materials for flexible integrated circuits, with many potential areas of application in consumer and other areas of electronics.

Efforts to develop polymer and small-molecule semiconductors for electronics have yielded several impressive demonstrations, including integrated circuits with more than 1000 transistors[3], flexible displays[3,4], sensor sheets[5] and other systems[6,7]. In all cases, however, the field-effect mobilities of the transistors are modest: typically ~1 $cm^2 V^{-1} s^{-1}$ for isolated devices[8,9] and <0.05 $cm^2 V^{-1} s^{-1}$ in integrated circuits[3–7]. Although these properties are sufficient for electrophoretic displays and certain other applications, improvements in the materials would expand the possibilities[1]. Separately, for any given application, increases in mobility relax the requirements on critical feature sizes in the circuits (for example transistor channel lengths) and tolerances on their multilevel registration, which can be exploited to reduce the cost of the plastic substrates and patterning systems to achieve roll-to-roll fabrication by dry printing[10] or ink-jet printing[11].

Recently developed carbon-based semiconducting nanomaterials, especially single-walled carbon nanotubes (SWNTs), might provide an opportunity to achieve extremely high intrinsic mobilities, high current-carrying capacities and exceptional mechanical/optical characteristics, in bendable formats on plastic substrates[12]. Although isolated SWNTs are not relevant to the applications contemplated here, recent work shows that sub-monolayer random networks[13–16] or aligned arrays[17,18] of SWNTs can serve as thin-film semiconductors which, in the best cases, inherit the exceptional properties of the tubes, for example device mobilities up to ~2,500 $cm^2 V^{-1} s^{-1}$, on-state currents above several milliamperes, and cut-off frequencies above 1 GHz for devices on plastic. The network geometry is of particular interest for flexible electronics because it can be easily achieved by printing SWNTs from solution suspensions[19]. The present work demonstrates implementations of SWNT networks in flexible integrated circuits on plastic that have attractive characteristics, together with corresponding theoretical models and simulation tools that capture all of the key aspects.

The system layouts (Fig. 1a) exploit architectures similar to those in established silicon integrated circuits. A thin (50-μm) sheet of polyimide serves as the substrate. Random networks of SWNTs grown by chemical vapour deposition and subsequently transfer printed onto the polyimide form the semiconductor layer[17]. Source and drain (S–D) electrodes of gold serve as low-resistance contacts to these networks, as determined by scaling studies (Supplementary Fig. 1). Although roughly one-third of the SWNTs are metallic, purely metallic transport pathways between the S–D electrodes can be eliminated by suitably engineering the average tube lengths and the network layouts: for the present purposes, we used soft lithography and reactive-ion etching to cut fine lines into the networks. The resulting network strips are oriented along the overall direction of transport, with widths designed to reduce the probability of metallic pathways below a practical level without significantly reducing the effective thin-film mobility of the network.

Figure 1b shows a scanning electron micrograph of a region of an integrated circuit just before deposition of the gate dielectric. A magnified view of a part of the SWNT network in the channel of one of the devices (Fig. 1c; the S–D electrodes are to the right and left, outside the field of view) reveals narrow, dark horizontal lines, corresponding to the etched regions. The critically important role of these features in determining the electrical characteristics can be quantified through first-principles modelling studies that consider percolative transport through sticks with average lengths and layouts (for example etched lines, densities of SWNTs and so on) corresponding to experiment[20]. Fig. 1d shows the distribution of current flow in a typical case, in which the colour indicates the current density in the

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on-state of the device. In addition to providing guidance on optimal design (Fig. 2a), these simulations reveal that networks with this geometry and coverage (~0.6%) distribute current evenly, thereby serving as an effective film for transport. A typical device incorporates ~16,000 individual SWNTs. The circuits are completed in top-gate configurations by deposition and patterning of high-capacitance, hysteresis-free dielectrics enabled by low operating voltages (~40 nm of hafnium dioxide) directly on the tubes, followed by gate metallization and the addition of vias and interconnects. Figure 1e shows a representative system, complete with arrays of isolated enhancement-mode (lower right region) and depletion-mode (lower middle region) transistors, various logic gates (lower left part), and two four-bit row decoders each twenty logic gates in size (middle and upper parts). Fabrication details are further described in the Methods.

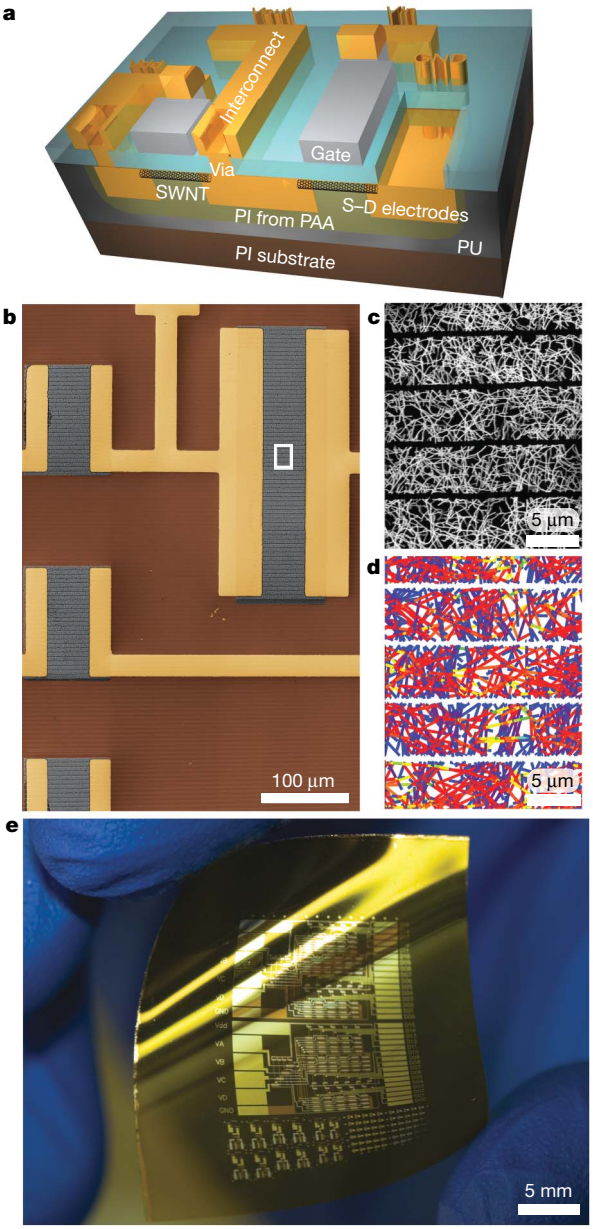

Figure 1 | Illustration, scanning electron microscope images, theoretical modelling results and photographs of flexible SWNT integrated circuits on plastic. a, Cross-sectional diagram of a SWNT PMOS inverter on a PI substrate. PI, polyimide; PU, polyurethane; PAA, polyamic acid; $V_{dd} \equiv$ Vdd, common power supply voltage; $V_{out} \equiv$ Vout, output voltage; $V_{in} \equiv$ Vin, input voltage; GND, common ground. **b**, Scanning electron microscope image of part of the SWNT circuit, made before deposition of the gate dielectric, gate or gate-level interconnects. The S–D electrodes (gold) and substrates (brown) had been colourized to highlight the SWNT network strips (black and grey) that form the semiconductor. **c**, Magnified view of the network strips corresponding to a region of the device channel highlighted with the white box in **b**. **d**, Theoretical modelling results for the normalized current distribution in the on-state of the device (view as in **c**), where colour indicates current density (yellow, high; red, medium; blue, low). **e**, Photograph of a collection of SWNT transistors and circuits on a thin sheet of plastic (PI).

Figure 2 summarizes measurements on individual transistors. Figure 2a illustrates the predicted and measured influences of the geometry of the etched lines described above on devices with coarse dimensions (that is, channel lengths $L_C = 100\ \mu m$), selected to be compatible with established low-cost patterning techniques such as screen printing[21], and with sufficiently high densities of SWNTs to achieve good performance and uniformity as a thin-film semiconductor. For widths of ~5 μm, the etched lines increase the on/off ratios by up to four orders of magnitude, while reducing the transconductances (g_m) by only ~40%. Figure 2b, c shows characteristics of transistors with this geometry, illustrating well-behaved responses with minimal hysteresis and with excellent channel-width-normalized transconductances (as high as 0.15 $\mu S\ \mu m^{-1}$ and typically 0.12 $\mu S\ \mu m^{-1}$ for $L_C \geq 50\ \mu m$, which corresponds to an estimated cut-off frequency of >100 kHz), device mobilities (μ_{eff}; as high as ~80 $cm^2\ V^{-1}\ s^{-1}$ and typically ~70 $cm^2\ V^{-1}\ s^{-1}$ as calculated using standard models of metal–oxide–semiconductor field-effect transistors with measured gate capacitances (Supplementary Fig. 2), for both the linear and the saturation regimes), and subthreshold swings (S; as low as 140 mV dec^{-1} and typically ~200 mV dec^{-1}).

The transconductances and the subthreshold behaviours, in particular, exceed those that have been demonstrated in flexible integrated circuits on plastic with organic thin-film semiconductors ($g_m < 0.02\ \mu S\ \mu m^{-1}$ for $L_C \approx 50\ \mu m$, $S > 140$ mV dec^{-1})[22,23] or with silicon nanowires ($g_m < 0.01\ \mu S\ \mu m^{-1}$ for $L_C \approx 50\ \mu m$, $S > 280$ mV dec^{-1})[24], and are competitive with the best reports of p-channel single-crystalline silicon ribbons ($g_m \approx 0.25\ \mu S\ \mu m^{-1}$ for $L_C = 50\ \mu m$, $S \approx 230$ mV dec^{-1})[25]. Under low-to-moderate bias conditions, the on/off ratios can be as high as 10^5 (Fig. 2f and Supplementary Fig. 3a), and typically ~10^3, for transistors with this geometry. The inset in Fig. 2b and Supplementary Fig. 4a show a decrease in the on/off ratio with increasing drain–source voltage (V_{DS}), which is due primarily to the slightly ambipolar nature of the device operation. These ratios also decrease with L_C (Supplementary Fig. 1b). The favourable d.c. properties of long-channel devices can be achieved at short L_Cs, for improved operating speeds, either by use of correspondingly shorter SWNTs and narrower etched stripes, as suggested by modelling results, or by using pre-enriched semiconducting SWNTs[26].

The threshold voltage (V_T) can be controlled by using gate metals with different work functions, because the high-capacitance gate dielectrics reduce the relative contribution of voltage across the dielectric to V_T (ref. 27). For example, replacing gold with aluminium as the gate metal shifts V_T by −(0.6–0.8) V, thereby changing the device operation from depletion mode to enhancement mode (Fig. 2b). Systematic bending tests of individual devices and inverters showed no significant change in device performance during inward or outward bending to radii as small as ~5 mm (Fig. 2d). Collectively, these properties are as good as or better than those of previously reported devices based on SWNT random networks, in spite of the moderate decreases in g_m associated with the etching procedures. Transistors that use dense, perfectly aligned arrays of SWNTs have improved performance, that is, device mobility up to 2,500 $cm^2\ V^{-1}\ s^{-1}$, but these layouts cannot be formed readily with solution deposition techniques[17]. As such, they are not relevant for the type of printed, flexible electronics applications contemplated here.

For use in integrated circuits, the yields and performance uniformity of the transistors are critically important. We examined these aspects through measurements on more than 100 devices (Fig. 2e, f and Supplementary Fig. 5). The results show standard deviations of ~20% for the normalized on-state current (I_{on}) and ~0.05 V for V_T. The former result is quantitatively in agreement with percolation theory, illustrated also in Fig. 2e. Although on/off ratios vary by roughly two orders of magnitude, most of the values are $>10^3$. The distribution (Fig. 2f) indicates no correlation with V_T (suggesting the importance of extrinsic doping effects on SWNTs[28]), and has a width which is much larger than that predicted by percolation models (Fig. 2f, inset) that do not explicitly include effects of S–D contacts. These results strongly indicate that the variation in on/off ratio results from electron conduction caused by tunnelling through the Schottky barriers at the S–D contacts (Fig. 2f, inset)[29]. Although unnecessary for the circuits reported here, doping techniques similar to those demonstrated in single-SWNT devices can be used to suppress the ambipolar behaviour and improve on/off ratio uniformity[30]. Such doping methods could also help to eliminate decreases in on/off ratio with increasing V_{DS}, as mentioned previously and illustrated in Fig. 2b and Supplementary Fig. 4a.

We find that standard models for silicon device technologies can capture macroscopic device behaviours. Figure 2b, c illustrates the level of agreement that can be achieved with a level-3 p-channel metal–oxide–semiconductor (PMOS) SPICE (simulation program for integrated circuits emphasis) model that uses a parallelly connected exponential current source controlled by both gate voltage and V_{DS} to mimic the electron tunnelling current. This level of compatibility with established simulation tools allows the use of existing sophisticated computer-aided design platforms developed for silicon integrated circuits.

As the first step towards large-scale integration, we modelled and then built 'universal' logic gates. Figure 3a shows a circuit diagram of a PMOS inverter with enhancement load. The inverter exhibits well-defined static voltage transfer characteristics, consistent with simulation, at a supply voltage of −5 V (Fig. 3b). The rise in output voltage with increasing positive input voltage is due to the ambipolar behaviour of the driving transistor. Maximum voltage gains of ~4, together with good noise immunity with a transition-region width of <0.8 V and a logic swing of >3 V are achieved, indicating that the inverter can be used to switch subsequent logic gates without losing logic integrity. Measuring their a.c. responses generated a

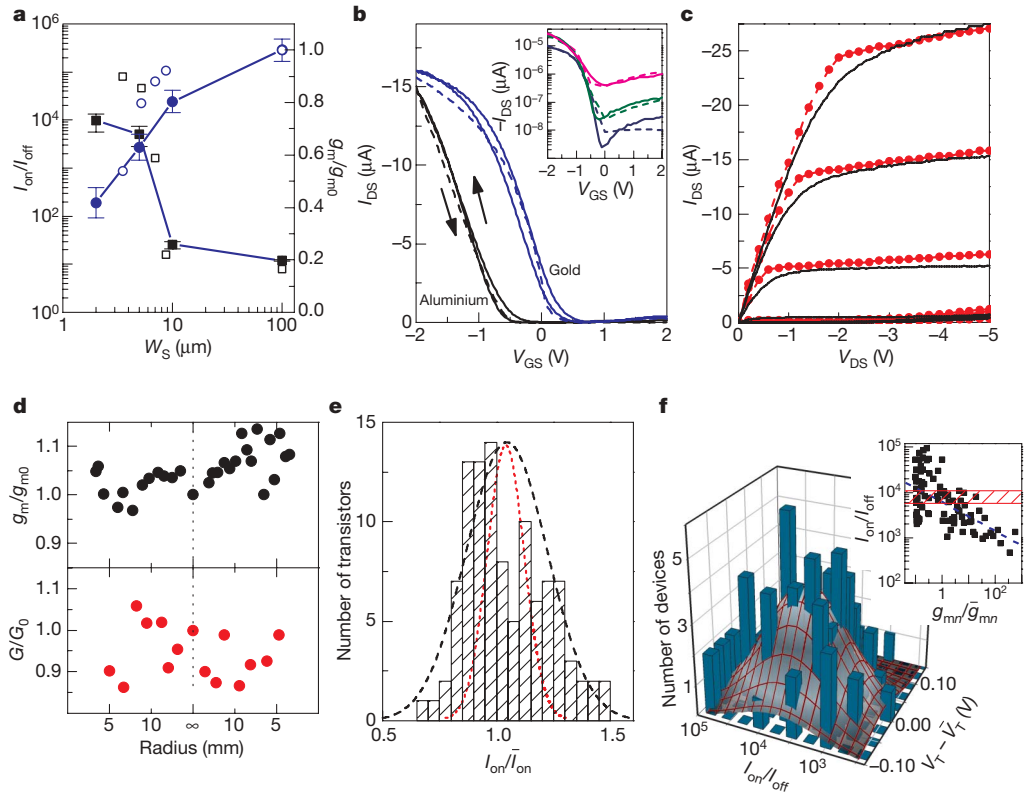

Figure 2 | Electrical properties of thin-film transistors that use SWNT network strips for the semiconductor, on thin plastic substrates. a, The measured (filled) and simulated (open) influence of the width of the strips (W_S) on the on/off ratio (I_{on}/I_{off}; black) and normalized transconductance (g_m/g_{m0}, where g_{m0} represents the response without strips; blue) of transistors with channel lengths of 100 μm. Error bars represent s.d. of $n = 6$ thin-film transistors. **b**, Measured (solid) and simulated (dashed) V_{GS}–I_{DS} characteristics of depletion-mode (blue) and enhancement-mode (black) SWNT thin-film transistors whose channel widths are 200 μm and whose channel lengths are 100 μm. $V_{DS} = -1$ V; I_{DS}, drain–source current; V_{GS}, gate–source voltage. Inset, V_{GS}–I_{DS} curve of the enhancement-mode device plotted on a logarithmic scale, with $V_{DS} = -0.5$ V (navy), −2 V (green), −5 V (magenta). **c**, Measured (black) and simulated (red) V_{DS}–I_{DS} characteristics of an enhancement-mode thin-film transistor (V_{GS} changed from −2 V to 2 V in steps of 0.5 V). **d**, Plots of g_m/g_{m0} for a thin-film transistor and G/G_0 (normalized voltage gain) for an inverter as functions of bend radius (g_{m0} and G_0 denote the responses in the unbent state). **e**, Histogram of I_{on} (measured at $V_{DS} = -0.2$ V; $\bar{I}_{on}$, averaged on-state current) with superimposed gaussian fitting for measured (dashed black) and simulated (dashed red) results. **f**, Two-dimensional histogram showing the correlation between the I_{on}/I_{off} (measured at $V_{DS} = -0.2$ V) and threshold voltage distributions ($\bar{V}_T$, averaged threshold voltage). Inset, correlation between I_{on}/I_{off} and normalized n-branch transconductance ($\bar{g}_{mn}$, averaged n-branch transconductance). The dashed blue line depicts the result of a linear fit. The hatched red area shows the distribution of I_{on}/I_{off} predicted by percolation models that do not explicitly account for the influence of source–drain contacts.

Bode magnitude plot closely resembling the characteristics of low-pass amplifiers, with operation in the kilohertz range even for devices with long channels ($L_C \approx 100\,\mu m$) and significant channel-width-normalized overlap capacitance ($\sim 40\,fF\,\mu m^{-1}$; Fig. 3c). The ability to achieve switching speeds in the kilohertz range with device geometries that are compatible with techniques such as screen printing is important for the potential use of such SWNT networks in low-cost, printed electronics[21]. By adding another driving transistor to the inverter, either in parallel with the pull-down transistor to incorporate OR logic (Fig. 3d, e) or in series to incorporate AND logic (Fig. 3g, h), it is possible to construct NOR and NAND logic gates, respectively. The output characteristics and simulation results are presented in Fig. 3f, i. Voltage amplification is observed in all cases.

All of these experimental and computational components can be used together to yield SWNT-based digital circuits (Fig. 4a). The largest circuit in this chip is a four-bit row decoder (Fig. 4b), designed using modelling tools and measured characteristics of stand-alone logic gates. This circuit incorporates 88 transistors, in four inverters and a NOR array, with the output of the inverter serving as one of the inputs for the NOR gate. The circuit diagram (Fig. 4c) is configured such that any given set of inputs only give one logic-'1' output. The input–output characteristics of the decoder are shown in Fig. 4d and Supplementary Fig. 6, which demonstrates its ability to decode a binary-encoded input of four data bits into sixteen individual data output lines, at frequencies in the kilohertz range. These results suggest that SWNT networks can form the basis for a potentially interesting and scalable alternative to conventional organic or other classes of semiconductors for flexible integrated circuitry applications. The development of optimized materials and solution-printing techniques for fabricating SWNT-based integrated circuits that achieve the performance levels reported here, together with further exploration of circuit- and systems-level implementation, represent some directions for future work.

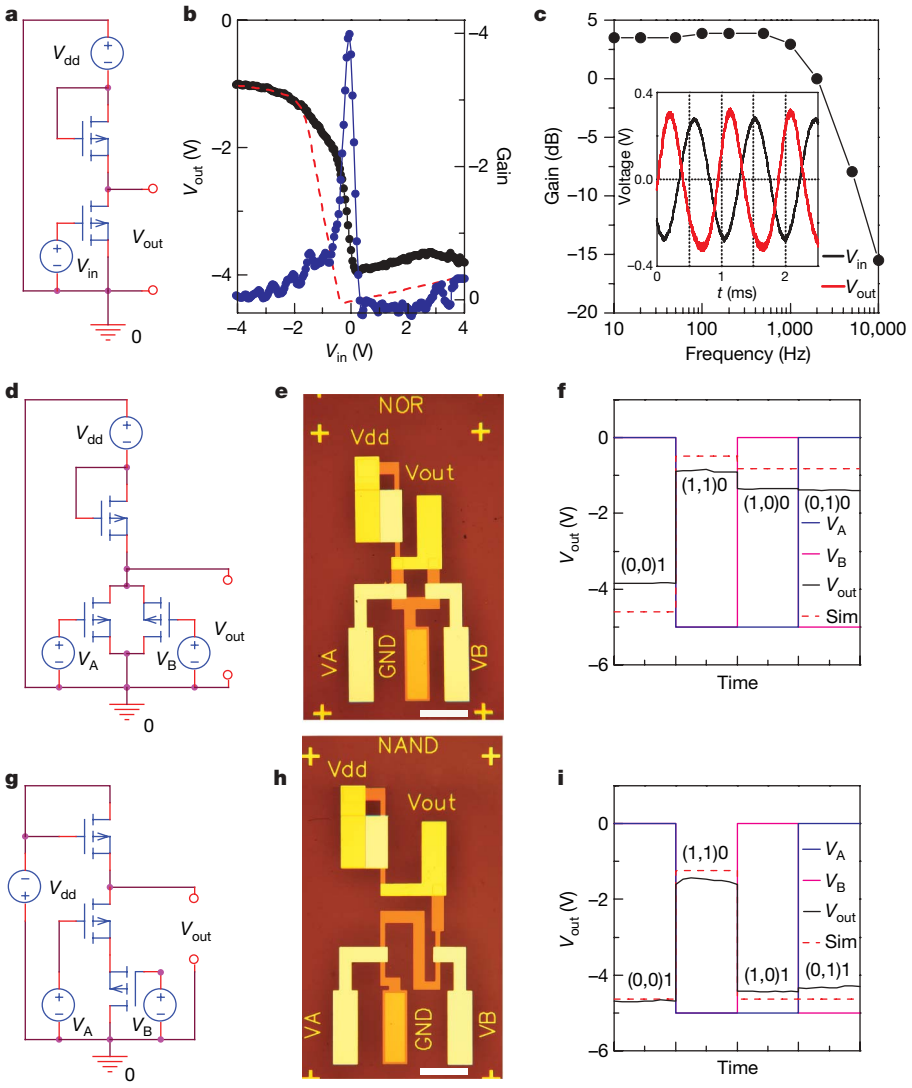

Figure 3 | Circuit diagram, optical micrographs, output–input characteristics and circuit simulation results for different logic gates. **a–c**, Inverter. **d–f**, NOR gate. **g–i**, NAND gate. We adopt a negative logic system. The V_{dd} applied to these logic gates is −5 V relative to GND. The logic-'0' and -'1' input signals of two terminals ($V_A \equiv$ VA and $V_B \equiv$ VB) of the NOR and NAND gates are driven by 0 V and −5 V, respectively. The logic-'0' and -'1' outputs of the NOR gate are −(0.88–1.39) V and –3.85 V, respectively. The logic-'0' and -'1' outputs of the NAND gate are –1.47 V and −(4.31–4.68) V, respectively. In **b**: black, V_{out}; blue, gain. In **f** and **i**, any specific combination of input–output signals is indicated as (logic address level inputs)logic address level ouput, and the timescales on the x axes are omitted because data collection involved the switching of voltage settings by hand. In **b**, **f** and **i**, dashed red lines represent circuit simulation results. Scale bars in **e** and **h**, 100 μm.

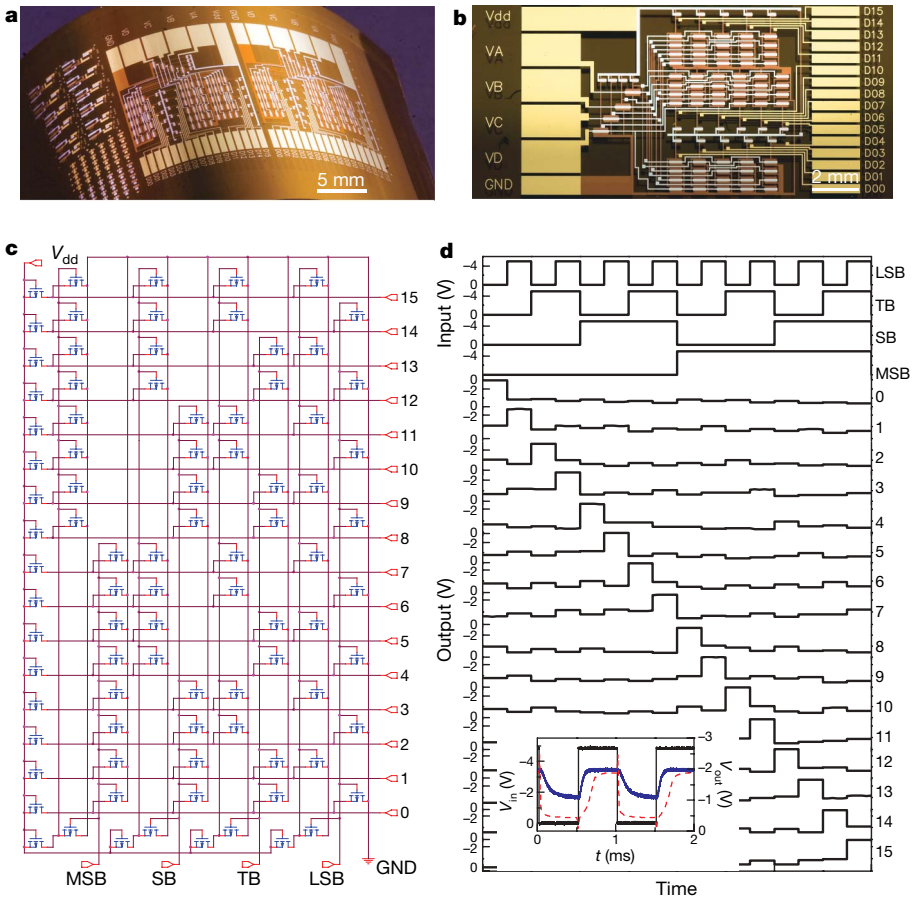

Figure 4 | Medium-scale integrated circuits based on SWNT network strips, on a thin plastic substrate. a, Optical image of a flexible SWNT integrated circuit chip bonded to a curved surface. **b**, Optical micrograph and **c**, circuit diagram of a four-bit row decoder with sixteen outputs (0–15). The bits are designated as most significant bit (MSB), second bit (SB), third bit (TB) and least significant bit (LSB). The V_{dd} applied was −5 V relative to GND. **d**, Characteristics of the four-bit decoder. In descending order, the first four traces are inputs, labelled LSB, TB, SB and MSB on the right-hand side; the remaining traces, labelled '0' to '15', show the output voltages of the sixteen outputs. Inset, measured (blue) and SPICE-simulated (red) dynamic response of one output line under a square-wave input pulse (black) at a clock frequency of 1 kHz.

METHODS SUMMARY

The process flow for fabricating SWNT integrated circuits on plastics is depicted in Supplementary Fig. 8. SWNTs were synthesized by chemical vapour deposition on silicon dioxide–silicon wafers and then etched into strips using an experimentally simple, optical soft lithography technique. Standard photolithography, electron-beam evaporation, gold wet chemical etching and oxygen plasma etching were used to pattern S–D electrodes and isolate each device. We then used a film of polyamic acid to encapsulate predefined S–D electrodes and SWNT networks on the growth wafers for transfer to a polyimide substrate coated with liquid polyurethane. Subsequent curing of the liquid polyurethane and polyamic acid completed the transfer process. Metal gates were defined on top of a high-capacitance dielectric (~40-nm) layer of hafnium dioxide. Vias and windows for probing were opened by wet etching (dipped into concentrated hydrofluoric acid aqueous solution) through patterned photoresist. Last, another level of interconnect metallization formed local interconnections defined previously with the gate and source–drain metal layers. All electrical measurements were carried out in air using a semiconductor parameter analyser (Agilent, 4155C). Alternating-current input was provided by a function generator (GW Instek, GFG-8219A) and output was read using a standard oscilloscope (Tektronix, TDS 3012B). The stick percolation simulations involved finite-size, first-principles two-dimensional numerical models based on generalized heterogeneous random network theory. Device and circuit simulation used the commercial software package HSPICE (Synopsis).

Full Methods and any associated references are available in the online version of the paper at www.nature.com/nature.

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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Author Contributions Q.C., H.K. and J.A.R. designed the experiments. Q.C., H.K. and C.W. performed the experiments. Q.C., N.P., J.P.K., M.S., K.R., M.A.A. and J.A.R. analysed the data. Q.C. and J.A.R. wrote the paper.

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METHODS

Synthesis of SWNT networks. SWNT random networks were grown by chemical vapour deposition on silicon wafers with 100-nm-thick layers of thermal oxide. The process began with cleaning the SiO_2–Si wafer with piranha solution (a 3:1 volumetric mixture of concentrated sulphuric acid to 30% hydrogen peroxide solution). This process not only removed organic contaminants but also hydroxylated the re-oxidized SiO_2 surface, making it extremely hydrophilic to enable uniform deposition of catalyst[31]. This catalyst consisted of ferritin (Aldrich; diluted with de-ionized water at a volumetric ratio of 1:20 to control the density of catalyst) deposited onto the SiO_2–Si surface by adding methanol[32]. The wafer was then heated to 800 °C in a quartz tube to oxidize ferritin into iron oxide nanoparticles. After it had cooled down to room temperature, the quartz tube was flushed with a high flow of argon gas (1,500 s.c.c.m.) for cleaning and then heated up to 925 °C in hydrogen atmosphere (120 s.c.c.m.), which reduced iron oxide to iron. After the temperature had reached 925 °C, methane (1,500 s.c.c.m.) was released into the quartz tube as a carbon source while maintaining the hydrogen flow. Growth was terminated after 20 min, and the chamber was then cooled in hydrogen and argon flow. The density of the SWNT networks formed in this fashion was controlled by the dilution ratio of the ferritin solution, leaving the other aspects of the growth and processing unchanged.

Cutting strips into the SWNT networks with phase-shift lithography and reactive-ion etching. Elastomeric phase masks with depths of 1.8 μm, widths of 5 μm and periodicities of 10 μm were fabricated from relief structures defined by lithography and anisotropic etching through a casting and curing procedure[33]. AZ5214 photoresist, diluted with AZ1500 thinner in a 1:1 volumetric ratio, was spin-cast onto the SiO_2–Si wafer with SWNT networks at 5,000 r.p.m. and then baked at 95 °C for 1 min to afford a flat and solid 300-nm-thick photoresist layer. After cleaning the surface of phase mask with Scotch Tape, we placed it into conformal contact with the photoresist layer, flood exposed the resist by shining the i-line (365-nm) output of a mercury ultraviolet lamp through the mask, and then removed the mask. The SiO_2–Si substrate was then baked at 112 °C for another minute, followed by a flood exposure of ultraviolet light. Development in AZ MIF327 developer for 40 s created a regular array of submicrometre-wide spacings in the photoresist layer, with 5-μm periodicity. Photoresist strips of 5-μm width could also be generated by conventional photolithography with much wider spacings (~5 μm). Although large spacings lead to a reduction in effective channel width and an increase in parasitic capacitance, we used this technique instead of phase-shift lithography in fabricating the transistors used in the decoder circuits because conventional photolithography is easier to perform. We next used oxygen reactive-ion etching (200 mtorr, 20 s.c.c.m., O_2 flow, 100-W radio frequency power) to remove the exposed SWNTs. Last, the photoresist layer was removed by soaking in acetone for 1 h. Successfully using optical soft lithography to pattern the only sub-10-μm features in our circuits suggests the potential to use low-cost, low-resolution printing-like processes to define all features in the circuits[34].

S–D patterning and device isolation. A gold film (30 nm) was deposited by electron-beam evaporation (Temescal BJD 1800; base pressure of 3×10^{-6} torr) onto a SiO_2-Si substrate with predefined nanotube strips. We then used standard ultraviolet photolithography to pattern the S–D electrodes and interconnects using an etch-back scheme with a commercial wet etchant (Transene, TFA) to remove gold in exposed areas. After that we used oxygen reactive-ion etching (200 mtorr, 20 s.c.c.m., O_2 flow, 100-W radio frequency power) to remove SWNTs outside channel regions that were protected by a patterned layer of photoresist (Shipley 1805).

This step can also be carried out on the plastic substrate after transfer, which avoids the dimensional instability associated with polymer shrinkage during the curing process and device failure due to incomplete transfer of the S–D electrodes. However, it will lead to inferior device performance, owing to the synergetic effect of a smaller contact area between the S–D electrodes and the partially embedded SWNTs, as well as a smaller effective channel width when we use photolithography to define SWNT strips as described above on polymer surfaces that are relatively rough (in comparison with the surface roughness of the silicon wafers; Supplementary Fig. 3). Therefore, this approach is only used in fabricating row-decoder circuits, which process has the highest requirements on device yield.

Transfer-printing process. The transfer-printing process involved spin-casting (1,500 r.p.m., 60 s) polyamic acid (PAA, Aldrich) onto the SiO_2–Si wafer with SWNTs and S–D patterns, and then heating at 110 °C for 3 min to remove the solvent. On the target polyimide (PI) substrate (DuPont, Kapton E; thickness ~50 μm), we spin-cast (5,000 r.p.m., 60 s) a film of polyurethane (PU, NEA 121). Before this step, we thermally cycled the PI between 30 °C and 270 °C to improve its dimensional stability[35]. We laminated this PU-coated substrate on top of the PAA–SiO_2–Si wafer with the PU facing towards the PAA film, and applied pressure on the back of the wafer to remove air bubbles. Heating them together to 135 °C for 30 min thermally cured the PU film, thereby binding the PI substrate to the PAA film. Peeling off the PI substrate lifted the film of PU–PAA with embedded SWNT networks and S–D electrodes off the SiO_2–Si wafer, with one side of the S–D electrodes exposed. In the final step a vacuum oven (base pressure of 300 mtorr) with nitrogen flow (500 s.c.c.m.) was used to thermally cure the PAA to the PI through imidization reaction[36].

Gate dielectric deposition. The gate dielectric was deposited on top of the PAA after the latter had been cured to the PI. In the first step, 30 nm of HfO_2 was deposited by electron-beam evaporation (Temescal BJD 1800; base pressure of 2×10^{-6} torr) at a relatively low deposition rate (<0.5 Å s^{-1}) as measured by a quartz crystal thickness monitor. This layer served as a protective layer for SWNTs against highly reactive precursors used in a subsequent atomic layer-deposition (ALD) process[37]. After evaporation, the sample was transferred immediately to the ALD chamber to preserve the hydrophilicity of the freshly deposited HfO_2, which facilitates the growth of high-quality, pin-hole-free ALD film. The ALD HfO_2 film (12 nm) was deposited using a commercial ALD reactor (Cambridge Nanotech, Savannah 100). One ALD reaction cycle consists of one dose of water followed by a 5-s exposure and a 300-s purge, and then one dose of $Hf(NMe_2)_4$ followed by another 5-s exposure and a 270-s purge. During deposition, the nitrogen flow was fixed at 20 s.c.c.m. and the chamber temperature was set at 120 °C. The low deposition temperature prevents cracking of HfO_2 due to the mismatch of thermal expansion coefficients but requires very long purging time to remove excess precursors absorbed on the surface, to prevent chemical-vapour-deposition-type reactions in the chamber[38].

Via opening and gate/interconnect pattering. After the dielectric had been deposited, the gate pattern was defined in another photolithography step. A lift-off scheme was used to allow alignment of gate electrodes to the S–D electrodes using previously patterned alignment markers. Metal for the gate electrodes (120 nm aluminium or 2 nm chromium–120 nm gold) was deposited by electron-beam evaporation (Temescal BJD 1800; base pressure of 3×10^{-6} torr). In this metallization step (as well as the next step, for defining interlayer interconnects) two angled evaporations (incidence angle, 60°) with substrates placed at opposite orientations and a blanket evaporation (incidence angle, 90°) were performed to ensure that the metal layers covered the underlying surface topography, thereby avoiding open points that would otherwise form in the interconnect lines. In all cases, the deposition rate must be within 4–7 Å s^{-1}. If the evaporation rate is lower than 4 Å s^{-1}, accumulated heat can lead to cracking of the PU layer; if the evaporation rate is higher than 7 Å s^{-1}, the strain accumulated in the metal film can lead to defect formation in the lift-off process.

Following deposition, the lift-off was accomplished by soaking in acetone for 10 min, followed by a short ultrasonic treatment (30 s) to ensure that the lift-off process was complete. Because the SWNTs were covered by HFO_2, the ultrasonic treatment did not damage the nanotube network. (Prolonged acetone soaking can dissolve, at a low rate, the PI cured from PAA, owing, presumably, to incomplete imidization.) Contact pads for probing and vias for interlayer interconnects were exposed by photolithography using AZ 5214 photoresist. A hard bake (120 °C, 2 min) of the photoresist was performed before hydrofluoric acid etching (4 s in concentrated HF solution) of HfO_2 (ref. 39) to improve the adhesion between the photoresist and the HfO_2. We note here that in this step the gold pads patterned in the S–D layer under vias must be larger in size than the via holes to protect the PU from being etched by the hydrofluoric acid through acidolysis reaction. The interlayer interconnect (5 nm chromium–100 nm gold) was patterned using a lift-off process and photolithography. The patterning of gate electrodes and interconnects were carried out separately because (1) the predefined gate layer can also serve to protect the gate dielectric against possible defects existing in the photoresist mask layer, preventing the creation of pin holes in the channel region in the wet etching step, and (2) aluminium tends to form a poor contact with the gold S–D electrodes, possibly because of intermetallic formation[40], such that a different interconnect metal, such as the chromium–gold combination, was necessary when using aluminium gates. Finally, the completed device/circuit was aged in air for 24 h, and then thermally annealed at 120 °C for 30 min, to achieve stable operation.

Device and circuit characterizations. Direct-current measurements of SWNT transistors and circuits were carried out in air using a semiconductor parameter analyser (Agilent, 4155C), operated by Agilent Metrics I/CV Lite software (version 2.1) and GBIP communication. Triaxial and coaxial shielding was incorporated into a Signatone probe station to achieve a better signal-to-noise ratio. A precision LCR meter (Agilent, 4282A) was used for capacitance and impedance measurements. Alternating-current input signals were generated by a function generator (GW Instek, GFG-8219A). The output signals were measured using a standard oscilloscope (Tektronix, TDS 3012B).

Stick percolation simulation. We constructed a sophisticated first-principles numerical stick percolation model for the above random SWNT network by generalizing the random network theory[20,41,42]. The model randomly populates a two-dimensional grid with sticks of fixed length (L_S) and random orientation (θ) and determines I_{on} through the network by solving the percolating electron transport through individual sticks. In contrast to classical percolation, the SWNT network is a heterogeneous network: one-third of the carbon nanotubes are metallic and the remaining two-thirds are semiconducting. Because L_C and L_S here are much larger than the phonon mean free path, linear-response transport obviates the need to solve the Poisson equation explicitly. The system is well described by drift–diffusion theory within individual stick segments of this random stick network. The low-bias drift–diffusion equation, $J = q\mu n \mathrm{d}\varphi/\mathrm{d}s$ (where J is current density, q is carrier charge, μ is mobility, n is carrier density, φ is electropotential and s is length along the tube), when combined with the current continuity equation, $\mathrm{d}J/\mathrm{d}s = 0$, gives the non-dimensional potential φ_i along tube i as:

$$\frac{\mathrm{d}^2\varphi}{\mathrm{d}s^2} - C_{ij}(\varphi_i - \varphi_j) = 0$$

Here $C_{ij} = G_0/G_1$ is the dimensionless charge-transfer coefficient between tubes i and j at their intersection point. $G_0 \approx 0.1\, e^2/h$ and $G_1 = qn\mu/\Delta x$ are the mutual- and self-conductances of the tubes, respectively, and e is the elementary charge, h is Planck's constant and Δx is the grid spacing. The density of the random stick network is measured in area normalized by L_S, and the density of our SWNT network was ~40 according to scanning electron microscope measurements. The finite-length strips were simulated by imposing a reflecting boundary condition at the edge of each strip.

SPICE simulation. We described the behaviour of the SWNT thin-film transistors as that of a PMOS field-effect transistor parallelly connected with an exponential current source dependent on voltage (V_{GS} and V_{DS}). The PMOS field-effect transistor was modelled using a standard square-law model with channel-length modulation and S–D resistance effects. The exponential current source was used to mimic the ambipolar current ($I_{ambipolar}$), which led to an exponential increase in I_{off} with increasing V_{DS}. We expressed the exponential term in the form of a Taylor series

$$I_{\mathrm{ambipolar}} = K_n(V_{GS} + V_{G0})\left(1 + V_x + \frac{V_x^2}{2} + \cdots\right)$$

where K_n and V_{G0} are fitting parameters and V_x is defined as $V_x = V_{\mathrm{Threshold}} + \alpha V_{GS} - \beta V_{DS}$, and the first three terms were incorporated into the SPICE model. All fitting parameters were extracted from measured I–V characteristics (summarized in Supplementary Table 1). The channel-length scaling behaviour of these SWNT random network transistors can only be captured by our percolation modelling. The results of such models (for example, off-state resistances) can be used as inputs to the SPICE models to capture the full range of behaviours.

The above model was then used in designing and simulating digital logic circuits[43]. In transient simulation, load capacitance was calculated automatically from measured overlap capacitance ($330\,\mathrm{nF\,cm^{-2}}$) and gate capacitance ($80\,\mathrm{nF\,cm^{-2}}$) per unit area as well as estimated contact resistance ($11\,\mathrm{k\Omega}$), by the HSPICE program. Although the measured voltage responses of fabricated circuits agreed well with the design specifications, the current load responses showed behaviour only qualitatively similar to the simulation results (Supplementary Fig. 9). This deviation may be due to the relatively large batch-to-batch variations in device performance, which influenced the current load more significantly than they did the voltage responses.

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Medium Scale Carbon Nanotube Thin Film Integrated Circuits on Flexible Plastic Substrates (Online Supplementary Information)

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Supplementary Discussion

Scaling Analysis of Single-walled Carbon Nanotube (SWNT) Thin-film Transistors (TFTs)

Channel length (L_C) scaling properties of SWNT TFTs must be explored prior to successful circuit design and integration. The device on current scales linearly with channel width (W), which can be easily understood since the channel width only changes the number of the stripes in the channel. Fig. S-1a shows the transfer characteristics of an array of SWNT TFTs with different L_Cs. The W normalized on resistance ($R_{on}W$) under different gate voltages (V_{GS}) increase linearly with the decrease of L_Cs (Fig. S-1a, inset). The contact resistance, as determined from the y axis intercept, is much smaller compared to the channel resistance, which indicates that these transistors are not contact limited. Fig. S-1b presents the effective mobility (μ_{eff}) and device on/off ratio (I_{on}/I_{off}) as a function of L_C. μ_{eff} decreases only slightly at small L_Cs, confirming that the Schottky barrier between SWNT and Au has limited effects on device performance. More importantly, μ_{eff} and threshold voltage (V_T) extracted from linear region and

saturation region doesn't show significant difference (Fig. S-1 b & c). It is an advantage compared with devices built on organic transistors, whose mobility is dependent on V_{GS} as a result of their variable range hopping transport mechanism.[44] Device on/off ratios show, on the other hand, very strong variation with L_C, increasing sharply and then gradually saturating for L_C larger than 50 μm. This correlation derives from purely metallic pathways between source/drain (S/D) electrodes that increase in number with decreasing L_C, for a given tube density and average tube length. These variations are quantitatively consistent with percolative modelling.[20] The decrease of on/off ratio at high source-drain voltage (V_{DS}) is caused by band-to-band tunnelling current and the off current can be reduced through doping scheme reported for single SWNT devices.[30] In conclusion, the scaling properties of SWNT TFTs allow us to predict properties of a given SWNT TFT based on measurements performed on another device with different geometries, which forms the basis for our rational circuit design efforts.

Gate Capacitance of SWNT TFTs

Gate capacitance is a crucial parameter for transistors, serving as the basis to extract μ_{eff} and estimate the transient behaviour of transistors/circuits. Here we present the first direct capacitance measurements of SWNT random networks. We used a structure similar to the layout of our SWNT TFTs, where the capacitor forms between the top round-shaped electrodes and the nanotube network beneath it (Fig. S-2, Inset). The measurements were performed at 100 kHz under serial connection model because the leakage current is small but the contact resistance, especially the contact resistance between SWNTs and Au electrodes is significant. Measured capacitance-voltage (*C*-*V*) characteristics closely resemble previous results based on individual tubes, with symmetric *C*-*V* curves in the depletion region and accumulation region reflecting the underlying band structure symmetry of SWNTs (Fig. S-2).[45] The dip of capacitance at the device off state is wide and shallow, possibly due to the diameter distribution of nanotubes in the

network. The measured gate capacitance, 85 nF/cm^2, is about one third of measured thin film capacitance of 42nm thick HfO_2, which is in good agreement with previous modelling results.[46]

Distribution of Device On/off Ratios

Compared with other device parameters, the on/off ratios show much larger variation, as shown in Fig. 2f and Fig. S-3. The origin of this distribution is likely due to electron injection current, from the slightly ambipolar nature of the device operation. Devices with high electron conduction current generally have low on/off ratios and, as a consequence, larger subthreshold slopes (Fig. S-3 a).

The Dependence of Off-state Current (I_{off}) on Drain-source Voltage (V_{DS})

Our *p*-channel SWNT top-gate transistors show slight ambipolar behaviour. As a result, I_{off} contains, in general, contributions from electron injection and transport through semiconducting pathways through the networks as well as ohmic transport of electrons through metallic pathways.[47] For devices with long L_Cs, whose on/off ratio is high (~> 1,000) for low V_{DS}, metallic tube paths do not exist or are very few. In this case, I_{off} mainly comes from undesired electron injection. This behaviour leads to superlinear increases in I_{off} with linearly increasing V_{DS} as shown in Fig. S-4a. By contrast, for devices with small L_Cs, which usually have low on/off ratio even for low V_{DS}, metallic pathways become the dominant contributor to I_{off}. Here, I_{off} increases linearly with V_{DS}, as shown in Fig.S-4b.

Distribution of Effective Device Mobility and Subthreshold Swing

The distribution of μ_{eff} and subthreshold swing (S) were examined through measurements on more than 100 devices (L_C 100 μm, W 200 μm), as summarized in Fig. S-5. We find standard deviations of ~10% for μ_{eff} and ~15% for S, which are sufficient for most envisioned applications of flexible electronics.

Switching Speed Characteristics of the Four-bit Decoder Circuit

The operation speed of the decoder circuit was characterized by measuring one output signal with one alternating current input. Results show that the decoder can be successful switched in kHz regime, with a $\tau \approx 50$ μs rise time and a $\tau \approx 100$ μs fall time (Fig. S-6). The experimental results agree reasonably well with transient simulation results based on previously described SPICE model for SWNT TFTs.

Operational Stability Test of SWNT TFTs

We observed good stability in our top-gate SWNT transistors as illustrated by data in Fig. S-7. These measurements involved electrically cycling the devices in ambient conditions (relative humidity ≈ 90 % and T = 20 ^{o}C~25 ^{o}C) between V_{GS} = -2 and 0 V at V_{DS} = -0.2 V. The data indicate negligible changes in I_{on} or on/off ratio for more than two hundred cycles.

Estimation of Some Properties of SWNT TFTs

Estimated total number of SWNTs involved in transport for a typical device:

$$N = \frac{W}{L_S} \cdot \frac{L_C}{L_S} \cdot D = \frac{200}{7} \times \frac{100}{7} \times 40 = 1.6 \times 10^4 \, tubes$$

where W is channel width, L_C is channel length, L_S is average tube length and D is area nanotube density normalized by L_S, respectively.

Estimated total surface coverage by SWNTs in channel region:

$$\rho = \frac{N \cdot d_{NT} \cdot L_s}{W \cdot L_C} = \frac{1.6 \times 10^4 \, tubes \times 1.5 nm \times 5 \mu m}{200 \mu m \times 100 \mu m} = 0.6\%$$

where N is number of nanotubes in channel region, and d_{NT} is nanotube diameter.

Estimated cut-off frequency of a device:

$$f_T = \frac{g_m}{2\pi(C_i + C_{parasitic})} = \frac{0.12\mu S/\mu m \times 200\mu m}{2\pi(85nF/cm^2 \times 200\mu m \times 50\mu m + 330nF/cm^2 \times 200\mu m \times 12\mu m)} = 230KHz$$

where g_m is transconductance, C_i is gate capacitance, and $C_{parasitic}$ is source/drain-gate overlap capacitance respectively.

Supplementary Figures and Legends

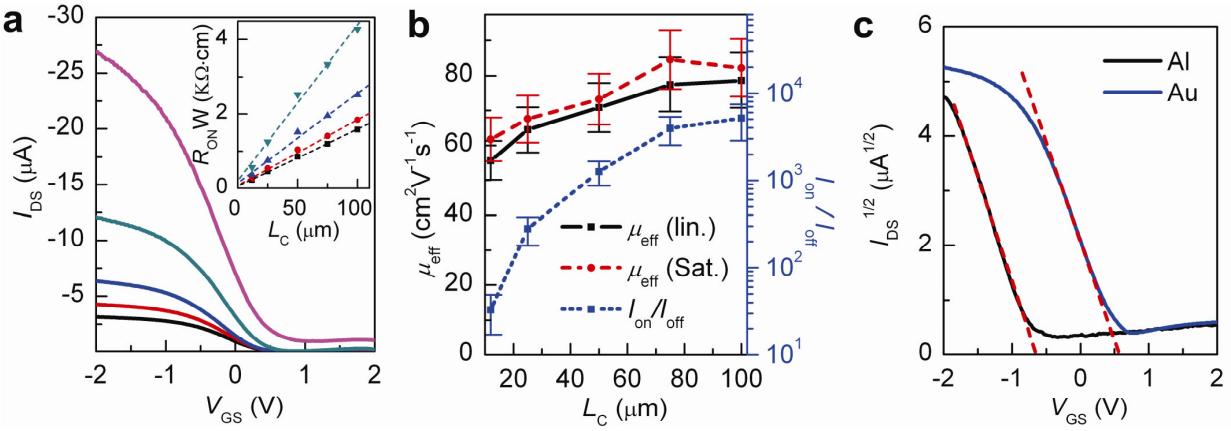

Figure S-1. **a**, I_{DS} - V_{GS} characteristics (V_{DS}: Drain-source voltage=-0.2 V) of devices with channel width (W) of 200 μm and channel lengths (L_C), from top to bottom, of 10 μm, 25 μm, 50 μm, 75 μm, and 100 μm. (I_{DS}: Drain-source current, V_{GS}: Gate-source voltage). Inset: Width-normalized ON resistance ($R_{ON}W$) under different V_{GS} as a function of L_C. The solid lines represent the linear least square fit of the data. **b**, Effective mobility (μ_{eff}), extracted from both linear region and saturation region, and device on/off ratio (I_{on}/I_{off}, measured with V_{DS} =-0.2 V) as a function of L_C. **c**, $I_{DS}^{1/2}$- V_{GS} characteristics (V_{DS} =-2 V) of a device with W of 200 μm and L_C of 100 μm. Dashed lines serves as visual guide to extract threshold voltage (V_T).

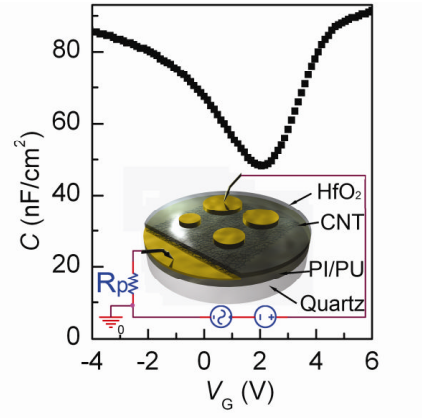

Figure S-2. Capacitance-voltage characteristics of a dish-shaped metal-insulator-semiconductor capacitor formed by gold, HfO_2, and SWNT network. Inset: Schematic of the capacitor array (CNT: Carbon nanotube, R_p: Parasitic resistance).

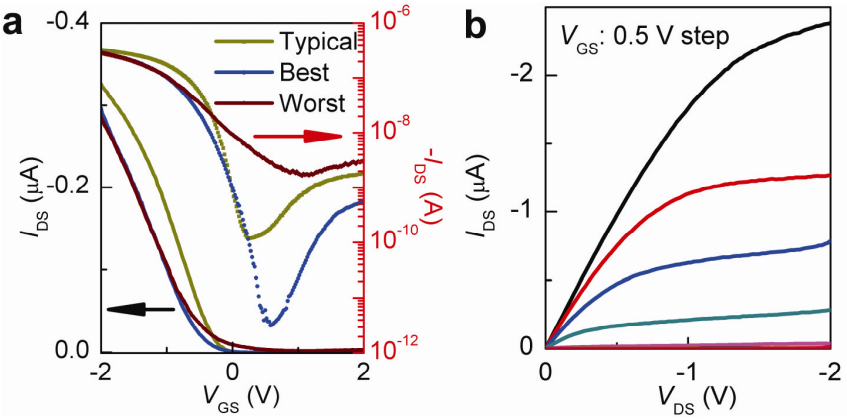

Figure S-3. I_{DS}-V_{GS} characteristics (V_{DS}: Drain-source voltage=-0.2 V) in both linear scale (left axis) and logarithmic scale (right axis) of three representative devices with typical (dark yellow), high (blue), and low (dark red) on/off ratios (**a**) and I_{DS} –V_{DS} characteristics (V_{GS}: Gate-source voltage changed from -2 V to 0 V) (**b**) of a top gate device with high on/off ratio. For all three devices, channel widths are 200 μm and channel lengths are 100 μm, with photolithographically defined 5 μm wide strips and source/drain electrodes patterned after transfer (I_{DS}: Drain-source current).

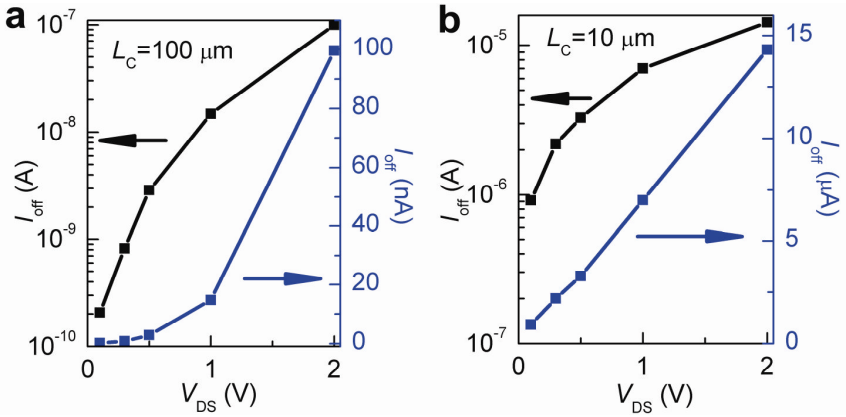

Figure S-4. Off state current (I_{off}) as a function of drain-source voltage (V_{DS}) for devices with channel length (L_C) of 100 μm (**a**) and 10 μm (**b**) respectively, shown in both linear scale (right axis) and logarithmic scale (left axis)

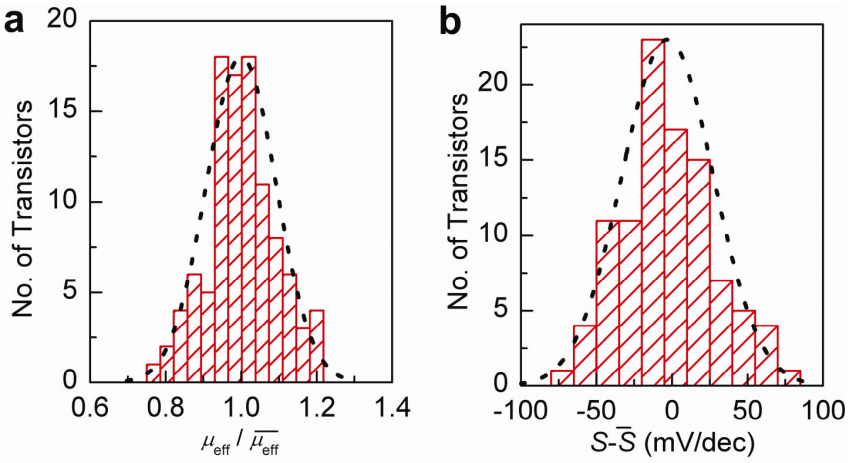

Figure S-5. Histograms of normalized effective mobilities (μ_{eff} / $\bar{\mu}_{eff}$) (**a**) and subthreshold swing variations ($S-\bar{S}$) (**b**) determined from measurements of over 100 SWNT transistors. (The bars over the quantities μ_{eff} and S refer to average values. The dotted lines represent Gaussian fits to the data.)

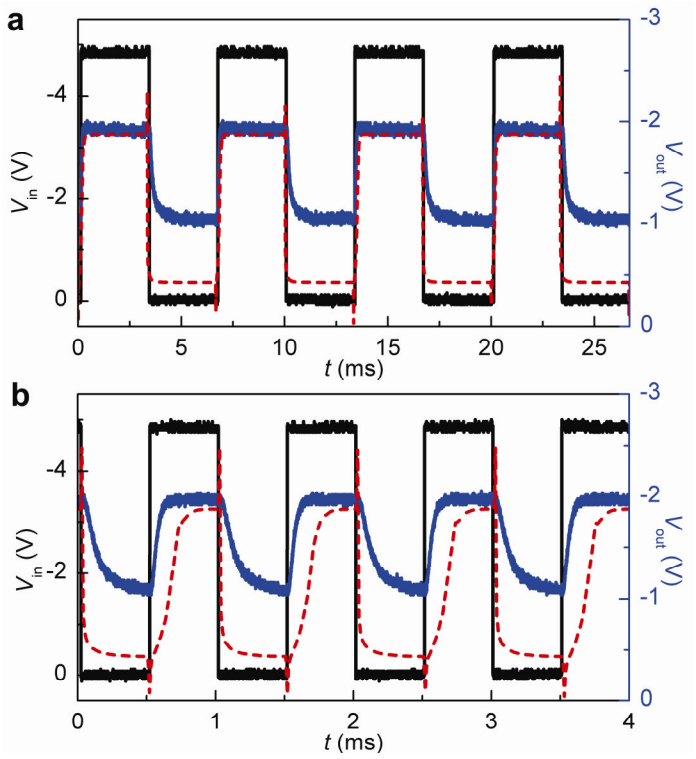

Figure S-6. Dynamic switching characteristics of the four-bit decoder. The data show the measured (blue) and simulated (red dashed) output voltage of the least significant bit of the No. 7 output line, and the square wave input pulse (black), at clock frequency of 150 Hz (**a**) and 1 kHz (**b**), and constant bias from other input lines.

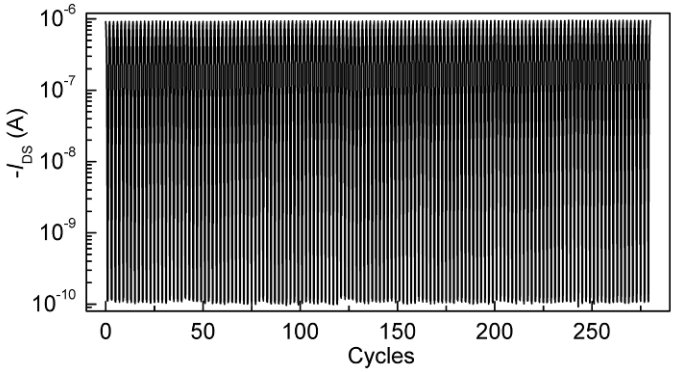

Figure S-7., Drain-source current (I_{DS}) of a typical SWNT thin-film transistor modulated by a triangle waveform (-2 V to 0 V) applied to the gate with a constant drain-source bias (-0.2 V), showing the operational stability of SWNT devices in air.

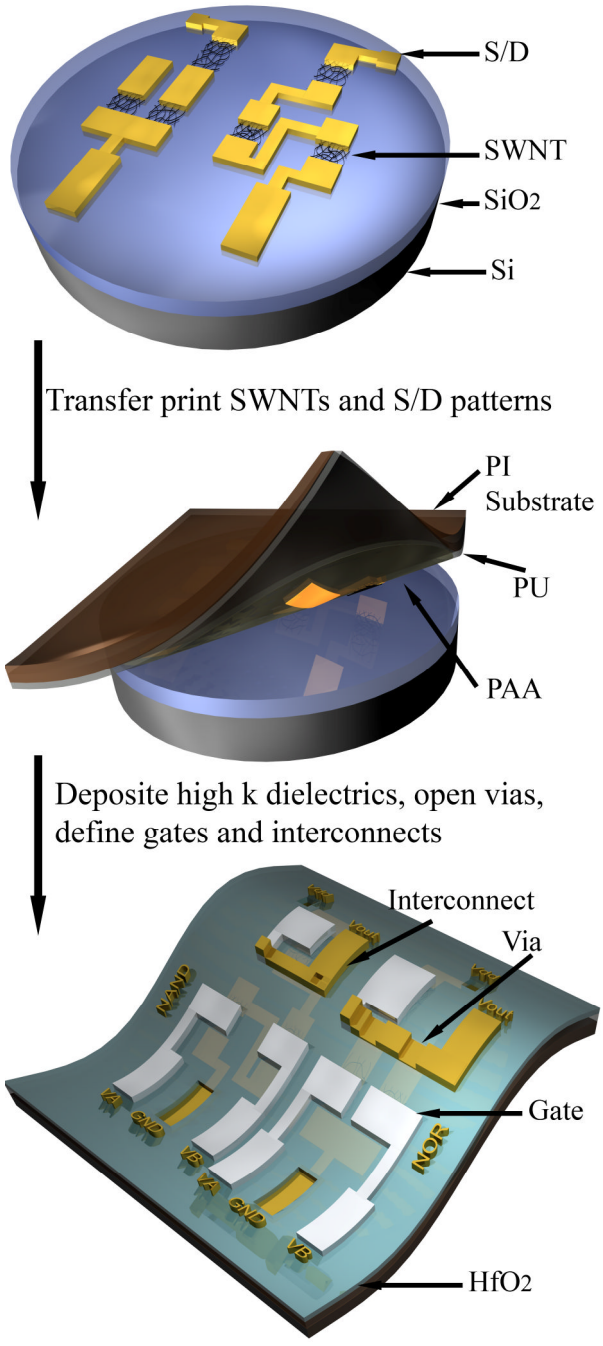

Figure S-8. Schematic illustration of the process for fabricating circuits on plastics with transfer-printed single-walled carbon nanotube (SWNT) networks (S/D: Source/Drain electrodes, PI: Polyimide, PU: Polyurethane, PAA: Polyamic acid).

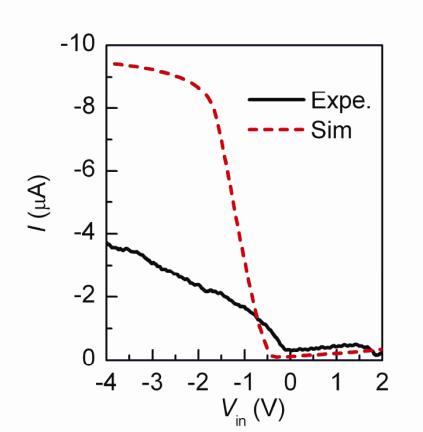

Figure S-9. Measured (solid line) and simulated (dashed line) dependence of inverter current load (I) on input voltage (V_{in}).

Supplementary Tables

Table S-1. Fitted SPICE Model Parameters.

Component	Parameter	Value
Voltage Controlled Current Source	$V_{threshold}$	-4 V
	α	0.45
	β	3
	K_N	10^{-9}
	V_{G0}	1 V
p-FET	λ	0.1
	V_T	-0.4 V
	K_P	20 μA/V^2
	R_S	11 kΩ
	R_D	11 kΩ

Supplementary Notes

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