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FULL PAPER

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Printable Single-Crystal Silicon Micro/Nanoscale Ribbons, Platelets and Bars Generated from Bulk Wafers**

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This article demonstrates a method for fabricating high quality single-crystal silicon ribbons, platelets and bars with dimensions between ~100 nm and ~5 cm from bulk (111) wafers by using phase shift and amplitude photolithographic methods in conjunction with anisotropic chemical etching procedures. This "top-down" approach affords excellent control over the thicknesses, lengths, and widths of these structures and yields almost defect-free, monodisperse elements with well defined doping levels, surface morphologies and crystalline orientations. Dry transfer printing these elements from the source wafers to target substrates by use of soft, elastomeric stamps enables high yield integration onto wafers, glass plates, plastic sheets, rubber slabs or other surfaces. As one application example, bottom gate thin-film transistors that use aligned arrays of ribbons as the channel material exhibit good electrical properties, with mobilites as high as ~200 $cm^2 V^{-1} s^{-1}$ and on/off ratios > 10^4.

1. Introduction

Printable or solution processable semiconductor materials have attracted significant attention recently due to their potential to enable cost effective, non-vacuum based fabrication approaches for large area electronics, often referred to as macroelectronics, and particularly to systems that use low cost plastic substrates.[1] Several classes of semiconducting small molecule and polymer materials have been demonstrated as active layers in thin film electronics for displays, sensors and other devices on plastic substrates.[2] While these organic semiconducting materials have some promise for these and other applications such as radio frequency identification tags, the moderate device performance and uncertain reliability represent challenges, especially for demanding applications. An emerging direction for research in this field focuses on the possibility of replacing these organic semiconductors with inorganic materials in various forms, ranging from low temperature or laser annealed polycrystalline thin films, to single crystal semiconductor wires or ribbons.

Two different methods can be used to create the wires/ribbons. The first, known as a bottom-up approach, uses direct chemical synthesis[3] of these elements from vapor or liquid phase molecular precursors with or without the use of size selected catalysts. The second, known as a top-down approach, uses specialized lithographic and etching procedures to create the wires/ribbons from bulk wafers or wafers with thin film stacks on their surfaces. The bottom-up approaches can create an impressive variety of structures, including nanoribbons,[4–12] nanomembranes,[13–23] nanowires,[24–28] and multicomponent heterostructured nanoelements.[29–32] These objects can be used individually or collectively as active layers for high-perfor-

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mance transistors, light-emitting diodes and other devices.[25,28,31] Two main challenges exist with the bottom up approach. First, tight control of the dimensions and dimensional uniformity, the doping levels, the crystallographic orientations and the materials purity can be difficult. Second, producing organized arrays of these elements, in configurations that are suitable for scalable integration over large areas into macroelectronic systems, can be challenging.

The top-down approaches overcome this second difficulty by exploiting transfer printing techniques that retain the geometrical order of the elements as defined by the lithographic steps. Also, they offer excellent control over the dimensions, crystallinity and doping levels of the micro/nanostructured elements and can be applied to any of the wide range of materials that are available, in many cases as commodity items, in wafer scale sources, including Si, SiGe, bi-layered Si/SiGe, GaAs, GaN, and others.[13,16,19,21–23,32–41] Recent reports demonstrate that various types of field effect transistors, diodes and other devices can be formed on polymeric substrates using micro/nanoribbons of these sorts of single crystal inorganic semiconductors. These systems show good electrical performance,[35–38,42] mechanical flexibility,[38,41] low cost[35,36] and, in certain structural forms, stretchability,[34] even in intrinsically brittle materials such as GaAs.[40]

The source of silicon material used for the "top-down" approach often consists of wafers that imbed sacrificial layers, such SiO_2 in silicon-on-insulator (SOI) structures.[37,38] This type of SOI wafer is useful because it provides a simple route to micro-/nano-structures of Si in which photolithographic patterning is followed with selective etching of the SiO_2. Although this method produces well-defined Si micro/nanostructures, the high-cost associated with SOI wafers makes the fabrication of large quantities of Si micro/nanostructures economically unattractive. Our recent work introduced a method to generate micro/nanoscale ribbons with geometries (thicknesses and widths of ~200 nm and ~10 μm, respectively) similar to those that can be produced from SOI wafers, but using low cost bulk silicon wafers as the source material.[35,36] The present paper extends this initial work in several important ways. First, it provides detailed studies of the materials aspects of the processing and introduces optimized etching chemistries that increase substantially the level of control over the dimensions and uniformity of the fabricated structures. Second, it shows the fabrication of ribbons via wet etching with Tetramethyl ammonium hydroxide (TMAH), which is compatible with integrated circuit processing. Third, it exploits these new approaches to fabricate not only ribbons, but also thick (up to 50 μm) bars and wide (up to 100 μm) platelets, whose geometries can be useful for solar cell and sensor applications, respectively. Fourth, it demonstrates the printing of these elements, in a selective manner with an automated tool, over large areas. Fifth, it shows that nanoribbons formed in this manner can be structured into 'wavy' geometries on elastomeric substrates, as a bulk wafer alternative to the SOI based stretchable electronics reported recently.[34] Sixth, it illustrates the fabrication of silicon microphotodiodes generated from thick silicon bars. Collectively, these results might be important for future macroelectronics systems and other devices that require large-area, high-performance and low-cost semiconducting materials.

2. Results and Discussion

2.1. Fabrication of Silicon Ribbons

Figure 1 schematically illustrates processing steps for generating Si micro/nanostructures from a bulk wafer. The first step uses phase shift and traditional photolithography to define lines of photoresist (PR) aligned perpendicular to the <1$\bar{1}$0> direction on the surface of a silicon (111) wafer, as shown in Figure 1a. Evaporating Ti/Au (3 nm/30 nm) on this pattern of

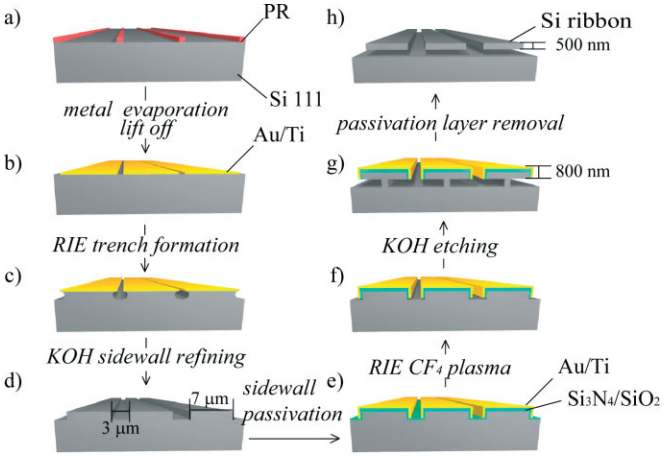

Figure 1. Schematic illustration of steps for generating Si ribbons from a bulk silicon (111) wafer, including a) defining thin photoresist lines on a Silicon (111) wafer by near field phase shift lithography; b) evaporating Ti/Au (3 nm/30 nm) and subsequent liftoff to define trenches; c) isotropic reactive ion etching the Si using the Ti/Au as an etch mask; d) etching the resulting trenches with an KOH/IPA solution to generate square sidewalls and a smooth base; e) passivating these sidewalls using 60 nm SiO_2/270 nm PECVD silicon nitride and angled evaporated Ti/Au (3 nm/30 nm); f) removing the exposed SiO_2/silicon nitride by reactive ion etching; g) anisotropic etching of unprotected silicon with KOH; h) continued etching of unprotected silicon to generate free standing silicon ribbons.

PR and then removing the PR with acetone produces a metal mask for dry etching (Fig. 1b). Isotropic reactive ion etching (RIE; etch gas: SF_6) of the exposed silicon produces trenches with rounded cross sectional profiles, as shown in Figure 1c. Etching these trenches in KOH/Isopropyl alcohol (IPA), according to details presented in the following section, transforms the rough, rounded trenches into grooves with perfectly rectangular cross sections and smooth surfaces, with dimensions that can be controlled accurately (Fig. 1d). This refining procedure represents an advance over previously described approaches, and is critically important to produce smooth surface morphologies and with dimensions that can be selected over a wide range (from ~100 nm to ~100 mm). The next step involves growing thermal oxide (60 nm) on the silicon and depositing a conformal coating of Si_3N_4 (thickness = 270 nm) via

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plasma enhanced chemical vapor deposition (PECVD) to protect the sidewalls of the rectangular grooves. Angled electron beam evaporation (75° from the normal axis of a wafer) of Ti/Au (3 nm/30 nm) with a collimated flux forms an etch mask on the sidewalls (Fig. 1e) but leaves the SiO_2/Si_3N_4 on the floors of these grooves exposed. RIE with a CF_4 plasma removes this exposed SiO_2/Si_3N_4 (Fig. 1f). Anisotropic etching in KOH creates an etch front that proceeds along the Si <110> directions, beginning on one side of the trench and continuing in the lateral direction until the etch fronts meet (Fig. 1f). Further etching the unprotected silicon produces freestanding single-crystal silicon ribbons (Fig. 1h), bars or platelets, depending on the parameters associated with the photolithographic and other processing steps.

The fabrication approaches of Figure 1 create silicon structures in well defined arrays with uniform geometries. Dry transfer printing can lift these structures from the wafer, retaining the lithographically defined order, provided that they are designed with sacrificial breakaway 'anchors' that keep them tethered to the wafer after complete undercut etching. As illustrated in this paper, the printing can be done in a selective manner from specific areas of the wafer. Figure 2 presents a schematic representation of this process, as operated in a mode that expands the areal coverage of the silicon and a chemical method that regenerates the surface of the silicon to prepare it for the fabrication of additional printable structures. The printing is performed with a home-built mechanical three-axis stage controller and a poly(dimethylsiloxane) (PDMS) stamp with a

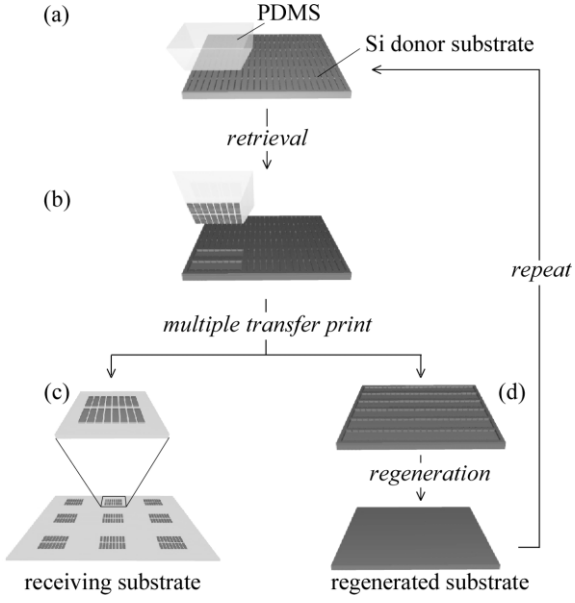

Figure 2. Schematic illustration of the process for transfer printing silicon ribbons onto desired substrates and for regenerating the surface of the source wafer: a) conformal contact of a PDMS transfer element with the top surface of selected regions on a source wafer that supports an array of silicon ribbons attached to the wafer at their ends; b) removal of the stamp and lift off of a fraction of the ribbons from the wafer; c) repeated transferring of silicon ribbons onto various substrates; d) anisotropic wet chemical etching (e.g., KOH) of the wafer to regenerate its surface for the production of another set of silicon ribbons.

fabricated relief structure (i.e., 2×2 array of square relief structures with lateral dimensions of ~ 0.5 mm $\times$ 0.5 mm) formed using the techniques of soft lithography. In contrast to our previous work,[43] this printing system provides an automated way to transfer the silicon with high throughput, and excellent control over registration and positioning (to within ~ 1 μm). The three-axis mechanical stage is under both precise position control and force control. A motion program places the PDMS in conformal contact with the top surface of a portion of the silicon ribbon array. PDMS stamps were inked with silicon ribbons, bars or platelets via Van der Waals interactions between the PDMS and the Si. Removing the PDMS stamp from the donor substrate quickly leads to efficient transfer of the structures from the wafer to the stamp (Fig. 2b).[44] Next, the stage places the PDMS stamp in contact with the surface of the target substrate and removes it slowly, leaving the silicon ribbons on the substrate. Repeating this process can fill a large area substrate with silicon in desired locations. After depleting the source wafer of silicon elements, the substrate can also be recycled by mechanically and/or chemically polishing the surface of the wafer with a 40 wt % KOH solution heated to a 120 °C for 15 min. The anisotropic wet chemical etching of donor substrate produces a flat surface on the silicon wafer suitable for the production of additional silicon structures. This process can be repeated multiple times to consume the thickness of the wafer.

Figure 3 shows scanning electron microscopy (SEM) images of the structures at different steps of the fabrication sequence illustrated in Figure 1. In the initial step, phase-shift photolithography (see Experimental Sec.) using a PDMS phase mask produces narrow PR lines with thicknesses and widths of 400 and 200 nm (Fig. 3a), respectively. Metal deposition and liftoff create a metal masking layer (Fig. 3b). Next, RIE etching the exposed silicon area with SF_6 produces nearly isotropic profiles (Fig. 3c). This step forms trenches with round-shaped sidewalls and rough surfaces that can lead to local defects, thickness variations and other unwanted features in the silicon structures. These issues are avoided by use of the anisotropic refining step that transforms the non-ideal cross sections of the trenches to perfect, rectangular shapes. The KOH used for this step removes silicon along {110} planes much faster, by up to several hundred times, than along the {111} planes. The origin of this difference in etching rate rests in the lower density of atoms and higher density of dangling bonds on the {110} planes than the {111} planes.[45–47] In particular, the trench and sidewall regions are composed of Si $(1\bar{1}0)$ and higher index crystal etching planes. From the SEM images in Figure 3 it is apparent that the higher index planes etch faster in the KOH than the Si $(1\bar{1}0)$, leaving the Si $(1\bar{1}0)$ exposed after the sidewall refining step. The resulting profiles are rectangular due to the 90° orientation of the silicon $(1\bar{1}0)$ sidewalls relative to the Si (111) floors. Figure 3d shows that refining with a KOH/IPA solution creates mesas with straight ($\sim 90°$ with respect to the wafer surface) and smooth sidewalls and trench floors with an average roughness of 0.45 nm as estimated by atomic force microscopy (AFM) measurements (500 nm $\times$ 500 nm measurement area). Figure 3e shows the sidewall bilayer resist. The thin SiO_2 layer

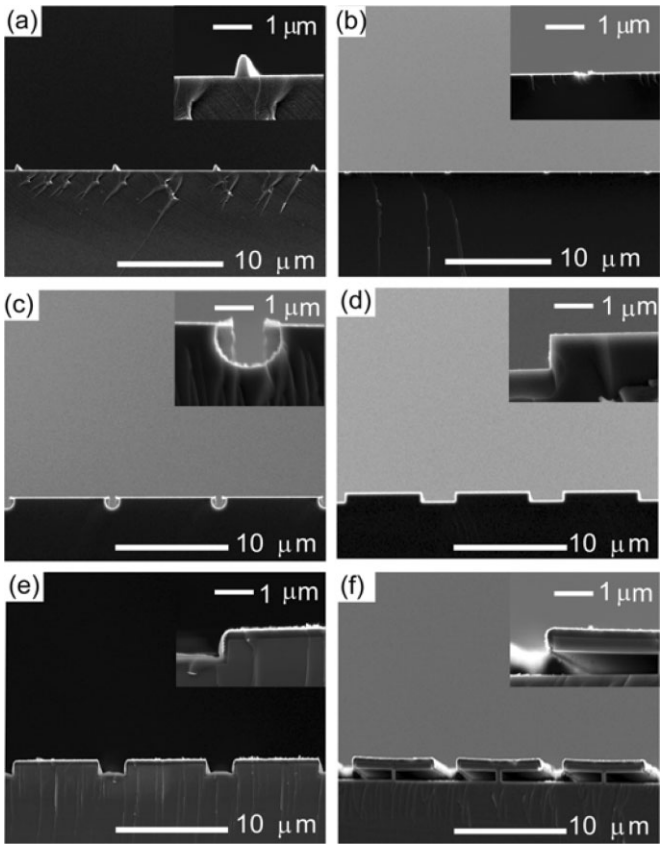

Figure 3. Scanning electron microscopy (SEM) images showing the geometries of the structures formed at different steps of the fabrication process: a) defining thin photoresist lines on a Silicon (111) wafer by near field phase shift lithography; b) evaporating Ti/Au (3 nm/30 nm) and subsequent liftoff to define trenches; c) isotropic reactive ion etching the Si using the Ti/Au as an etch mask; d) etching the resulting trenches with an KOH/IPA solution to generate square sidewalls and a smooth base; e) passivating these sidewalls using 60 nm SiO_2/270 nm Si_3N_4 and angled evaporated Ti/Au (3 nm/30 nm); f) removing the exposed SiO_2/Si_3N_4 by reactive ion etching followed by anisotropic etching of unprotected silicon with KOH. The insets in the SEM images are higher magnification views of the structures formed in the corresponding steps.

promotes adhesion of the Si_3N_4, leading to conformal step coverage on the silicon mesa surface as depicted in the inset of Figure 3e. Angled evaporation of Ti/Au at 75° from the surface normal, followed by removal of the exposed bilayer by RIE (Fig. 3e) reveals Si $(1\bar{1}0)$ planes for horizontal etching using a KOH solution. This etching produces silicon ribbons anchored at their ends to the wafer (Fig. 3f). The etch front continues until the silicon microstructures are released. At the ends of the ribbons, the etching terminates where Si (111) planes intersect, to produce triangular regions near the anchor points. The ribbons can be designed (i.e., sufficiently small ratios of their lengths and widths to the gap between their bottom surfaces and the top surfaces of the wafer) such that there is a stable, air gap between them and the wafer along, at least partially, along their lengths to avoid stiction. The largest and smallest features sizes that we attempted to fabricate using the approach outlined in Figure 1 were 20 μm thick, 60 mm long and 100 μm wide and 87 nm thick, 185 μm long and 5 μm wide, respectively. The maximum lengths and thicknesses are limited by the size of the wafer. The minimum widths and lengths are limited by the lithography. The minimum thicknesses and maximum widths depend on the edge roughness and robustness of the etch masks, respectively.

Figure 3f highlights the parallel orientation of the ribbon width (etch front) with respect to the surface floor. The dimensions of these ribbons can be controlled by the geometries of the patterns of photoresist, the depth of the RIE trench, the angle of the angled evaporation, and the extent of anisotropic etching. The optimized procedures introduced here enable the thicknesses and the widths of the structures to be selected over a very wide range, and enable not only ribbon geometries but also bars, where the thicknesses are in the range of several microns, and platelets or sheets, where the widths are up to 100 μm.

2.2. Anisotropic Etchant/Additives Study and Surface Morphology

Surface roughness is important to the mechanical and electrical performance of devices made from these silicon structures. The etchants not only influence this roughness, but their chemistry is also important to consider for subsequent device integration. For example, K^+ ions are known to diffuse into insulating films and can alter, in undesired ways, sensitive components (i.e., dielectric layers in transistors) of electronic devices.[48] Also, these ions in silicon dioxide films are mobile under an applied electrical field which can lead to shifts in the threshold voltage and hysteresis[49] in transistors that use such contaminated oxides for gate dielectrics. Silicon wet etching can be accomplished with organic and inorganic aqueous solutions. Organic systems include Tetramethyl ammonium hydroxide (TMAH), ethylenediamine-pyrocatechol (EDP), and hydrazine. The inorganic solutions consist of aqueous hydroxides of potassium, sodium, cesium, lithium and ammonium. Both EDP and hydrazine are toxic and hydrazine is also explosive. The organic etchant TMAH is popular because it is compatible with integrated circuit processing, it is easy to handle and store, it produces smooth etched surfaces, and it can operate at high temperatures.[50] One possible disadvantage of TMAH is its relatively high cost compared to most inorganic wet etchants. KOH is the most popular inorganic etchant with features such as low toxicity and cost, and a high degree of etch selectivity for the Si (110)/(111) crystal planes.[50] KOH is, however, generally avoided for integrated circuit applications due to contamination introduced by the potassium. For both kind of etchants, additives such as IPA (for KOH[51–53] and TMAH[54,55]) can significantly alter the etch rate selectivity and etched surface morphologies, even though they are typically not involved directly in the etching reactions themselves.[51,52]

We examined carefully the behavior of KOH and TMAH etchants for the procedures of Figure 1. The mechanism for the etching of Si (111) planes with TMAH is different than that with KOH. The etching rate of the Si (111) plane is much higher, specifically by a factor of two, in TMAH than in KOH un-

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der similar experimental conditions.[56] These differences have the potential to lead to different morphologies. Figure 4 presents AFM images of the bottom surfaces silicon ribbons formed using different anisotropic etching solutions and the procedures of Figure 1. Figure 4 shows cases corresponding to 35 % KOH (Fig. 4a), 35 % KOH/IPA (Fig. 4b), 25 % TMAH (Fig. 4c), and 25 % TMAH/IPA (Fig. 4d). Each sample was so-

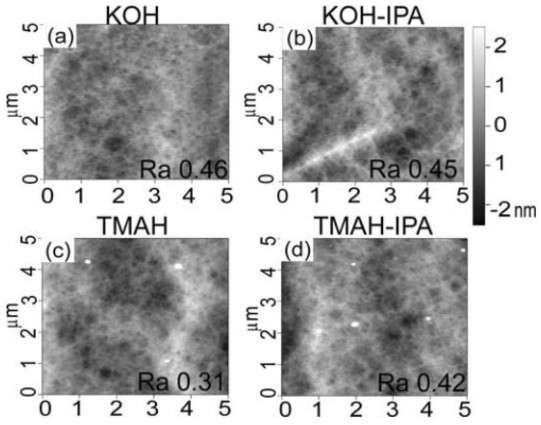

Figure 4. Atomic force microscopy images of the bottom surface of a single silicon ribbon undercut in different anisotropic etchants and additives: a) 5 μm × 5 μm image of a single silicon ribbon undercut in 35 % KOH etching solution, b) undercut in 35 % KOH/IPA, c) undercut in 25 % TMAH, d) undercut in 25 % TMAH/IPA. Average surface roughness values are depicted in each image.

nicated in concentrated hydrochloric acid prior to retrieval and subsequently dipped in HF (10 s) to remove KOH induced particle precipitation.[57] The average surface roughness (*Ra*) for each case was determined from 3 μm × 3 μm areas. The results show that TMAH and KOH/IPA yield smooth surfaces (*Ra* = 0.31 nm and 0.45 nm, respectively) with no systematic differences. As a result of its other features TMAH might represent the etchant of choice for structures that are to be incorporated as active thin films in electronic circuits.

2.3. Controlling Silicon Ribbon Dimensions

One of the simplest methods to control the thickness involves controlling the time for anisotropic KOH etching of the structures in Figure 3f. Figure 5 shows optical micrographs of arrays ribbons with average thicknesses of 365 nm, 306 nm, and 141 nm, as determined by AFM. The darker lines in Figure 5b and c are silicon nitride. This layer prevents unwanted contamination of the silicon by the PDMS during contact involved in transfer printing.[39] Also, it can be incorporated directly into devices. The color variations in the optical images result from slight thickness differences among the ribbons, and can be partially attributed to inhomogeneities in the etch (unstirred) bath.[58] A thickness variation of as small as ~8 nm (Fig. 5c) can cause striking variations in color. These colors vary smoothly along a given silicon ribbon, which suggests a minimal degree of short range thickness variation. The thick-

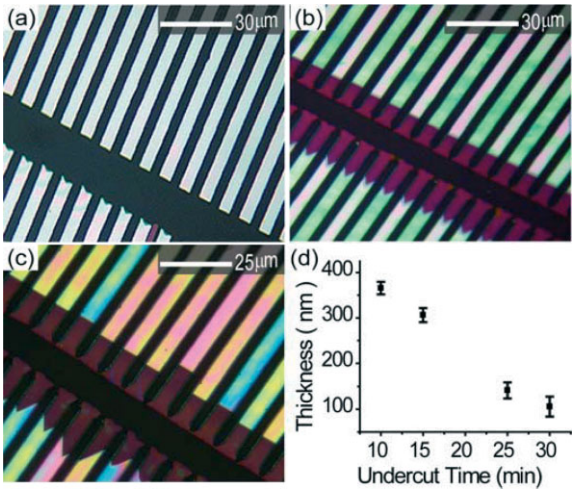

Figure 5. Optical micrographs of arrays of silicon ribbons of different thicknesses on a PDMS stamp: a) 365 nm, b) 306 nm, c) 141 nm, respectively. The color variation in the optical images is a result of the thickness differences. d) Plot of the average thickness of silicon ribbons as a function of the KOH etching time.

ness of the silicon ribbons varies due to relief that appears on the bottom surfaces of the ribbons due to etching. The top surfaces remain flat, due to protection from the anisotropic etchant via a metal/bilayer mask. The conformal contact between the PDMS stamps and the ribbons during the retrieval (i.e., 'inking') step is not affected by such variations. Further generations of ribbons can have surface roughness, but this roughness does not prevent conformal contact with the PDMS stamps provided that the amplitude of the roughness is comparable to or smaller than its characteristic spatial wavelengths.

Figure 5d shows a plot of the thickness as a function of KOH etching time. The thinnest ribbons that could be fabricated reliably in this manner had thicknesses of (87 ± 10) nm. Further etching tended to produce significant defects, predominantly at the edges of the ribbons. Thin-film transistors formed using these ribbons as the active channels showed mobilities that tended to decrease with decreasing ribbon thickness (i.e., etching time). This behavior can be partially attributed to an increase in the degree of surface roughness with decreasing ribbon thickness.

The main limitations of this approach are related to (i) KOH etching at the interface between the SiO_2/Si_3N_4 and the silicon and (ii) the finite degree of anisotropy of the KOH etchant. Employing a different anisotropic etchant, such as Tetramethyl ammonium hydroxide (TMAH), may enable thinner ribbons due to its higher etching selectivity towards silicon versus silicon nitride and its higher etching rate for the Si (111) planes.[50,56]

A different means to control the thickness uses the SF_6 plasma etch step to define different depths for the trenches in Figure 1c. Figure 6a shows ribbons with thicknesses of (944 ± 5) nm generated in this manner and printed onto a SiO_2 coated silicon wafer. The thickness variation across a group of ribbons (i.e., 12 mm × 14 mm array) was ±7 nm. Even thicker

ribbons, which have geometries more similar to bars, can be generated by replacing the SF_6 etch with inductively coupled plasma reactive ion etching (ICPRIE). Figure 6b shows a scanning electron micrograph of ~10.7 μm thick silicon bars generated using ICPRIE for the trenches and a 60° angle evaporation. The ribbons were detached from the mother wafer and transfer printed onto a Kapton plastic sheet (25 μm thick) coated with a 135 nm thick epoxy adhesive layer. The ribbons were placed in contact with the epoxy layer and heated at 75 °C to enhance the bonding. Peeling back the PMDS stamp left the ribbons attached to the target substrate. The inset presents a high resolution SEM of the structures. By suitable choice of the conditions for ICPRIE and angle of evaporation, it is possible to produce even thicker ribbons (i.e., greater than 20 μm) using this approach.

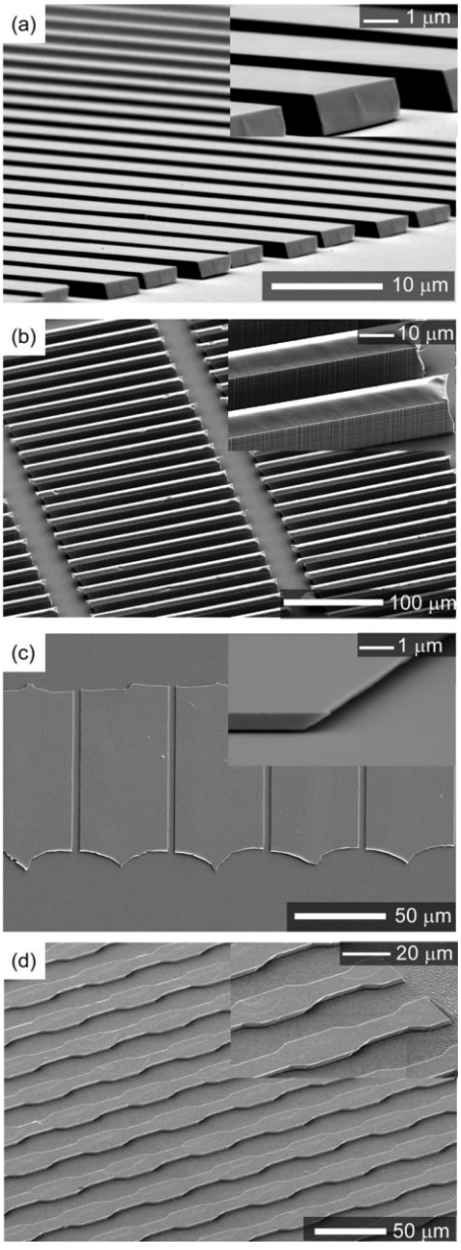

Figure 6. a) SEM images of ~1 μm thick silicon ribbons transfer printed without adhesives onto a SiO_2 coated silicon wafer. b) SEM image of the top surface of 10.7 μm thick silicon ribbons transfer printed onto Kapton (i.e., 25 μm thick) coated with a 135 nm epoxy adhesive. c) SEM image of 0.5 μm thick silicon platelets printed onto an epoxy coated silicon wafer. d) SEM of silicon ribbons fabricated with a controlled variations in width. The insets in all cases provide magnified views.

The widths of the ribbons can be controlled through the phase shift lithography step in Figure 1a. Very wide ribbons, in geometries that resemble two dimensional planar sheets, can be formed. Figure 6c shows ~48 μm wide, ~185 μm long and ~500 nm thick platelets transfer printed onto a 135 nm thick epoxy adhesive layer on a silicon wafer. The undercut etching step in this case required 30 minutes, which corresponds to an etch rate along the Si (110) planes of 1.6 μm min^{-1} using our KOH recipe. Moreover, AFM and SEM measurements indicate an anisotropic selectivity ratio for Si (110)/(111) = 130 which suggests a 0.18 μm thickness variation across 48 μm silicon sheets. These platelets, like the ribbons and bars, have smooth surfaces. In addition to these wide structures, it is possible to produce ribbons and platelets that have widths that vary along their lengths. As an example, Figure 6d shows an SEM image of structures with two distinct widths ($W_1 \simeq 7$ μm, $W_2 \simeq 14$ μm, length ≃ 185 μm, thickness ≃ 2.5 μm) but with uniform thickness of ~2.5 μm.

Finally, the lengths of the structures can be controlled by the amplitude and/or phase shift lithography steps. Figure 7 shows ribbons that have lengths of up to 6 cm, attached at their ends to the source wafer. The ribbons can bend and also stack together due to capillary forces during drying. The fabrication process should allow for the generation of ribbons even longer than those shown in Figure 7, limited only by the size of the wafer. These results collectively illuminate the motivation behind studying details of the materials and etching chemistries of our previous methodologies.[35,36] In particular, improvements in understanding lead to processing modifications that enable the fabrication of new silicon geometries and morphologies, thereby opening up new application possibilities in solar technology and imaging, as outlined subsequently.

2.4. Stretchable Silicon Ribbons

As the images indicate, the ribbon structures described previously are flexible (i.e., bendable). In their as-fabricated state, however, they are not stretchable. One route to achieve stretchability involves structuring ribbons into sinusoidal 'wavy' shapes,[34] by bonding them to prestrained elastomeric substrates, such that they respond to applied strains in a manner that is similar to an accordion bellows. We show here that silicon ribbons generated using the procedures of Figure 1 can, like the SOI derived ribbons previously reported, can be formed into these stretchable, 'wavy' shapes. Generating 'wavy' silicon with ribbons formed according to previously reported procedures[35,36] is challenging due to thickness variations associated with the structures. The procedures introduced here eliminate these nonideal aspects. In particular, the smooth surfaces and edges of ribbons generated by the refining step,

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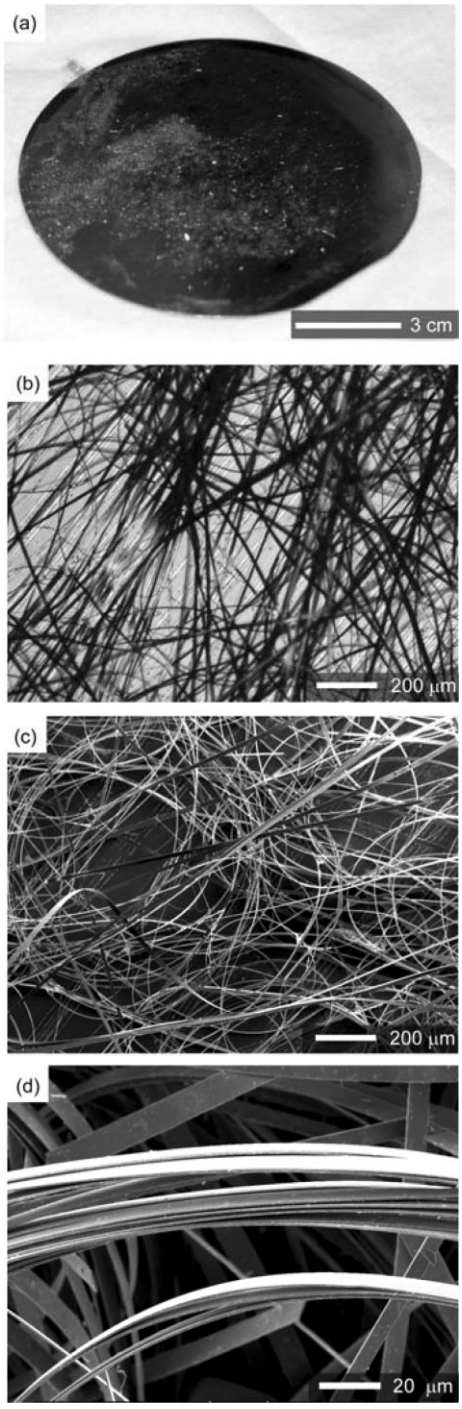

Figure 7. a) Optical image of ultralong (up to 6 cm) silicon ribbons with one of their ends attached to the silicon source wafer b) Optical micrograph of the ribbons. c) SEM of the ribbons, d) High resolution SEM of the ribbons.

and the resulting uniformity in the structure thicknesses, are critically important.

The process for generating wavy silicon ribbons from bulk wafers began with the procedures of Figure 1, where we selected lengths, widths and thicknesses of 1 mm, 7 μm and 530 nm, respectively. An untreated PDMS slab lifted these silicon ribbons off of the wafer. The ribbons were then printed onto prestrained PDMS substrates previously treated with UVO,[59–61] such that strong –O–Si–O– bonding occurs with the native oxide of the silicon. The UVO treated PDMS has $-O_nSi(OH)_{4-n}$ chemical moieties on its surface[62] that can bond irreversibly with other materials, particularly those with exposed -OH groups.[63]

This dual transfer process that placed the undercut etched surface of the silicon ribbons in contact with the PDMS to demonstrate the ability to bond to this etched surface. Relaxing the prestrain yields wavy silicon ribbons, as illustrated in Figure 8a. The inset shows a high magnification view of the top portion of the wave trough. The images show well defined wavy shapes with wavelengths of 73 μm, which is within 13 % of theoretical predictions[34] summarized by

$$\lambda_0 = \frac{\pi h}{\sqrt{\varepsilon_c}}, \quad A_0 = h\sqrt{\frac{\varepsilon_{pre}}{\varepsilon_c - 1}} \tag{1}$$

where $\varepsilon_c = 0.52\left[\sqrt{\frac{E_{PDMS}\,(1-\nu_{Si}^2)}{E_{Si}\,(1-\nu_{PDMS}^2)}}\right]^{2/3}$ is the critical strain for buckling, ε_{pre} is the degree of prestrain, λ_0 and A_0 are defined as the wavelength and amplitude respectively. The thickness of the silicon ribbon structures is h, ν is the Poisson ratio and E is equal to the Young's modulus of Si and PDMS. The following values were used to yield the calcualted value of it (i.e., 84 μm): $E_{Si} = 160$ GPa, $E_{PDMS} = 2$ MPa, $\nu_{PDMS} = 0.48$, $\nu_{Si} = 0.27$. The distances between adjacent ribbons are sufficiently small in this case, that mechanical coupling leads to uniform phases. Figure 8b shows the behavior of these wavy ribbons at different applied strains. Ribbons cycled (i.e., compressed, relaxed and then stretched) multiple times showed no delamination or fracture, for strains ranging from –10 % to 10 %.

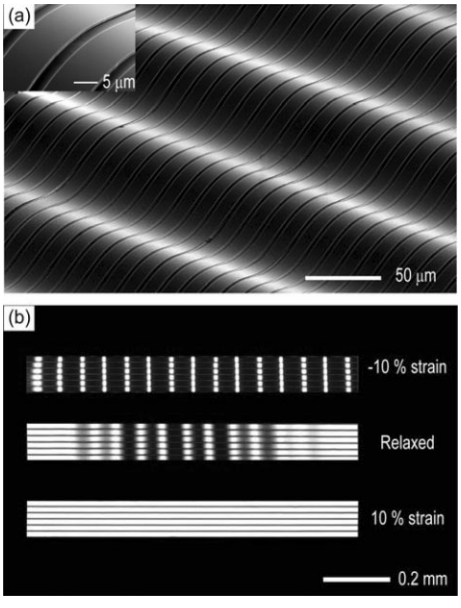

Figure 8. a) SEM image of wavy silicon ribbons on a PDMS substrate. The inset provides a magnified view. b) "Wavy" silicon ribbons under different applied strains.

2.5. Selective Area Transfer Printing of Silicon Ribbons

To demonstrate automated, selective transfer printing, we first fabricated a dense array of silicon ribbons on a piece of silicon with area 12 mm × 14 mm, according to steps in Figure 1, and then followed the steps in Figure 2 to print small patches (~0.5 mm × 0.5 mm) of ~900 nm thick ribbons from this wafer onto a 0.8 mm thick glass substrate with area 40 mm × 48 mm and coated with a 500 nm thick layer of PDMS to facilitate contact and transfer. The mechanistic details of the transfer from the PDMS stamp to a thin PDMS layer are under investigation. We suspect that the transfer is enabled by the ability of the thick stamps to deform easily in such a manner that facilitates the release of the ribbons upon peel back.

Figure 9a presents the result. The inset illustrates the piece of silicon from which the ribbons were generated after the printing process. Figure 9b shows an optical micrograph of an array of printed silicon ribbons. Each printing step exhibited efficiencies for transfer from the wafer to the stamp and then to the glass, of greater than 95 %. The slight variations in the patch size/shape are mainly a result of missing or extra ribbons. Missing ribbons were caused by dust or misalignment of the stamp features with the donor substrate. Extra ribbons resulted from this same kind of misalignment as well as unwanted mechanical sagging and contact of the stamp in its recessed regions. Close examination of Figure 9b shows, for example, some extra ribbons. Engineering improvements in the stamps, the printer and the processing environment can eliminate these sorts of defects. The overall procedures illustrated in these figures correspond to an increase, by more than a factor of 10×, in the areal coverage of the silicon, from the source wafer to the glass substrate. This type of capability to form large area, low coverages of silicon can be useful for systems such as backplane circuits for displays.

2.6. Large Area Printing of Multiple Silicon Ribbon Generations

The process of Figure 1 enables the generation of silicon structures on a full wafer scale. Repeated application of this fabrication process, to create multiple 'generations' of ribbons, is possible with a single wafer. A uniform etching step in KOH prepared the wafer surface for subsequent processing sequences. Figure 10a shows some examples of 1st, 2nd, and 3rd generations (G1, G2, and G3, respectively). The ribbon yields for G1, G2, and G3 were > 99 %, > 85 %, and > 75 %, respectively. The yield reductions in G2 and G3 silicon ribbons results from pattern defects that remain from one cycle to the next in the processing. Most important, however, is the residual roughness that remains after the KOH chemical polishing step. Combining this chemical approach with mechanical polishing can return the surface to its initial smooth state, to eliminate this source of defects.

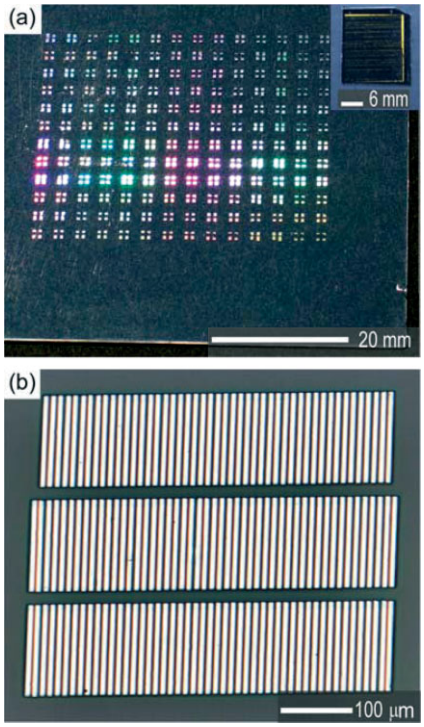

Figure 9. Selective area transfer printing of silicon ribbons; a) Optical image of a PDMS coated glass substrate with arrays of printed ribbons. The fabrication involved repeated transfer printing from a 12 mm × 14 mm donor (inset) onto a 40 mm × 48 mm piece of glass. The sample here demonstrates a greater than ten time increase in areal coverage of the silicon. b) High resolution optical micrograph of one array pattern of silicon ribbons.

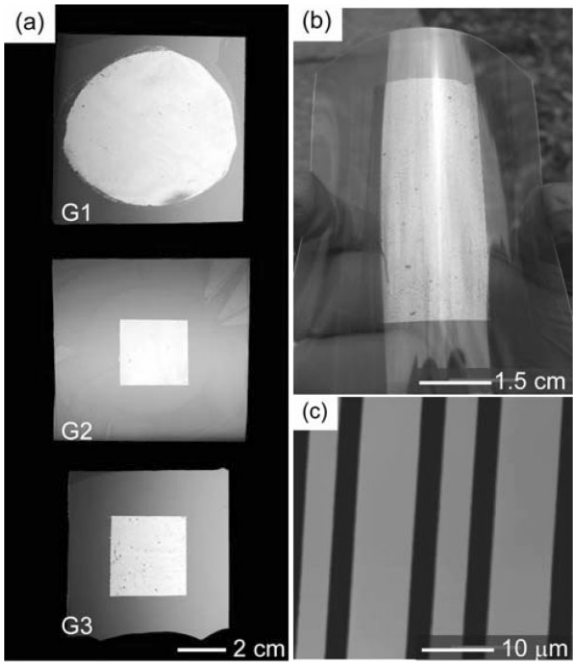

Figure 10. Large-area printing of silicon ribbons. a) Optical micrographs of silicon ribbons generated on refinished wafers and transferred to glass, using the KOH based regeneration method. After the production of ribbons on a wafer, the wafer is re-finished by this etching process, allowing the production of subsequent, "generations" of ribbons. 1st, 2nd, and 3rd ribbon generations are represented (G1, G2, and G3, respectively). b) Optical micrograph of G2 ribbons printed on a flexible PET plastic substrate. c) Large area AFM scan of G2 ribbons on a glass substrate.

ADVANCED FUNCTIONAL MATERIALS

Figure 10b shows optical micrograph of G2 ribbons printed onto a flexible poly(ethylene terephthalate) (PET) plastic substrate coated with a thin layer of PDMS (~450 nm) using a Meyer bar.[43] The substrate can be bent and flexed (>20 times to a radius of curvature of 7 mm) without delamination or cracking of the ribbons, as observed through an optical microscope. Figure 10c presents an AFM image of G2 ribbons on a silicon wafer coated with 500 nm of PDMS. An average surface roughness of the top surface for these ribbons was $Ra = 0.82$ nm. AFM images of G3 ribbons showed comparable smoothness.

2.7. Thin Film Transistors and Microphotodiodes on Plastic Substrates

To evaluate the utility of the silicon structures in electronics, we built bottom gate thin film transistors using the G2 ribbons. The device layout was similar to our previously published results.[35] Briefly, a 400 nm thick film of Au formed a gate electrode on a thin Kapton film. A layer of SiO_2 (~80 nm) deposited via PECVD and a thin film of epoxy (SU-8, Microchem) served as a bilayer gate dielectric on top of this gate electrode. The total thickness of this bilayer was ~190 nm. The dielectric constants of the SiO_2 and epoxy are 3.9 and 4.0, respectively. The calculated total capacitance per unit area of the bilayer dielectric is 18.4 nF cm^{-2}.

Figure 11a shows the current–voltage response of a typical thin film transistor that incorporates these materials, measured at gate voltages ranging from –5 V to 10 V and source/drain voltages of 0 V to 5 V. The channel length and width of this device are 100 μm (fringing field currents are not important in these devices due to the natural isolation provided by the structure of the ribbons.). These devices exhibit n-type enhancement mode operation and a relatively small hysteresis (~1.5 V for sweep rates of ~1 Hz). Figure 11b shows representative full transfer characteristics of G2 ribbon devices. The threshold voltage was $V_{th} = 1.6$ V, the per ribbon mobility was ~207 cm^2 V^{-1} s^{-1} (fill factor 70%) and the ON/OFF ratio was >10^4. These per ribbon mobilities are somewhat lower than those of similar devices fabricated using SOI derived ribbons. The large number of interface trap sites between the PECVD oxide and Si (111) crystal planes, and the roughness of the ribbons might contribute to this reduction.[35,64,65] Also, the dependence of silicon crystal orientation on field effect mobility for electrons has been previously reported for single crystal silicon[66] and more recently for thin film transistors that incorporate laser annealed polysilicon as the active material.[67] From these reports the difference in mobilites for single and poly crystalline transistors that use Si (100) versus Si (111) textured thin films can be as high as 100–150 cm^2 V^{-1} s^{-1}. Previously, we reported transistors that use Si (100) active layers in similar device layouts that show device mobilities of ~260 cm^2 V^{-1} s^{-1} in the linear regime.[38] From a series of G2 devices we determined the average effective device mobility in the linear regime to be (122±17) cm^2 V^{-1} s^{-1}. The previous reports of the effect of crystal texture on electron mobility[66,67] are in general agreement with our data presented here.

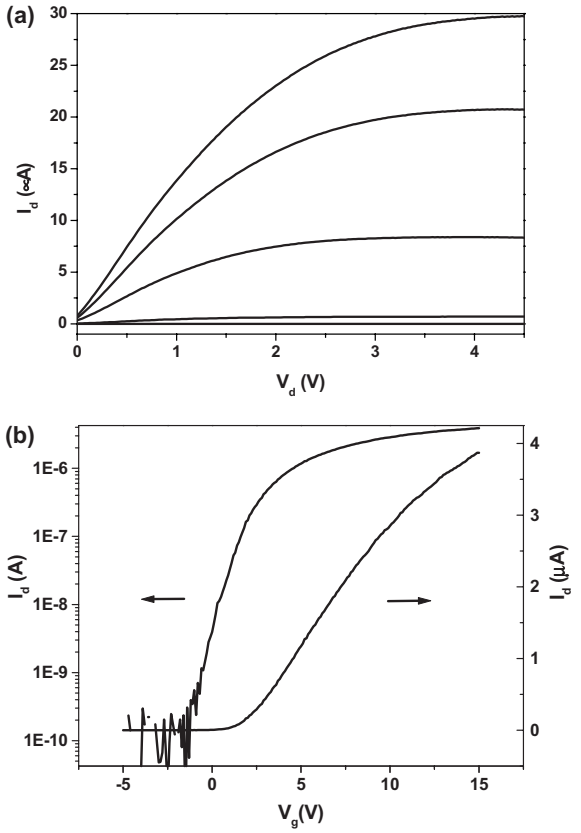

Figure 11. a) Current–voltage curves of thin film transistor device that uses G2 silicon ribbons. The gate voltages range from –5 V to 10 V. The channel length and width are 100 μm. b) Full transfer characteristics of a G2 ribbon device, which indicates an effective device mobility of 145 cm^2 V^{-1} s^{-1} and a per ribbon mobility of 207 cm^2 V^{-1} s^{-1} and an ON/OFF ratio > 10^4.

The process detailed in Figure 1 enables applications that cannot be achieved using previously reported procedures.[35,36] As an example, we fabricated photodiodes that use thick (>10 μm) silicon bars doped with phosphorous (n-type) on one side and boron (p-type) on the other. Figure 12a presents a schematic illustration of the device. The experimental section provides the fabrication details. Time of flight secondary ion mass spectroscopy reveals the depths of these doped regions to be 400 nm and 250 nm respectively. A PDMS stamp was used to transfer an array (20 mm × 20 mm) of ~10 μm thick, 1 mm long and 50 μm wide silicon bars from the source wafer to a PET sheet coated with uncured Ag epoxy (~5 μm thick). The ribbons were placed into contact with the uncured Ag epoxy and then heated at 75 °C for 2 min to bond them to the plastic substrate and to form an electrical connection to the back side (~5 μm thick) as shown in Figure 12b. Peeling back the PDMS stamp away after this heating procedure left the ribbons attached onto the plastic sheet. The substrate was heated further for 15 min at 110 °C prior to electrical measurements.

Figure 12c shows the current–voltage response of a typical device under different illumination conditions. At the highest illumination intensity the turn on voltage for a typical device was ~0.25 V. This kind of thin device might be interesting for

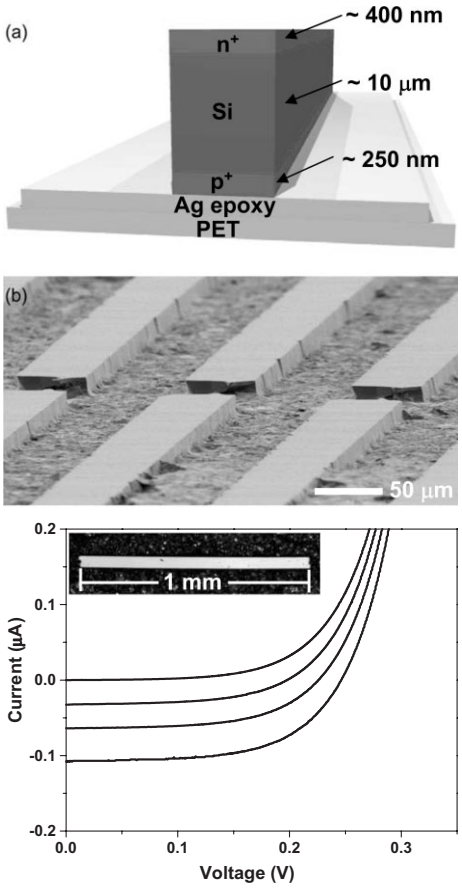

Figure 12. a) Schematic diagram of a photodiode fabricated from a Si bar transfer printed onto a silver epoxy coated PET film. b) SEM images of the silicon microphotodiodes printed onto a PET sheet. c) Current–voltage curves of a typical diode under varying illumination conditions. The inset shows an optical image of the device.

silicon photodetector or photovoltaic systems, particularly when the materials cost represents an important consideration or when the large area coverages enabled by the printing technique provide valuable capabilities.

3. Conclusions

This paper demonstrates that optimized etching chemistries provide a robust fabrication process for smooth, almost defect free high quality single crystal silicon ribbons, platelets and bars from bulk wafers. The experimental data highlight the ability to tune the geometries (i.e., lengths, widths, and thicknesses) of these structures over a range from less than 100 nm to more than 5 cm. Transfer printing procedures with automated printers enable integration of organized arrays of these structures into bendable formats on plastic sheets as well as stretchable geometries on elastomeric substrates. Transistors based on well aligned silicon ribbons formed in this manner show good electrical properties and low operating voltages. In addition, microphotodiodes fabricated from thick silicon ribbons exhibit good diode behavior which shows unique applications in photovoltaics. Taken together, there results might be useful in the development of semiconductor devices, materials and processing approaches for large area, low cost electronics. Replacing the angled evaporation steps to simplify the processing, identifying strategies that minimize the amount of etched silicon and developing related processing approaches for silicon wafers with different orientations represent some of the technological challenges that are currently being addressed.

4. Experimental

Fabrication of Silicon Ribbons: A layer of photoresist (PR; Shipley S1805) was spin-coated on a (111) Silicon wafer (Montco silicon, n-type or p-type, 400 μm thick, resistivity = 5–15 Ω cm) at 3000 rpm for 30 s and soft baked at 110 °C for 2 min. A two step ultraviolet (UV) exposure consisting of near field phase shift photolithography and traditional lithography produced 400 nm wide lines of photoresist [68]. The first exposure used a polydimethylsiloxane (PDMS) phase mask patterned with a pattern of lines of relief with depths of 1.8 μm, widths of 10 μm and separations of 10 μm. Placing this mask into conformal contact with the photoresist, exposing it to UV light (10 mW cm^{-2} in intensity, Karl Suss MJB3 mask aligner) for 2.7 s, removing the mask and developing the unexposed regions of the resist generated PR lines aligned perpendicular to the <1$\bar{1}$0> direction. The second exposure used a Cr photomask to remove certain portions of these PR lines, thereby defining the lengths of the ribbons and the positions of the anchors. Developing the patterned wafer for 10 s in developer (MF-26 A, Microchem corp., Newton, MA) generated 10 μm × 185 μm photoresist patterns. The wafer with patterned PR was subsequently placed in a chamber of an electron beam evaporator (Temescal, Berkeley, CA), for deposition of Ti/Au (3 nm/30 nm). Removing the acetone defined etch masks of Ti/Au. Dry etching (Plasma-Therm reactive ion etching (RIE) system, SF_6, 40 sccm, 30 mTorr, RF power = 200 W, 45 s) removed the exposed silicon to form ~500 nm (up to 12 μm) deep trenches. Anisotropic etching of the silicon was accomplished with either solutions of potassium hydroxide or Tetramethylammonium hydroxide (TMAH, 25 wt %, Sigma-Aldrich, Milwaukee, WI). The KOH etchant was formed by dissolving KOH pellets in water and, in some cases, mixing in IPA. The sidewall "refining" step was carried out in a 35 wt % KOH/IPA mixture at 85 °C for 4 min to produce straight, 90° sidewalls. Next, the Ti/Au metal mask was removed by wet etching (Transene Co., Danvers, MA). The wafer was then loaded in a horizontal tube furnace to grow a thermal oxide layer (60 nm thick at 1100 °C), and was subsequently coated with a 270 nm thick conformal layer of silicon nitride film (Plasma-Therm plasma enhanced chemical vapor deposition system [PECVD], SiH_4 gas 200 sccm, N_2 gas 900 sccm, NH_3 gas 5 sccm, 900 mTorr, RF power = 25 W). Angled evaporation of Ti/Au (3 nm/30 nm) was carried out in an ebeam chamber at a 75° angle normal to the wafer, providing partial or complete coverage of the sidewalls of the trenches. RIE (CF_4, 40 sccm, 50 mTorr, RF power = 150 W, 5 min) removed the silicon nitride and thermal oxide not protected by the Au/Ti. Silicon ribbons were completely undercut etched with a (35 wt %) KOH solution at 85 °C. A 49 wt % HF solution removed the silicon nitride-thermal oxide to complete the fabrication process. The substrates were cleaned in 1:1:5 HCl:H_2O_2:DI-H_2O solution rinsed in DI water and dried with N_2 gas.

The phase mask was prepared from a 'master' fabricated on a SOI wafer with (110) top silicon [68]. The master was exposed to a vapor of (tridecafluoro-1,1,2,2-tetrahydro-octyl)-1-trichlorosilane (United Chemical Technologies Inc., Bristol, PA) in a vacuum desiccator for 1 h to functionalize the native oxide on the silicon as well as the exposed regions of the buried oxide. PDMS (component ratio A/B = 1:10, Sylgard 184, Dow Corning Corp., Midland, MI) was poured onto the master and subsequently cured at 65° C for 3 h. Peeling back the PDMS completed the fabrication of the phase mask.

ADVANCED FUNCTIONAL MATERIALS

Ultra-long and Thick Ribbons: The widths, lengths and thicknesses of the silicon structures can be controlled by modulating the lengths and widths of the relief structures on the phase shift mask, the angle of the metal evaporation, the depth of the RIE etching that defines the trenches, the time of the KOH undercut etch, and the spacing between the trenches. We fabricated a 3 inch phase shift mask for the production of ultra-long silicon ribbons (~6 cm) using the procedures outlined in section 4.1. The silicon ribbons were designed such that they remain attached at one of their ends to the source wafer.

Thick silicon ribbons were fabricated by adjusting the depth of the isotropic etching step for the trenches by using either long RIE etching or etching with an inductively coupled plasma reactive ion etcher (STS-ICPRIE, STS Mesc Multiplex Advanced Silicon Etcher). For example, STS ICPRIE parameters that generated silicon trenches approximately 12 μm deep were: Gas flow rate: $O_2/SF_6 = 13/130$ sccm for the silicon etching step and $C_4F_8 = 110$ sccm for passivation, gas pressure: 94 mTorr, etching power: 600/12 W inductively coupled plasma (ICP)/platen (P), deposition power: 600/0 W for ICP/P, etching duration: 7 s, and deposition duration: 5 s. Immersing the samples in $NH_4:H_2O_2:H_2O = 1:1:5$ removed the deposited fluoropolymer on the silicon sidewalls. Next, a process similar to that in Figure 1 was performed. An angle of evaporation of 60° normal to the wafer surface produced 10.7 μm thick, 190 μm long and 10 μm wide silicon ribbons. A PDMS stamp was used to remove these thick silicon ribbons from the wafer. Peel rates of ~0.01 m s^{-1} were used to detach the silicon ribbons from their anchors [44].

Stretchable Silicon: An un-deformed PDMS stamp was placed in conformal contact with the surface of a wafer bearing anchored ribbons then peeled back to lift the ribbons off of the wafer (efficiencies of >95 %). Next, a slab of PDMS treated with UV ozone (UVO) was placed in a mechanical stage and stretched by ~10 %. The untreated PDMS stamp inked with silicon ribbons was placed into contact with the strained PDMS while gently applying pressure to insure conformal contact between the substrates. Peeling back the stamp transferred the ribbons onto the prestrained substrate with >95 % transfer efficiency.

Selective Area Printing: A home-built programmable 3-axis mechanical stage instrument was used to selectively print silicon ribbons onto a receiving substrate. In the example shown here, a piece of a silicon wafer with area 12 mm × 14 mm was used to produce a dense array of anchored ribbons. The printing used a PDMS stamp consisting of a 2 × 2 array of square relief structures with lateral dimensions of ~0.5 mm × 0.5 mm and relief heights of ~35 μm. The stamp was placed in a sample holder on the motorized stage, under computer control. A series of retrieving (i.e., 'inking') and printing steps were performed until the donor substrate was completely depleted, resulting in a 40 mm × 48 mm printed array of silicon ribbons on the receiver substrate.

Large Area Printing: A PDMS stamp (i.e., transfer element) was made by pouring a mixture of PDMS (A/B 1:10, Sylgard 184, Dow Corning) in a 100 mm × 15 mm petri dish followed by curing at room temperature overnight. The transfer element was placed in conformal contact with the top surface of a 3 in silicon wafer patterned with fully undercut silicon ribbons. Quickly delaminating the PDMS stamp resulted in the retrieval of all of the silicon ribbons (greater than 99 % pick-up efficiency). The silicon ribbons "inked" on the PDMS stamp can be transferred to glass or plastic substrates. In the processes described here, the transfer element was placed in contact with a PDMS coated (i.e., 500 nm thick) glass substrate, to form a physical bond between the ribbons and the PDMS layer. Quickly delaminating the PDMS stamp transferred all of the silicon ribbons to the desired substrate with efficiencies of greater than 95 %.

In the regeneration process, the used silicon wafer (i.e., donor substrate) was chemically polished in a 40 wt % KOH solution at 120 °C for 15 min to remove the relief features associated with the anchors. This process prepares the substrate for another round of ribbon fabrication.

Device Fabrication: A Ti (2 nm)/Au (50 nm) gate electrode was deposited onto a polyimide (25 μm thick, Kapton) substrate, followed by PECVD deposition of a SiO_2 layer (~80 nm). A photopatternable epoxy (SU-8 5, Microchem) diluted by 90 vol % in a thinner (SU-8 thinner) was spin cast onto the SiO_2 layer at 3000 RPM for 30 s and subsequently exposed to UV light (~10 mW cm^{-2}) for 15 s. The PDMS stamp "inked" with G2 ribbons was placed in contact with the epoxy adhesive layer at 75 °C for 1 min and peeled back to transfer the silicon ribbons to the Kapton. The substrate was then fully cured at 125° C for 5 min. The silicon ribbons sink into the epoxy layer during the pre-curing step leaving approximately ~190 nm of dielectric material between the bottom of the silicon and the top of the gate electrode, as determined by AFM. Contact pads of Ti (200 nm) were evaporated onto the substrate patterned by photolithography and etch back with TFTN Ti etchant (Transene Co).

Silicon photodiodes were generated from p-type silicon wafer which was heavily n-doped at the top surface with spin-on-dopant (P509, Filmtronics) and activated at 1100 °C for 2 min [41]. The p-doped junction was generated by coating the structure in Figure 1g (metal masked was removed prior to this step) with spin-on-dopant (B219, Filmtronics) and activated 1100 °C for 1 min. The structures were retrieved with a PDMS slab and transfer printed onto a 5 μm thick Ag epoxy coated PET sheet. Ag paint was used to contact the top of the cell while the Ag epoxy coated on the PET served as the common back electrode.

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