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Inorganic Semiconductors for Flexible Electronics**

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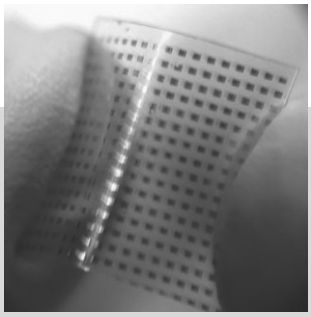

This article reviews several classes of inorganic semiconductor materials that can be used to form high-performance thin-film transistors (TFTs) for large area, flexible electronics. Examples ranging from thin films of various forms of silicon to nanoparticles and nanowires of compound semiconductors are presented, with an emphasis on methods of depositing and integrating thin films of these materials into devices. Performance characteristics, including both electrical and mechanical behavior, for isolated transistors as well as circuits with various levels of complexity are reviewed. Collectively, the results suggest that flexible or printable inorganic materials may be attractive for a range of applications not only in flexible but also in large-area electronics, from existing devices such as flat-panel displays to more challenging (in terms of both cost and performance requirements) systems such as large area radio-frequency communication devices, structural health monitors, and conformal X-ray imagers.

1. Introduction

Electronic systems that can cover large areas on flexible substrates have received increasing attention in the last couple of decades because they enable classes of applications that lie outside those easily addressed with wafer-based electronics. Examples include flexible displays, electronic textiles, sensory skins, and active antennas.[1,2] This type of electronics, sometimes referred to as macroelectronics, differs from established microelectronic and nanoelectronic systems, where progress is driven primarily by reducing the critical dimensions of the functional elements (e.g., channel lengths and dielectric thicknesses in transistors) to increase the speed and computing capacity and to reduce the operating voltages. Macroelectronics, instead, uses thin-film transistors (TFTs) distributed over large areas where, in existing applications that use glass substrates, they provide switching elements in active-matrix liquid-crystal displays (AMLCDs) or medical X-ray imaging devices.[3] Here, the overall size of the systems rather than the minimum feature size of an individual circuit component represents the primary scaling metric. Amorphous silicon (a-Si) is currently the dominant semiconductor used for transistors in these systems. In fact, this material is now the second most economically significant semiconductor, behind single-crystal silicon. An emerging direction in research is to develop alternative materials and patterning techniques for these macroelectronic systems, with a goal of increasing their performance, decreasing their cost (per unit area), and enabling them to be formed on low-cost, bendable substrates. Low-temperature deposition or printing-type techniques for fabricating of high-quality semiconductor films on substrates such as metal foils,[4] plastic sheets,[5] and even paper[6] are of

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particular interest. Integrating semiconductors with plastic substrates, which are the most attractive type of flexible substrate for many applications, requires processing temperatures below the glass-transition or thermal-degradation temperatures of the plastics. Although many promising results have been obtained with thin films of small-molecule organics and polymers,[7] the electrical performance that can be obtained from them is still too low (comparable to a-Si in the best cases) for many potential applications. Even with high-purity single crystals of these materials the mobilities are less than those of polycrystalline silicon.[8,9] Furthermore, the uncertain long-term reliability and lack of controlled doping techniques for these materials represent other areas that require further research.

By contrast, many inorganic semiconductors exhibit high carrier mobilities and excellent stability.[10] The main challenge, for uses in macroelectronics on plastics, for example, is that forming high-quality films of these materials and certain steps associated with processing them into devices require temperatures that exceed the glass-transition and/or thermal-decomposition temperatures of the plastics. Also, many aspects of the growth and processing do not scale easily to large areas without the use of complex manufacturing systems. Progress in the last several years, however, has led to examples of methods that avoid these limitations. This Review summarizes some of this work, with an emphasis on inorganic semiconductor films that have been, or have the potential to be, integrated with plastic substrates to generate high-performance TFTs. The materials include films of silicon with various levels of crystallinity (i.e., from amorphous to poly- and monocrystalline), transparent oxides, chalcogenides, nanowires synthesized via "bottom-up" chemical routes, and nano-/microstructures fabricated from wafers via "top-down" approaches. This article reviews the properties achievable with these materials, using field-effect mobilities (as determined by standard analysis of characteristics measured in transistor devices) and on/off current ratios as the primary metrics. The content is organized according to the material type, with discussions of the techniques for growing the films and illustrative examples of devices and circuits that have been built with them. The last section presents some perspectives on the trends for future work.

2. Films of Silicon—From Amorphous to Large-Grained Polycrystalline

TFTs fabricated with hydrogen-terminated amorphous Si (a-Si:H) represent, by far, the most successful systems for applications in large-area electronics. Silicon films with various degrees of crystallinity and mobilities that can be orders of magnitude larger than a-Si:H can be formed using a-Si precursor films and thermal treatments. These films are classified as nanocrystalline Si (nc-Si), microcrystalline Si (μc-Si), and

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polycrystalline Si (pc-Si). The mobilities, in general, increase with grain size because the grain boundaries often represent scattering and trapping sites. Figure 1 summarizes the properties of different Si films formed through chemical vapor deposition (CVD) approaches. Among the methods listed in this figure, radiofrequency plasma-enhanced chemical vapor deposition (RF-PECVD) is the most widely used, and can be implemented with highly engineered manufacturing tools. Although relatively high temperatures (i.e., ca. 250 °C) are typically needed to achieve high-quality a-Si films with high hydrogen concentrations (typically on glass substrates), low-temperature processes have been investigated in recent years to enable direct deposition of a-Si and nc-Si onto plastic substrates.[11] For example, TFTs fabricated with 50 nm a-Si:H films grown via RF-PECVD at 75 °C on poly(ethylene terephthalate) (PET) substrates show performance comparable to similar devices fabricated on glass substrates, that is, mobilities of ca. 0.4 $cm^2 V^{-1} s^{-1}$ for n-type channels and on/off current ratios of $>10^5$.[12] In addition, PECVD films of Si can be easily doped in situ by proper selection of gases for growth.[13] Films of nc-Si deposited at 150 °C by PECVD excited at radiofrequencies of 80 MHz (much higher than the traditional frequency of 13.56 MHz) exhibit mobilities of 0.06–0.2 $cm^2 V^{-1} s^{-1}$ for holes and ca. 12 $cm^2 V^{-1} s^{-1}$ for electrons in the saturated regimes in TFTs fabricated with these films.[14] Higher mobilities (e.g., ca. 150 $cm^2 V^{-1} s^{-1}$ for electrons) can be achieved in TFTs fabricated with nc-Si films grown at higher temperatures, for example, around 260 °C, on glass substrates.[15] Although plastic substrates were not demonstrated, the growth temperature is compatible with certain high-temperature plastics (e.g., polyimide). The PECVD process can also be carried out with microwave radiation at 2.45 GHz. Absorption at this frequency can be enhanced with magnetic fields, resulting in efficient dissociation of the silane precursors. The magnetic field causes the electrons to move in a circular motion (i.e., electron cyclotron resonance (ECR)) at the microwave frequency. This method, also called ECR-PECVD, offers several advantages over RF-PECVD in terms of deposition rate and defect concentration.[16] In addition to plasmas, thermal energy generated from heated wires can decompose silane molecules to grow a-Si and nc-Si films on both hard and soft plastic substrates.[17] In this approach, known as hot-wire chemical vapor deposition (HW-CVD), the substrate and decomposition temperatures can be independently controlled. Silicon films grown via this method exhibit properties somewhat worse than those formed by PECVD, in terms of mobility. For example, on PET substrates TFTs fabricated with HW-CVD a-Si films show mobilities (for electrons) of ca. 3×10^{-4} $cm^2 V^{-1} s^{-1}$ in the saturated regime. Devices fabricated with RF-PECVD a-Si films show mobilities of around 0.1 $cm^2 V^{-1} s^{-1}$ for similar deposition temperatures (i.e., 100 °C).[18]

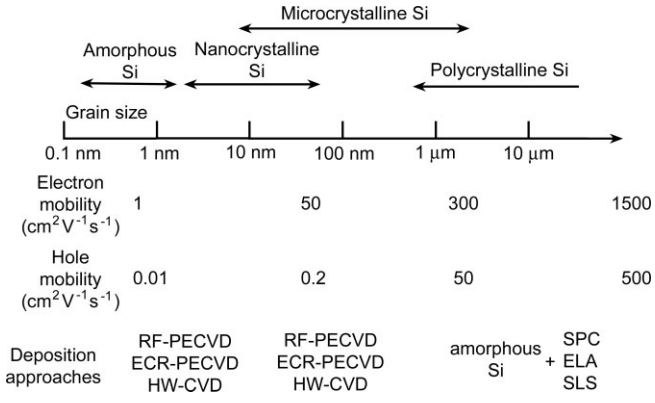

Figure 1. Grain sizes and carrier mobilities of Si films with various crystallinities grown via dry processes. Abbreviations: RF-PECVD, radiofrequency plasma-enhanced chemical vapor deposition; ECR-PECVD, electron cyclotron resonance plasma-enhanced chemical vapor deposition; HW-CVD, hot-wire chemical vapor deposition; SPC, solid-phase crystallization; ELA, excimer-laser annealing; SLS, sequential lateral solidification.

Transport in films of a-Si and nc-Si grown using these procedures can be improved significantly by transforming them into pc-Si films with techniques such as solid-phase crystallization (SPC), excimer-laser annealing (ELA), or sequential lateral solidification (SLS).[19] SPC involves the solid-state transformation of the energetically metastable a-Si phase into crystalline Si. Although this process can yield large-grain materials and good performance (e.g., TFTs made of n-type pc-Si films crystallized at 650 °C show mobilities of 64 $cm^2 V^{-1} s^{-1}$ in both linear and saturated regimes[20a]) in TFTs on flexible steel foils,[20] the high intragrain defect density can limit the characteristics. Also, the high processing temperatures are not compatible with plastic. A straightforward approach that avoids these limitations involves converting a-Si into pc-Si on a high-temperature substrate (such as glass) and then transferring the resulting pc-Si onto a plastic substrate.[21] Introducing this type of transfer process, however, complicates the fabrication sequence and thus increases the cost. Another approach uses lasers to heat, on short time scales but to high temperatures, the a-Si to convert it to pc-Si. When implemented with suitably designed thermal buffer layers, this approach can be performed directly on certain plastic substrates, such as polyimide. The two most established laser methods are ELA and SLS. Figure 2A presents a scanning electron microscopy (SEM) image of a pc-Si film formed by ELA, clearly showing grains with characteristic sizes of a few hundred nanometers.[19] The grain size formed by ELA is usually similar to the laser wavelength, resulting in large grain boundaries (i.e., a high density of defects) in the channel regions of the TFTs. The correlation between grain size and laser wavelength is thought to originate from interference effects in waves scattered at surface protrusions formed as a result of the volume expansion upon lateral solidification.[22] Larger grains with more controlled and optimized shapes can be achieved with a variant of ELA, known as SLS. This method uses a patterned beam (versus flood irradiation for ELA) to induce lateral crystallization of the melted Si from seeds in neighboring regions that were melted in the previous laser pulse. Briefly,

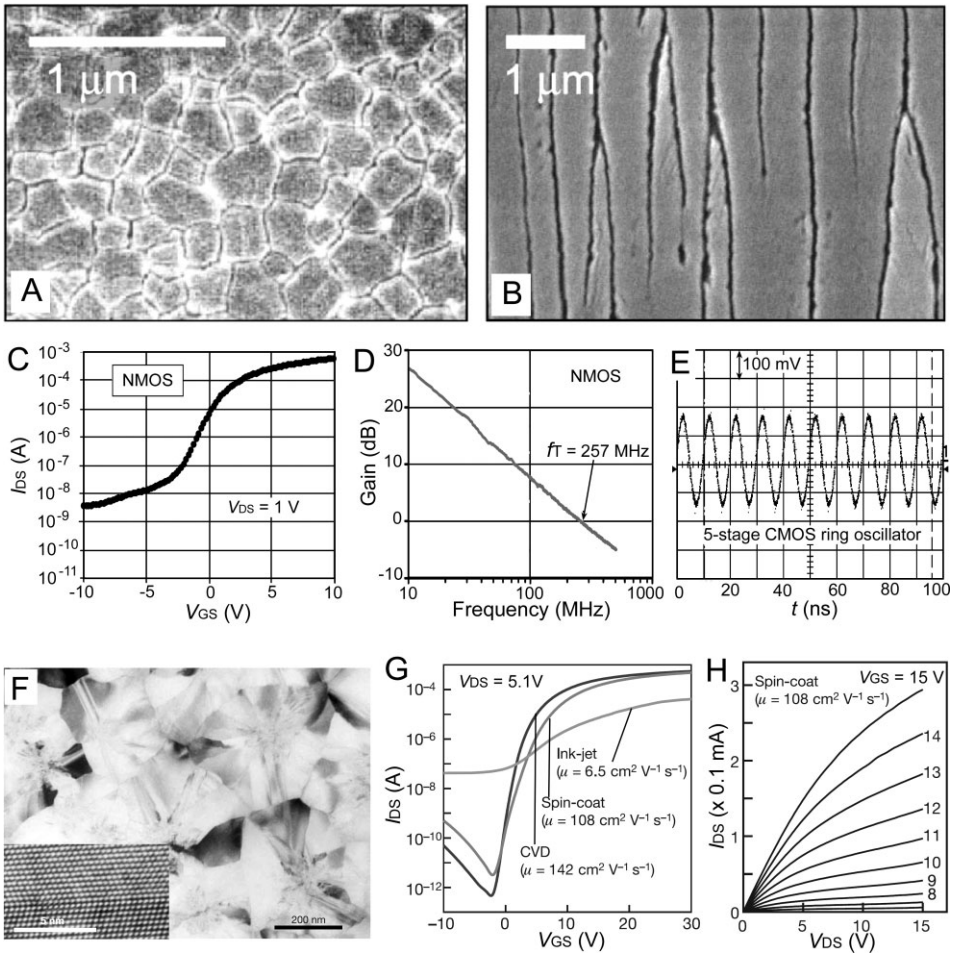

Figure 2. A,B) SEM images of defect-etched pc-Si films obtained by processing PECVD a-Si layers with different pulsed-laser crystallization techniques: A) ELA; B) line-scan SLS. These images show the different crystalline structures in the pc-Si films. Reproduced with permission from [19]. Copyright 2006 Materials Research Society. C–E) Characterization of TFTs and circuits fabricated with pc-Si films on polyimide substrates obtained by SLS. C) Transfer characteristics of an n-type TFT with channel length and width of 10 and 100 μm, respectively, measured at V_{DS} = 1 V. D) Microwave evaluation of an n-type TFT (channel length 2 μm). The unity current gain frequency (f_T) is the frequency at which the current gain passes through unity (0 dB gain). E) Output waveform of a five-stage, complementary metal-oxide semiconductor (CMOS) ring oscillator, fabricated with *n*- and p-type pc-Si films on a polyimide substrate and evaluated at drive bias (V_{DD}) of 15 V. The TFTs have channel lengths of 2 μm. The frequency is approximately 100 MHz. Adapted with permission from [25]. Copyright 2005 IEEE. F) Transmission electron microscopy (TEM) image of a pc-Si film formed using an a-Si layer deposited from a liquid precursor. The inset shows a high-resolution TEM image. G,H) Electrical characteristics of TFTs fabricated with pc-Si films shown in (F). The properties of different pc-Si films obtained through various approaches are also compared in (G). Adapted with permission from [27]. Copyright 2006 Nature Publishing Group.

SLS uses an iterative process that involves two (or more) well-defined steps: i) laser irradiation that completely melts the Si in a localized region, resulting in lateral growth of grains that initiate from the periphery of the melted spot; and ii) additional irradiation using spatially translated pulses that melt the Si next to the originally irradiated spot such that the existing grains grow epitaxially to extend the size of the crystalline regions. As a result, SLS always produces grains with much larger sizes, better-controlled shapes, and higher degrees of uniformity compared to ELA.[23] Figure 2B shows an SEM image of a Si film converted through line-scan SLS, indicating the formation of stripes of crystalline Si with high aspect ratios (i.e., the ratio of length to width),[19] which, when oriented along the channel in a transistor, can offer high mobility transport. In addition, other microstructures of crystalline Si can be obtained via various SLS schemes, as controlled by the patterns of the laser beams and the sequences of the pulses.[24] With thermal buffer layers, SLS can generate pc-Si films with quality similar to that shown in Figure 2B on plastic substrates (e.g., polyimide sheets with thicknesses of 10 μm formed on Si wafers).[25] Figure 2C shows the transfer characteristics of a transistor with a channel length of 10 μm and channel width of 100 μm, fabricated with n-type pc-Si film on polyimide. The mobility (for electrons) and threshold voltage (V_{th}) for this device are 191 cm^2 V^{-1} s^{-1} and 1.1 V, respectively. Microwave measurements indicate unity current gain frequencies (f_T) as high as 257 MHz for transistors with channel lengths of 2 μm (Fig. 2D). Because a-Si films can be easily

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doped in situ during deposition by controlling the feed gases, p-type metal-oxide semiconductor (PMOS) field-effect transistors made of pc-Si films can also be fabricated. Such devices on polyimide sheets also display good performance: mobility (for holes) of 45 $cm^2 V^{-1} s^{-1}$, V_{th} of –13.9 V, and f_T of 184 MHz for devices with channel lengths of 2 μm. Integrating n- and p-type devices generates flexible complementary metal-oxide semiconductor (CMOS) inverters and more complex circuits. Figure 2E shows output waveforms from a five-stage CMOS ring oscillator (with device channel lengths of 2 μm) with an oscillation frequency of ca. 100 MHz. Similar procedures can also be carried out on bendable steel foils to yield pc-Si TFTs with comparable performance.[26] Steel foils are attractive in this case because they do not require the thick thermal buffer stacks that are needed with plastic. They have the disadvantages that, compared with certain plastics, they are relatively expensive; they are not lightweight; they require specialized processing and conformal coatings to generate smooth surfaces; they are opaque, which, for example, prevents their use in backlit displays; and they are conductive, which leads to parasitic capacitance that can limit high-speed performance.

Although CVD techniques currently provide the most effective and versatile approaches to depositing Si, solution-printing techniques could be valuable as low-cost alternatives. Recent work shows, for example, that solutions of polysilanes formed by photopolymerization of cyclopentasilane (CPS) dissolved in a mixed solvent of CPS and toluene, referred to as liquid Si, can generate a-Si as well as pc-Si films.[27] The fabrication in this case begins with spin-casting a film of this liquid Si. Prebaking drives the volatile solvent components (CPS and toluene) out of the film. The Si–Si bonds in the polysilane start to break at temperatures near 280 °C, and a fraction of the polysilane is released as SiH_2 and SiH_3. At higher temperatures (i.e., ca. 300 °C) the Si–H bonds break and Si atoms start to polymerize, resulting in the formation of a 3D a-Si network. Bottom-gate TFTs fabricated with a-Si films generated in this manner and further baked at 540 °C for 2 h exhibit mobilities (for electrons) of only 10^{-3}–10^{-4} $cm^2 V^{-1} s^{-1}$, which is three or four orders of magnitude smaller than that of a-Si obtained through PECVD. The poor mobility can be attributed to the low concentration of hydrogen (0.3 %) in a-Si films formed at 540 °C, which leads to appreciable quantities of dangling bonds that frustrate transport. Although spin-coated films baked at 300 °C or lower contain more than 20 % hydrogen, they are not completely transformed into a-Si and can be easily oxidized in air. The a-Si films can, however, be laser-annealed (308 nm XeCl excimer) to convert them into pc-Si. The transmission electron microscopy (TEM) image in Figure 2F shows the polycrystalline nature of films produced in this manner. Figure 2G compares the transfer curves of TFTs (with the same geometry) built with pc-Si films formed by laser annealing of a solution-cast film of a-Si and one formed by conventional CVD. The mobilities (for electrons) of devices that use the solution-deposited a-Si are as high as 108 $cm^2 V^{-1} s^{-1}$, slightly lower than those that used CVD a-Si. Figure 2H plots the current–voltage (I_{DS}–V_{DS}) curves of a typical TFT at different gate voltages (V_{GS}). Solution processing is interesting because it allows films of a-Si to be printed, for example, through ink-jet nozzles. The thickness variations associated with such printed films, however, lead to poor properties in the laser annealed films (Fig. 2G). Obtaining uniform films, and optimizing the physical properties of the liquid precursor, such as its stability in an ambient environment, its viscosity, vapor pressure, and surface tension, represent areas for future work. In addition, the relatively high temperatures (e.g., 540 °C) needed to form the a-Si may prevent this method, in its current form, from being used with plastic substrates.

3. Films of Transparent Oxides

Oxides of transition metals, such as ZnO and its derivatives, provide another class of inorganic semiconductor for large-area electronics. These oxides are usually transparent in the visible owing to their large bandgaps of >3 eV. This optical property, when combined with transparent conductors and dielectrics, allows unusual applications, such as invisible electronics for heads-up displays on windshields or cockpit enclosures. Such oxide thin films, with properties suitable for TFTs, can be formed on both inorganic and plastic substrates by either gas-phase deposition or solution processes. The mobilities that can be achieved using the processes described in the following sections are in the range of ca. 1–70 $cm^2 V^{-1} s^{-1}$ with typical values of approximately 10 $cm^2 V^{-1} s^{-1}$.

3.1. ZnO Films Deposited From the Gas Phase

Radiofrequency magnetron sputtering[28] and pulsed-laser deposition[29] are the most commonly used techniques to form films of ZnO for device applications. In a typical process, ZnO removed from a solid target by use of these methods deposits on the surface of a substrate, usually at or near room temperature, in a vacuum chamber. An appropriate pressure of O_2 helps to eliminate defects (i.e., oxygen vacancies). Similar deposition techniques can also grow doped ZnO films with high conductivities, suitable for use as electrodes, by using targets that consist of mixtures of ZnO and dopants (e.g., Al_2O_3 and Ga_2O_3).[28] ZnO films formed in this way crystallize into grains with sizes in the range of several nanometers to tens of nanometers, resulting in surface roughness of several nanometers (see the typical SEM image shown in Fig. 3A).[30] This roughness can be important, depending on the device layout, because it can frustrate the use of (nonconformal) thin-film dielectrics (<10 nm) and it can degrade transport characteristics.[31] Increasing the substrate temperatures and/or post-thermal-annealing treatments can increase the grain size, which, in turn, can enhance device performance.

Figure 3B shows the geometry of some transparent TFTs fabricated with a ZnO film deposited at room temperature.[32]

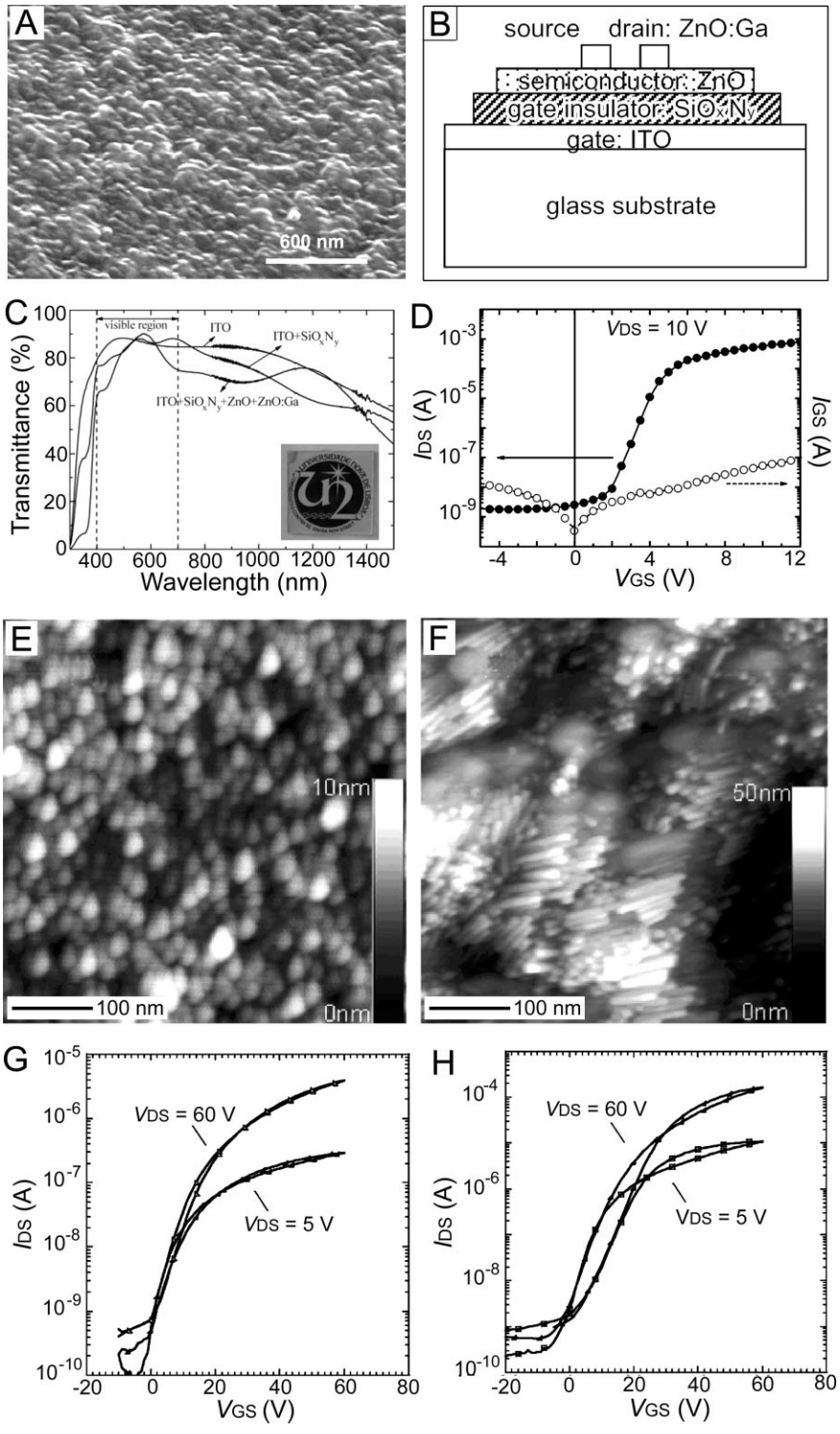

Figure 3. A) SEM image of a ZnO film deposited by radio frequency magnetron sputtering, showing the polycrystalline characteristics of the film. Reproduced with permission from [30]. Copyright 2005 Elsevier B.V. B) Geometry, C) optical, and D) electrical characterization of transparent TFTs fabricated with ZnO films as the semiconductor. Adapted with permission from [32]. Copyright 2004 Elsevier B.V. E,F) Atomic force microscopy images of assembled films formed by spin-casting dispersions of ZnO nanospheres and ZnO nanorods, respectively. G,H) Electrical characteristics of TFTs fabricated with films shown in (E,F). (G) and (H) correspond to the films of ZnO nanospheres and nanorods, respectively. Reproduced with permission from [39]. Copyright 2005 American Chemical Society.

In this case, a glass slide coated with an indium tin oxide (ITO) layer (100 nm thick) as a gate electrode provides a substrate on which a film of silicon oxynitride (SiO_xN_y; 200 nm thick) as the gate dielectric and a semiconducting film of ZnO (150 nm thick) are sequentially deposited via radiofrequency magnetron sputtering at room temperature. Films of Ga-doped ZnO (GZO; 100 nm thick) patterned by a lift-off process define the source and drain electrodes. These processes yield transparent TFTs with channel lengths and widths of 40 and 200 μm, respectively. The transparency of the materials (including the glass substrate of 1.1 mm thickness), as well as the TFTs in a spectral range of 300–1500 nm, are shown in Figure 3C. The average transmittance in the visible region is as high as 84 % for the TFTs. The comparison in Figure 3C indicates that transmission losses due to the ZnO TFTs (vs. the pristine glass substrate with ITO layer) are negligible (ca. 4 %). The inset shows a glass substrate (5×5 cm^2) covered by arrays of ZnO TFTs, through which an underlying logo is clearly visible. Electrical measurements indicate enhancement-mode n-type operation of these devices. Figure 3D presents a transfer curve from a typical transistor in the saturation regime (i.e., $V_{DS} = 10$ V). The mobility (for electrons) and V_{th} of this device are ca. 70 cm^2 V^{-1} s^{-1} and 1.8 V, respectively. The on/off current ratio is 5×10^5. Results of initial studies indicate that these devices are stable in an ambient environment.[33] In addition, p-type ZnO can be grown by doping the intrinsic n-type ZnO films with phosphorus (e.g., P_2O_5)[34] or arsenic (e.g., Zn_3As_2).[35] The availability of both n- and p-type ZnO enables the possibility of transparent CMOS circuits. Although all the reported devices are on rigid substrates, for example, glass and Si wafers, devices on plastic substrates might be possible because the materials can be deposited at low temperatures. Using pulsed-laser deposition, polycrystalline ZnO films (with grain size of 17 nm) have been successfully deposited on a flexible polyimide sheet, but no device results were reported.[36]

3.2. ZnO Films Spin-Cast From Colloidal Solutions

ZnO films can also be formed by spin-coating solution suspensions of ZnO nanocrystals in the form of chemically synthesized and functionalized spheres or rods. Control over reaction conditions and recipes allows the dimensions, shapes, and compositions of ZnO colloids to be selected over a wide range.[37,38] High-concentration (>50 mg mL^{-1}) suspensions of colloidal ZnO are generally desired, and can be achieved by attaching long-chain surfactant molecules to the ZnO surfaces. For example, ZnO nanoparticles with diameters of ca. 6 nm and nanorods with widths and lengths of 10 and 65 nm, respectively, and chemically modified with butylamine (with a low boiling point of 78 °C) can be dispersed in chloroform at concentrations of ca. 90 mg mL^{-1}. Spin-casting them onto SiO_2(300 nm)/Si wafers with prepatterned interdigitated Cr(3 nm)/Au(12 nm) source and drain electrodes form ZnO TFTs where the SiO_2 and Si provide the gate dielectric and the gate, respectively.[39] Annealing these devices at 230 °C in forming gas (N_2/H_2 of 95:5 v/v) for 30 min increases their stability and performance. Figure 3E and F shows atomic force microscopy (AFM) images of films of ZnO nanospheres and nanorods. These data reveal close-packed assemblies of spheres and in-plane aligned arrays of rods. The alignment and relatively large size of the nanorods, compared with the nanospheres, reduces the effective number of interfaces in the channel. Figure 3G and H compares the electrical characteristics (i.e., transfer curves in both linear and saturated regimes) of TFTs formed with films of ZnO nanospheres and nanorods, respectively. In both cases, the devices exhibit n-type transistor behavior. The mobilities of nanosphere TFTs extracted from the plots (Fig. 3G) are 2×10^{-4} cm^2 V^{-1} s^{-1} in the linear regime and 4×10^{-4} cm^2 V^{-1} s^{-1} in the saturated regime, while the linear and saturated mobilities for nanorod TFTs are 0.01 and 0.02 cm^2 V^{-1} s^{-1}, respectively (Fig. 3H). The performance can be improved by further post-deposition processes, that is, hydrothermal growth in an aqueous solution of zinc nitrate and ethyldiamine at 90 °C. These procedures increase the mobilities of the nanorod TFTs to 0.2 and 0.6 cm^2 V^{-1} s^{-1} in the linear and saturated regimes, respectively. These characteristics are, of course, much worse than those obtained with sputtered films, but are nevertheless interesting owing to the compatibility of solution-based techniques with low cost, large-area deposition.

3.3. Films of ZnO-Based Binary and Ternary Oxides

ZnO can crystallize with other materials, such as In_2O_3, Ga_2O_3, and SnO_2, to form binary or ternary oxides that are transparent and offer high mobility. An example is single-crystalline $InGaO_3(ZnO)_5$ (IGZO) films, which can be epitaxially grown on (111) single-crystal yttria-stabilized zirconia (YSZ) substrates, with mobilities as high as ca. 80 cm^2 V^{-1} s^{-1} reported for TFTs fabricated using them.[40] Although such results are not directly relevant to the scope of this Review, recent reports indicate that amorphous IGZO films with good properties can be formed on plastic substrates at room temperature.[41,42] In these systems, as well as for other amorphous oxide semiconductors containing post-transition-metal cations (e.g., ZnO:In^{III}), degenerate band conduction and large mobility are possible. Such behavior is different to that of amorphous covalent semiconductors, such as Si, in which carrier transport is controlled by hopping between localized tail-states and band conduction is not achievable. The conduction band minimum (CBM) in typical wide-bandgap oxide semiconductors (e.g., ZnO) is mainly composed of unoccupied metal *n*s orbitals (*n* denotes the principal quantum number), which can directly overlap neighboring metal *n*s orbitals to generate carrier-transport pathways. In addition, *n*s orbitals with large principal quantum numbers (i.e., $n>4$) lead to greatly dispersed CBM, which in turn leads to high electron mobility if the carrier relaxation times are not significantly different between the constituent materials.[43] As a result, amorphous oxide semiconductors can exhibit Hall-effect mobilities similar to those of their corresponding crystalline phases, even when grown at low temperatures. Figure 4A summarizes the Hall mobility (μ_{Hall}) and carrier concentration (N_e) for films of In_2O_3–Ga_2O_3–ZnO systems deposited by pulsed-laser deposition at room temperature.[41] The results clearly show that high mobility (>10 cm^2 V^{-1} s^{-1}) can be achieved in amorphous oxide systems, i.e., In_2O_3–Ga_2O_3 (a-IGO), Ga_2O_3–ZnO (a-GZO), In_2O_3–ZnO (a-IZO), and In_2O_3–Ga_2O_3-ZnO (a-IGZO).

Figure 4B shows the layout of TFTs fabricated with a-IGZO on a PET substrate. In this top-gate configuration, high-*k* Y_2O_3 (with dielectric constant of ca. 16; k = dielectric constant) and ITO serve as the gate dielectric layers and electrodes, respectively. Figure 4C shows a photograph of a PET sheet with an array of a-IGZO TFTs, laminated on a cylindrical surface (with a radius of 30 mm) for probing, illustrating the transparency and mechanical bendability.[42] The devices also exhibit good electrical performance when operated at room temperature. Figure 4D shows a series of *I*–*V* curves from a TFT with the geometry shown in Figure 4B, recorded at various gate biases in air. The thicknesses of the layers of a-IGZO, Y_2O_3, and ITO are 30, 170, and 40 nm, respectively.[41a] The channel length and width of the transistors are 50 and 200 μm, respectively. The data indicate enhancement-mode, n-type behavior. Both the linear and saturation values of mobility are ca. 10 cm^2 V^{-1} s^{-1}. The transfer characteristics (Fig. 4E) show on/off current ratios of ca. 10^6. In this case, the off current is dominated by gate leakage (I_{GS}), associated with the moderate quality of the low-temperature Y_2O_3 layer. The V_{th} and subthreshold slope ($S = dV_{GS}/d\log|I_{DS}|$) are +1.3 V and ca. 240 mV/decade, respectively, at $V_{DS} = 2$ V. Devices on PET substrates continue to operate when bent to radii of curvature radius as small as 30 mm (Fig. 4C), with only slight (10–15 %) reductions in mobility.

Transparent TFTs of this type are promising for a range of applications, such as backplanes for backlit liquid-crystal dis-

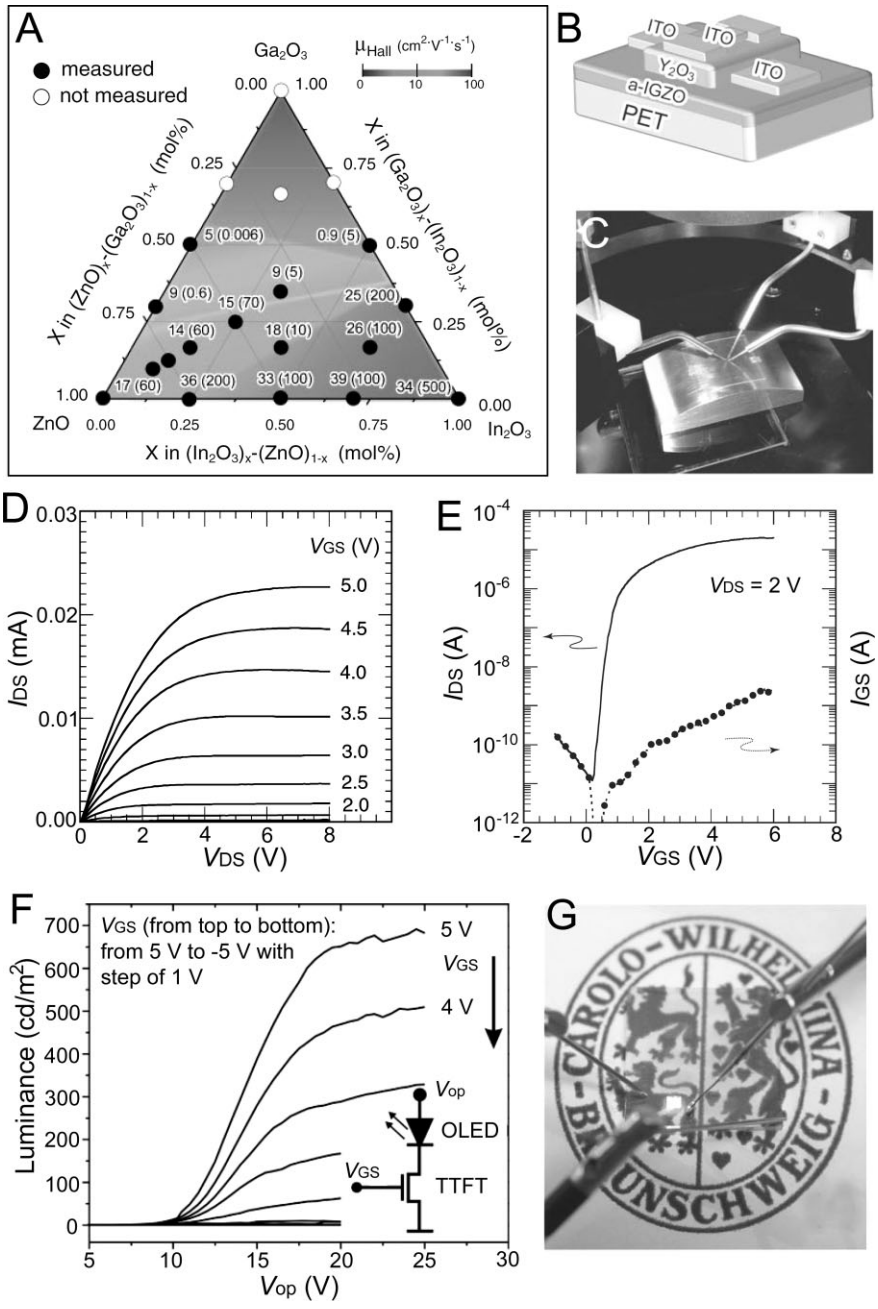

Figure 4. A) Room-temperature Hall mobility and carrier concentration as function of chemical compositions of the a-IGZO system. Values outside and inside parentheses show Hall mobility and carrier concentration in units of $cm^2 V^{-1} s^{-1}$ and 10^{18} cm^{-3}, respectively. B) Geometry of transparent TFTs fabricated with a-IGZO films on plastic PET sheets. C) Photograph of a flexible transparent TFT sheet bent to a radius of 30 mm. The TFT sheet is fully transparent in the visible spectral regime. D,E) Electrical characteristics of typical transparent TFTs using a-IGZO on flexible plastic substrates Panels (A), (D), and (E) reproduced with permission from [41a]. Copyright 2006 The Japan Society of Applied Physics. Panels (B) and (C) adapted with permission from [41b]. Copyright: 2004 Nature Publishing Group. F,G) Characterization of active-pixels composed of transparent TFTs using a-ZTO and OLEDs: dependence of luminance on the operating voltage (V_{op}) at different gate voltages (V_{GS}) applied to the switching transistor (F), and photograph of an active pixel in the "on" state (i.e., V_{GS} = 4 V) (G). Adapted with permission from [44].

plays and for certain types of organic light-emitting diodes (OLEDs). This latter possibility has been demonstrated with TFTs consisting of zinc tin oxide (ZTO; 60 nm thick) as the semiconductor, ITO (R_{sheet} = 8 Ω/square) as the gate electrode, Al_2O_3/TiO_2 (ATO; 220 nm thick) as the gate dielectric, and Al-doped ZnO (AZO; R_{sheet} = 8 Ω/square) as the source and drain electrodes.[44] The devices show mobilities (for electrons) of 11 $cm^2 V^{-1} s^{-1}$ in the saturated regime, on/off current ratios of 10^5, and transmittance >80 % in the visible range. The OLEDs consist of sequentially deposited electron-injection-enhancement layers, bilayers of hole- and electron-transport hosts, hole-transport layers, hole-injection layers, and ITO anode layers, integrated directly with the TFTs (further fabrication details are given by Görrn et al.[44]). Figure 4F shows an equivalent circuit of this hybrid inorganic–organic system and a set of luminance–operation voltage (V_{op}) curves at different gate voltages, indicating good modulation of the OLED emission. Figure 4G presents a photograph of a substrate consisting of ten transparent active-pixel devices, which sit on a background of a seal logo. These kinds of capabilities can be important for many applications, although the processing approaches, in their current form involve temperatures (ca. 350 °C) that are too high for most plastic substrates. Most recently, thin films of In_2O_3 combined with self-assembled thin organic dielectric layers have been used to fabricate transparent transistors with high performance: mobilities of >120 $cm^2 V^{-1} s^{-1}$ and a low operation voltage of ca. 1.0 V.[45]

4. Films of Chalcogenides

Chalcogenide compounds, including sulfides, selenides, and tellurides, are classes of semiconductors that have been used for transistors and other devices since the early days of solid-state electronics. In fact, the first TFT, demonstrated by Weimer in 1962, was fabricated with a thin film of polycrystalline CdS in a structure similar to that of metal-semiconductor field-effect-transistors (MESFETs).[46] Furthermore, the first AMLCD reported by Brody et al. in 1973 used CdSe-based TFTs as the pixel

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switches.[47a] Chalcogenide TFTs were successfully fabricated in the 1970s on not only rigid glass slides but also flexible plastics (e.g., Mylar films and Kapton strips) and certain types of paper.[47b,c] The emergence of MOSFETs and integrated circuits based on crystalline Si technology caused a decline in these development activities. The emergence of nanoparticle and nanowire versions of chalcogenides has led to a re-examination of these materials for transistor applications, particularly in fields such as large-area or flexible electronics, where silicon-wafer-based electronics cannot be used easily. This section summarizes some examples of TFTs fabricated with thin films of chalcogenide quantum dots (spin-cast from solutions) as well as crystalline layers derived from liquid precursors.

4.1. Films of Chalcogenide Nanocrystals

In one of the earliest reports of chalcogenide nanocrystals used in TFTs, a pyridine solution of CdSe particles (average size < 2 nm, without any organic capping layers),[48] formed a semiconducting film between source and drain electrodes (i.e., Cr/Au stacks) on a Si wafer (gate electrode) covered with a layer of SiO_2 (gate dielectric). Baking on a hotplate at temperatures of between 150 and 350 °C removed the solvent and caused the nanocrystals to coalesce (or sinter), forming grains with dimensions of up to 15 nm comparable to those in vapor-deposited CdSe TFTs.[49] Devices baked at 350 °C for 1 h showed mobilities of ca. 1 $cm^2 V^{-1} s^{-1}$ in the linear regime. As an alternative to this type of glassy deposit, careful control over the size distributions of the nanocrystals and the deposition conditions can lead to films that consist of superlattice nanocrystal solids. In particular, recent reports demonstrate the formation of close-packed PbSe nanocrystals (Fig. 5A), encapsulated with a layer of oleic acid, as semiconductors for TFTs.[50] The PbSe nanocrystal films are initially insulating because of the ca. 1.5 nm insulating oleic acid layers. Treating the PdSe films with a 1.0 M solution of hydrazine in acetonitrile increases the conductance of the film by approximately ten orders of magnitude and allows current through the films to be modulated by voltage applied to the gate, in behavior typical of an n-type field-effect transistor. Figure 5B shows the transfer characteristics. Analysis of devices with 8 nm diameter nanocrystals indicates mobilities of ca. 0.4 and ca. 0.7 $cm^2 V^{-1} s^{-1}$ in the linear and saturated regimes, respectively. The mobility increases with nanocrystal size, with a peak value of ca. 0.95 $cm^2 V^{-1} s^{-1}$ for 9.2 nm nanocrystals. The transport behavior of charges in an array of nanocrystals separated by insulating capping molecules depends on various parameters: the energy levels of adjacent nanocrystals (i.e., site energies, α), exchange coupling energy between the nanocrystals (β), and the Coulomb charging energy of the nanocrystal array (E_c). Both the dispersion of site energies ($\Delta\alpha$) and the

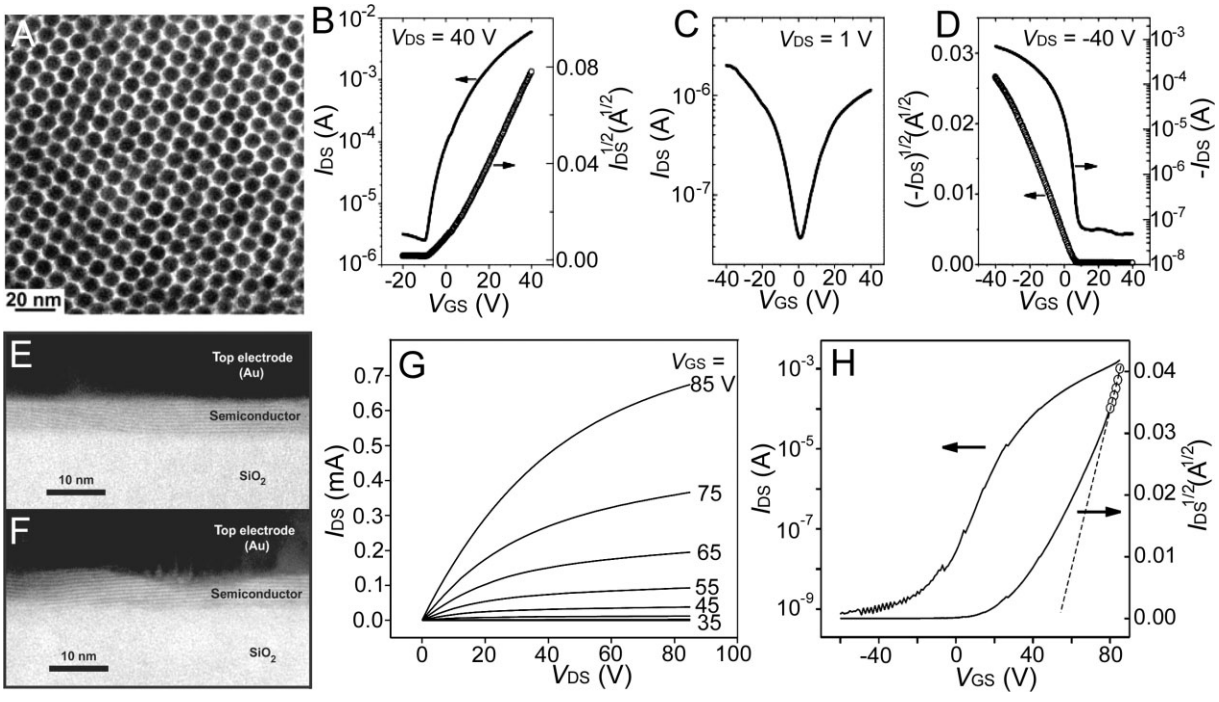

Figure 5. A) TEM image of an array of 8 nm PbSe nanoparticles. B–D) Electrical characteristics of TFTs formed with close-packed PbSe nanoparticle films, treated with hydrazine (B), followed by vacuum treatment or mild heating (C), or complete desorption of hydrazine (D). The devices behaved in n-type, ambipolar, and p-type mode, respectively. Adapted with permission from [50]. Copyright 2005 American Association for the Advancement of Science. E,F) TEM images of cross sections of devices fabricated with films of 5(0.5) nm $SnS_{1.8(1)}$ and 4.2(0.5) nm $SnS_{1.4(1)}Se_{0.5(1)}$, respectively. G,H) Electrical characteristics of the transistor shown in (F) with channel length and width of 14 and 250 μm, respectively. The transfer curves were measured in the saturated regime, i.e., V_{DS} = 85 V. Adapted with permission from [54]. Copyright 2004 Nature Publishing Group.

value of E_c relative to β are important for efficient charge transport.[51] Treating the films with hydrazine produces *activated films*, in which the hydrazine replaces the long-chain oleic acid capping ligands to decrease the interparticle distances, thereby increasing the value of β. The replacement of capping ligands also increases the dielectric constant of surrounding medium (from $\varepsilon \approx 2$ for oleic acid to $\varepsilon \approx 52$ for hydrazine), and thus substantially reduces E_c. These changes facilitate transport in the PbSe nanocrystal solid. Interestingly, vacuum treatment or mild heating (up to 100 °C) of activated PdSe films switches their conductivity from n-type (Fig. 5B) to ambipolar (Fig. 5C) and finally, to p-type (Fig. 5D). The p-type devices exhibit mobilities (for holes) of 0.12 to 0.18 $cm^2 V^{-1} s^{-1}$ in the saturated regime. Switching the transport type from electron to hole is reversible upon treatment with hydrazine. The n-type behavior may possibly result from charge transfer from the hydrazine, as observed for carbon nanotubes.[52] Additional thermal annealing of the activated PdSe nanocrystal films at elevated temperatures, for example, 200 °C, combined with exposure to hydrazine, again yields mobilities (for n-type devices) of as high as ca. 2.5 $cm^2 V^{-1} s^{-1}$ in the linear regime. This type of tunability in carrier transport might be useful for the fabrication of CMOS circuits.

4.2. Films of Chalcogenides Derived From Liquid Precursors

Hydrazine can be used as a solvent for mixtures of chalcogenides and chalcogens to form solution-phase precursors, which can be processed by low-cost, nonvacuum techniques, such as spin-casting and ink-jet printing.[53] For example, adding SnS_2 with an excess of S to hydrazine generates a solution of $(N_2H_5)_4Sn_2S_6$ (a precursor of SnS_2) that can crystallize out upon evaporation of the hydrazine. At elevated temperatures, this dried precursor (i.e., $(N_2H_5)_4Sn_2S_6$) decomposes endothermally, followed by a second broad exothermic process. Further heating leads to condensation of the chalcogenide dimer anions (i.e., $Sn_2S_6^{4-}$) into extended chalcogenide frameworks. Annealing can remove any remaining hydrazine and chalcogens to yield highly crystalline chalcogenide films.[54] Therefore, spin-casting of the precursor solution followed by thermal annealing can generate high-quality thin films of SnS_2 for fabricating TFTs. Figure 5E shows a cross-sectional TEM image of a device built with a ca. 5 nm thick $SnS_{1.8(1)}$ film, showing a continuously crystalline region. The ratio (i.e., 1.8 ± 0.1) between Sn and S, as determined by medium-energy ion scattering (MEIS), is close to the ideal stoichiometric ratio, that is, 2. Thin films of ternary chalcogenide can be produced from precursors formed by dissolving two binary chalcogenides with the same cations and different anions in hydrazine with the addition of an excess of chalcogens. Figure 5F shows a TEM image of 4.2 nm film of $SnS_{1.4(1)}Se_{0.5(1)}$ derived from a precursor formed by dissolving 14 mg SnS_2, 8 mg $SnSe_2$, and 6 mg S in 1.9 mL hydrazine.[54] Figure 5G and H present the electrical characteristics of a TFT (channel length and width of 14 and 250 μm, respectively) fabricated with the film shown in Figure 5F, indicating n-type, enhancement-mode behavior. The transistor exhibits mobilities of 2.4 and 12.0 $cm^2 V^{-1} s^{-1}$ in the linear and saturated regimes, respectively, and an on/off ratio of $> 10^6$. The operating voltage can be decreased by increasing the capacitance of the dielectric and by optimizing the contacts to the semiconductor.[55] p-Type transistors from this kind of solution precursor can be obtained by partial substitution of the main group metal cations of the chalcogenides with transition metals (e.g., $CuInSe_2$).[56]

5. Films of Assembled Nanowires Formed via Chemical Synthetic Techniques

Single-crystalline nanostructures, for example, nanowires and nanoribbons, formed from inorganic semiconductors are of great interest for TFTs because they provide monocrystalline transport pathways, and an associated potential for high performance. For instance, single-crystalline Si nanowires show transport properties that are similar to those of bulk materials.[57] A wide range of chemical synthetic approaches (commonly referred to as bottom-up techniques), including both gas-phase methods known as vapor–liquid–solid processes (VLS),[58] and liquid-phase methods known as solution–liquid–solid processes,[59] are available to generate nanowires of various materials (e.g., Si, Ge, III–V compounds, and II–VI compounds and oxides). A large number of publications reviews these synthetic approaches.[60] The present article focuses only on the formation of effective thin films of these materials and their use in TFT channels.

Fully dense monolayers of aligned nanowires/nanoribbons with uniform end-to-end registry represent ideal configurations for transistor applications. Sub-monolayers leave some fraction of the channel unpopulated with semiconductor material, resulting in low current outputs per physical width of the channels. Multilayer films can lead to nonuniform coverage, unwanted surface topography, and percolation transport pathways. Typically, chemically synthesized nanowires/nanoribbons are dispersed in appropriate solvents before integration into devices, although there are some examples in which these elements grow directly in the device structures.[61] In principle, generating organized arrays from disorganized suspensions requires external forces (e.g., shear forces, mechanical pressures, electrical fields, and magnetic fields) to overcome Brownian motion and to introduce well-defined order. Some of the processes that have been demonstrated for this purpose can be carried out on a wide range of substrates, including plastic. For instance, flow of a nanowire suspension through microfluidic channels can align nanowires of various materials.[62] In this case, shear flows orient the wires parallel to the flow direction. The flow rate controls the degree of alignment, and the deposition time and concentration determine the coverage of nanowires (i.e., density, measured in terms of average separation, of nanowires). This approach works on small scales with sparse arrays; scale-up to large

areas, dense arrays, and high throughput represent challenges that are being addressed by current research. An alternative approach uses Langmuir–Blodgett (LB)-type techniques in which nanowires on the water/air interface form nematic liquid crystal type structures under applied pressure.[63] In this process, the surfaces of the nanowires are first modified with surfactant molecules that have hydrophobic heads facing the water. The repulsive interaction between these hydrophobic groups and the water molecules lifts the nanowires to the water/air interface. A force is then applied to squeeze the nanowire film floating on the water surface. Once the surface pressure reaches a critical value, the nanowires rotate perpendicular to the pressure to create aligned arrays. These arrays can be transferred to a target substrate for further applications. In a third approach, electric and/or magnetic fields applied to a drying suspension of wires with suitable response to these external fields create aligned assemblies. For example, the interaction between an induced polarization in a nanowire and an applied electric field tends to align the wire parallel to the field direction.[64] Similarly, applied magnetic fields can concentrate and align ribbons or wires that are coated with a ferromagnetic material (such as Ni).[65] In this case, the Ni stripes can also serve as electrodes for TFT fabrication. Ni can form a silicide with Si to generate ohmic contacts.[66] Although these types of assembled films provide an attractive class of channel material, the throughput, degree of alignment, end-to-end registry, and uniformity must be considered for realistic applications.

A relatively recent report described the use of films of aligned nanowires of p-type Si and nanoribbons of n-type CdS, both synthesized via the VLS process, as semiconductors for TFTs.[67] In this case, passing solutions of these elements through microfluidic channels formed between stamps of poly(dimethylsiloxane) (PDMS) and a device substrate (either hard Si wafers or flexible plastic sheets) created the alignment. Figure 6A shows an image of several pieces of polyetheretherketone (PEEK) sheet (125 μm in thickness) coated with assembled p-type Si nanowire films for integration into TFTs. The inset shows aligned nanowires in the channel region (between the source and drain). Electrical measurements (Fig. 6B and C) indicate good device behavior with threshold voltages of ca. 3.0 V, on/off current ratios $>10^5$, and subthreshold slopes of ca. 600 mV/decade. This performance is maintained in bending tests with bend radii down to ca. 55 mm. Integrating n-type CdS and p-type Si TFTs yields complementary inverters with gains as high as ca. 27. More

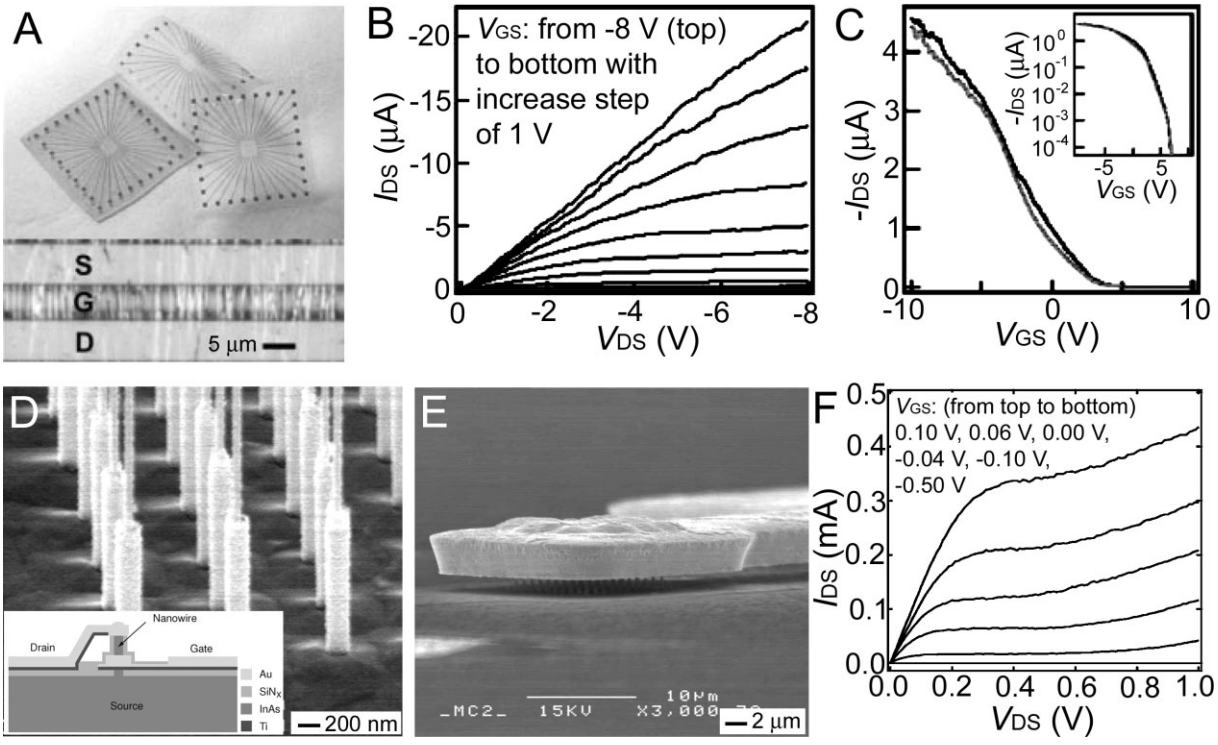

Figure 6. A) Photograph and B,C) electrical characterization of flexible TFTs fabricated with assembled p-type Si nanowires. In this case, a spin-cast layer of 1–2 μm thick SU-8 photoresist on a polyetheretherketone (PEEK) sheet of 125 μm thickness provides a smooth surface for device fabrication. Strips of Cr/Au (10/30 nm) form the gate electrodes, and a 30 nm thick aluminum oxide layer serves as the gate dielectric. Nanowire films are assembled on top of this dielectric. Forming source/drain electrodes of Ti/Au (60/80 nm) completes the fabrication. Adapted with permission from [67]. Copyright 2003 Nature Publishing Group. D–F) Characterization of vertically wrapped nanowire transistors. D) SEM image of nanowire array after forming the wrapped gate. The gate length is ca. 1 μm. The inset shows a schematic layout of transistors with airbridge drain contacts. Only one wire of the matrix of wires is shown here. E) SEM image and F) I_{DS}–V_{DS} characteristics of a typical device. Adapted with permission from [70]. Copyright 2006 IEEE.

complex circuits, such as five-stage ring oscillators fabricated with p-type Si nanowire films on glass substrates and with oscillation frequencies of up to 11.7 MHz (at supply voltages of 43 V), can be achieved with this approach.[68] Although the per-wire mobilities can be high (> 100 $cm^2 V^{-1} s^{-1}$), a disadvantage of these types of devices is their relatively low level of output current per width (determined from the physical dimensions of the devices), which results from the low to moderate coverage (ca. 3–4 %) of nanowires in the channel and their uncontrolled end-to-end registration.

Current levels from nanowire array transistors can be increased by using designs, such as vertical wrap-gated layouts, in which the coverage and registration can be greatly increased compared with the arrays shown in Figure 6A. Devices that use arrays of InAs nanowires with 80 nm diameters (defined by the size of lithographically patterned Au disks) grown epitaxially on appropriate substrates in a chemical-beam-epitaxy (CBE) system represent one example of this type of design.[69] These nanowires can be integrated into transistors (metal-insulator-semiconductor field-effect transistors (MISFETs)), shown in the inset of Figure 6D, by suitable processing. The sequence begins with deposition of 60 nm SiN_x as the insulating layer. Sputtering yields a conformal bilayer of Ti/Au for the gate electrode. Exposing the top portions of the wires by wet-etching creates the structure in Figure 6D. Optical lithography and wet-etching define the gate pads and gate fingers. The fabrication ends with the formation of the drain electrode, connected to the wrapped metal layers around the top portions of the wires by use of an air-bridge technology.[70] Figure 6E shows an SEM image of a typical transistor that incorporates ca. 40 nanowires (i.e., the total cross-sectional area of the channel is ca. 0.2 μm^2, with a corresponding coverage of only ca. 0.6 %). The wire coverage can be increased by increasing the density of the patterned catalysts (e.g., Au disks), resulting in further increases in current. The wafer growth substrate serves as the source electrode. Figure 6F presents the electrical response, which indicates n-type operation in depletion mode. An estimate of the mobility, based on models[71] traditionally used for nanowire transistors, yields ca. 3000 $cm^2 V^{-1} s^{-1}$. Although this vertical geometry naturally incorporates aligned nanowires with good end-to-end registration, integration for the types of macroelectronics applications discussed here requires further development.

6. Films of Nano-/Microstructures Formed From High-Quality Wafers

Single-crystal semiconductor wafers represent exceedingly well-developed forms of materials technology that are, at the same time, commodity items owing to their widespread use in conventional electronics and optoelectronics. The high levels of purity, surface smoothness, the control over crystallinity, doping concentration and type, and the resulting high carrier mobilities match or exceed those that are possible with current versions of growth techniques for films, nanowires, nanoparticles, or nanoribbons. Nanometer- and micrometer-scale structures—e.g., wires, ribbons, platelets, disks, membranes—fabricated from high-quality, bulk wafers can, as a result, provide useful building blocks for high-performance TFTs. This approach was first reported in 2004,[72] and significant advances have been achieved since that time.[73–79] This section discusses some aspects of approaches for generating such structures from bulk wafers and for printing them onto plastic and other substrates. Flexible TFTs and simple circuits fabricated with these printed elements provide examples of the levels of performance that can be achieved.

6.1. Fabrication of Nano-/Microstructures

Single-crystalline nano-/microstructures of semiconductors can be fabricated from conventional wafers (referred to as "mother wafers") of these materials through so-called "top-down" approaches (as opposed to the chemical synthetic "bottom-up" approaches described in the previous section) in which lithographic patterning and etching techniques create the desired structures from the near-surface portions of the mother wafers. Semiconductor elements generated in this manner inherit the high materials quality of the mother wafers, which, in turn, enables excellent electrical properties in devices built with them. Two etching strategies have been exploited to produce these kinds of structures, as illustrated in Figure 7. The most straightforward approach involves isotropic selective etching of sacrificial layers of multilayered wafers to release thin semiconductor structures (see Fig. 7A). Examples include Si structures generated from silicon-on-insulator (SOI) wafers and GaAs structures from GaAs wafers with epitaxial layers of AlAs and GaAs (top surfaces), where lithographic steps followed by removal of SiO_2[72–75,80] and AlAs,[81] respectively, release thin ribbons, platelets, or wires. Figure 7B shows an SEM image of GaAs ribbons with thicknesses of 270 nm, widths of 5 μm, and lengths of up to several centimeters, indicating their mechanical flexibility, dimensional uniformity, and surface smoothness.

A different class of approach uses similar lithographic steps, followed by anisotropic etching along certain crystalline planes to generate ribbons/wires from conventional bulk wafers in a manner that avoids the high costs associated with wafers that have specialized layered structures. Figure 7C depicts a process for generating Si ribbons from a (111) Si wafer. The first step defines shallow trenches with side walls terminated in (110) planes by lithography and reactive ion etching (RIE). Coating the top surfaces and parts of the side walls of the trenches with thin resists of, for example, SiO_2, Si_3N_4, and Au followed by etching in KOH, an etchant with high etching selectivity along the (110) orientation of single-crystalline Si, generates thin ribbons of Si.[76] Figure 7D presents an SEM image of structures fabricated in this manner. Thicknesses between several tens and several hundreds of nanometers can be achieved through appropriate control of the processing pa-

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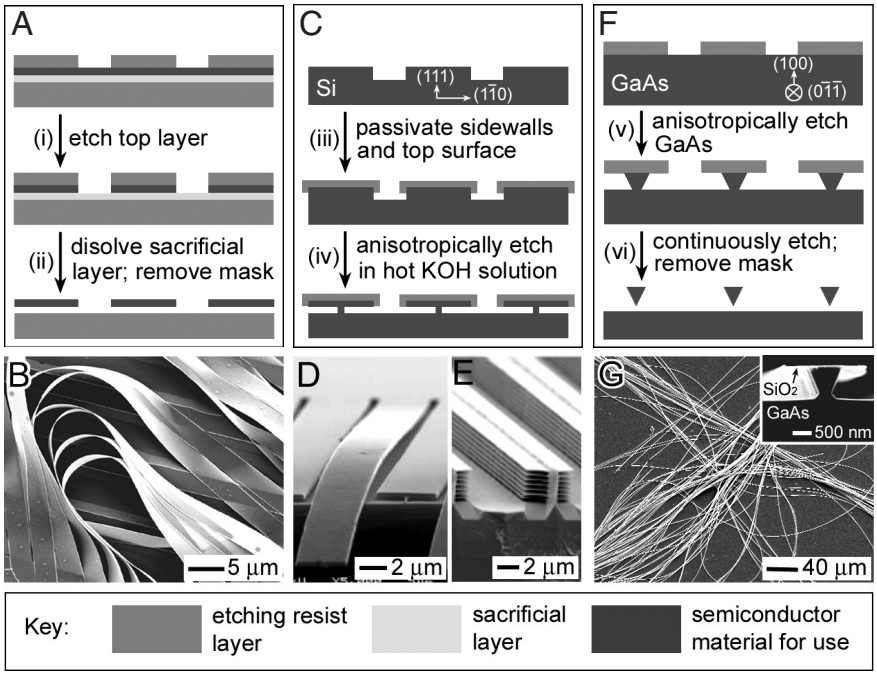

Figure 7. Fabrication procedures (A,C,F) that involve the combined use of lithography and wet chemical etching (and dry RIE etching as well) to generate nano-/microstructures of single-crystalline inorganic semiconductors. SEM images of structures (B) GaAs ribbons, D,E) Si ribbons, G) GaAs wires with triangular cross sections) fabricated using this approach.

rameters. The newly formed surfaces of the ribbons exhibit relatively smooth surfaces, that is, surface roughnesses of 0.5 nm, as determined by AFM analysis. More interesting, controlled ripple structures can be sculpted on the surfaces of side walls when the trenches are formed with specialized inductively coupled plasma (ICP)-RIE etching procedures. Processing such wafers according to the steps shown in Figure 7C produces large quantities of ribbons in the form of multilayer stacks (Fig. 7E).[82] In a related but simpler process, anisotropic etching that yields reverse mesas (i.e., structures with newly formed sidewalls that have an acute angle relative to the original surface of the mother wafer) forms freestanding wires with triangular cross sections. This approach has been applied to III–V compound wafers with top (100) surfaces and zinc blende face-centered cubic lattices. Figure 7F shows GaAs wires formed by anisotropic etching of a GaAs wafer with $1H_3PO_4$ (85 wt %)-$13H_2O_2$ (30 wt %)-$12H_2O$ (*V*/*V*/*V*) with etch mask lines (e.g., photoresist and SiO_2) patterned along the (0$\bar{1}$1$\bar{1}$) crystallographic direction on the surface of a (100) GaAs wafer.[83] Figure 7G presents an SEM image of GaAs wires with widths of ca. 400 nm formed using SiO_2 (50 nm thick) as the etching mask. The curved configurations of the wires indicate their excellent mechanical flexibility. Careful studies show that roughness (ca. tens of nanometers) on the etched surfaces originates from slight edge roughness and angular misorientation of the resist lines together with intrinsic roughness associated with the etching. In many cases, the active devices rely only on the top flat surfaces of the wires, and their performance is not adversely affected by the roughness on the etched sidewalls.

6.2. Dry Transfer Printing of Arrayed Nano-/Microstructures

Nano-/microstructures fabricated via the top-down procedures of Figure 7 can be either dispersed in solvents and then assembled on desired substrates using the types of techniques described in Section 5 or, more effectively, they can be designed to retain the positional and orientational order defined by the lithography process through the use of anchors that tether their ends to the original wafer. These ordered wires/ribbons can then be transfer printed onto desired substrates, including plastic sheets, using elastomeric PDMS stamps as transfer elements. Figure 8A illustrates the steps in this type of printing process.[83a,84] First, placing a piece of PDMS onto the surface of a wafer with patterned patches of wires/ribbons generates, through the interaction of generalized adhesion forces,[85] soft, conformal contact. These adhesion forces (or strong chemical bonds formed with appropriately designed surface chemistries) bond the semiconductor nano-/microstructures to the surface of the PDMS (step i). Peeling the PDMS stamp away from the wafer transfers all of the nano-/microstructures to the stamp (step ii), as the structures break away from the mother wafer at the anchor points. Placing this "inked" stamp against a plastic substrate coated with a thin layer of adhesive (e.g., epoxy resins or photocurable polymers), activating the adhesive (e.g., curing the polymer), and then peeling back the stamp completes the printing (step iii). In a related approach, control of the peel rate enables transfer without adhesives.[86] The printed arrays of semiconductor nano-/microstructures can be processed into TFTs through traditional photolithography and deposition of other materials (e.g., dielectrics and metal electrodes) that are compatible with the plastic substrate. If high-temperature processing (e.g., annealing of ohmic contacts for GaAs,[77] doping of Si,[74] growth of thermal oxides on Si) is required, then those steps can be carried out on the wafer before transfer (or even before fabrication of the nano-/microstructures). By repetitive printing in a step-and-repeat fashion, it is possible to create devices that cover areas on the plastic substrate that are much larger than the size of the mother wafer (see the right column of Fig. 8A).[84] A patterned PDMS stamp (e.g., with patterned posts or with patterned surface chemistries) can pick up wires/

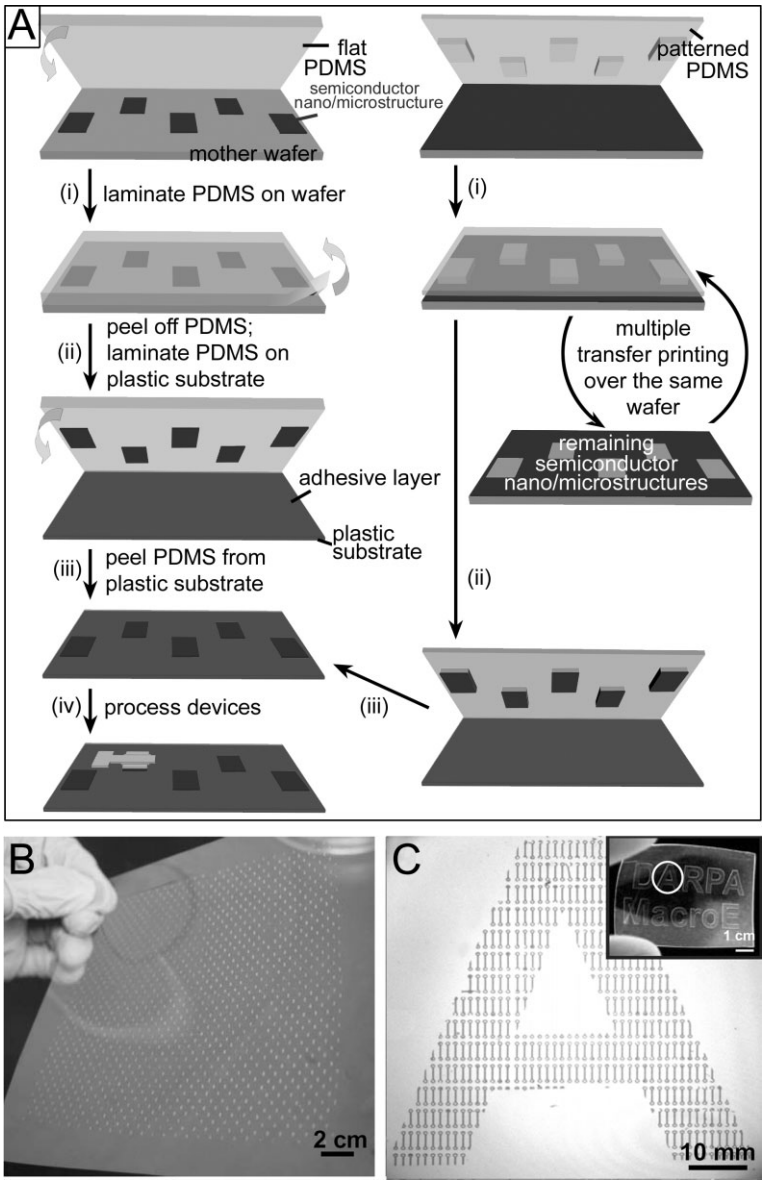

Figure 8. A) Schematic illustration of steps for transfer printing nano-/microstructures generated with the procedures of Fig. 7 onto plastic substrates using PDMS stamps with flat (left column) and patterned (right column) surfaces. The continuous semiconductor layers represent the arrays of wires/ribbons. B,C) Optical images of the patterned patches of arrays of silicon ribbons on polyurethane/PET sheets printed with PDMS stamps through the processes shown in (A). Adapted from [84].

ribbons from selected areas. The remaining nano-/microstructures on the mother wafer can be printed in subsequent steps. Figure 8B shows a PET sheet (15×15 cm^2) covered with patterned patches of Si ribbon arrays, transferred by using an 8×8 cm^2 PDMS stamp multiple times and a mother wafer much smaller than the PET substrate. PDMS stamps can be fabricated with any desired layout by use of soft lithographic casting and curing procedures.[87] For example, the inset of Figure 8C shows a pattern of printed Si ribbons that form the text "DARPA MacroE" constructed using a stamp and a flexible PET substrate. The enlarged image (i.e., the letter 'A') shown in Figure 8C indicates the high fidelity of the printing technique.

6.3. Si TFTs on Plastic Substrates

Printed arrays of single-crystal wires/ribbons can serve as active materials for high-performance electronic devices, for which some, all, or none of the processing is performed on the mother substrate. The ability to separate, in this manner, high-temperature growth and processing from the final device substrate (e.g., low-temperature plastic) is a key feature of this approach. Figure 9A shows an optical image of a polyimide sheet (with a thickness of 25 μm) covered with an array of TFTs fabricated with printed Si ribbons (290 nm thick) where the contact-doped regions are defined on the mother wafer.[75] The adhesive layer for the transfer is a liquid precursor to polyimide, that is, polyamic acid, which is converted into electronic-grade polyimide by baking. The dielectric material is SiO_2 grown by PECVD at relatively low temperature (e.g., ca. 250 °C). Source, drain, and gate electrodes use Cr/Au (5/100 nm) deposited by electron-beam evaporation. Figure 9B and C show a top- and cross-sectional view of an as-fabricated Si-ribbon TFT, respectively. These transistors exhibit electrical behavior similar to that of similar devices fabricated on the mother wafers. Figure 9D presents the source–drain current from a transistor with channel length (L_c) of 9 μm, a channel overlap distance (L_o) of 5.5 μm, and a channel width (W_c) of 200 μm as a function of the drain voltage, for different gate voltages. Figure 9E presents transfer curves from devices with different channel lengths. The mobilities extracted from these types of devices in the linear regimes are as high as ca. 500 cm^2 V^{-1} s^{-1}. Figure 9F presents microwave measurements on a transistor with $L_c = 2$ μm, $L_o = 1.5$ μm, and $W_c = 200$ μm. The f_T is ca. 515 MHz, at gate and drain biases of 2 V. The frequency is, as expected, highly dependent on L_c and L_o. Figure 9G compares the measured (filled) and calculated (open) f_T values for devices with different L_c and L_o, indicating reasonable agreement between them (the measurements do not involve de-embedding). Although higher-frequency operation is possible by reducing L_c and/or L_o, this approach is not attractive for many macroelectronic systems because it requires high-resolution lithography, which can be difficult to achieve in a cost-effective manner on large area, plastic substrates. By contrast, MESFET devices made of GaAs wire/ribbons can offer high speeds even with coarse patterning resolution and limited capacity for overlay registration, the latter of which is of particular advantage for

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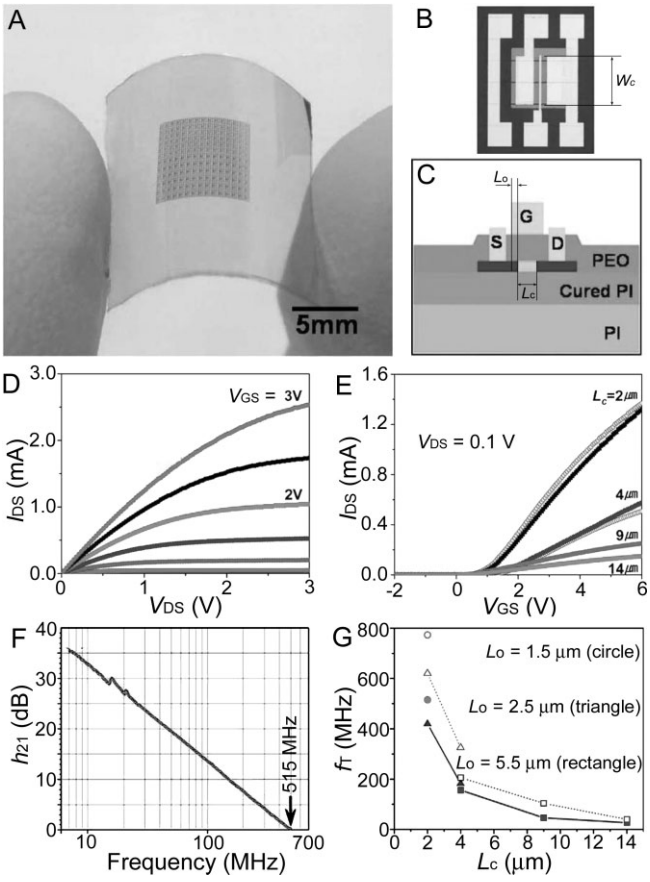

Figure 9. A–C) Images and D–G) electrical characteristics of transistors fabricated with Si ribbons on polyimide substrates. PEO stands for the SiO_2 layer grown by PECVD. Adapted with permission from [75]. Copyright 2006 IEEE.

plastic substrates because they often do not show good dimensional stability over large areas. The next section discusses such devices.

6.4. GaAs TFTs on Plastics

MESFET type TFTs with geometries shown in Figure 10A on plastic substrates can be fabricated with printed GaAs ribbons (or wires) that incorporate integrated ohmic contacts. Figure 10B presents an image of a thin polyurethane sheet (with thickness of ca. 7 μm) with an array of TFTs, fabricated using GaAs ribbons shown in Figure 7B. Each ribbon consists of bilayers of 150 nm semi-insulating GaAs (SI-GaAs) and 120 nm n-GaAs (carrier concentration 4.0×10^{17} cm^{-3}), on which ohmic source–drain electrodes are formed by annealing metal stacks, that is, 70 nm AuGe/10 nm Ni/70 nm Au, at 450 °C for 1 min in an atmosphere of N_2. Schottky gate electrodes are formed by directly depositing 75 nm Cr/75 nm Au. Wrapping these devices around a glass rod with a diameter of 7 mm indicates their level of flexibility (Fig. 10B). The device performance exhibits only a relatively minor change (< ≈ 15 %) with bending. In practice, the mechanical fragility of thin GaAs ribbons (compared to Si ribbons) demands extreme care in the transfer printing. TFTs can also be formed with relatively thick GaAs wires (width of ca. 1–2 μm), which exhibit higher resistance to fracture.[77,78] Figure 10C shows an image of a 2×2 cm^2 PET sheet of transistors formed with ca. 1.8 μm thick GaAs wires. Each device incorporates 10 parallel wires, as shown in the inset of Figure 10C. Figure 10D shows electrical characteristics of a transistor with a gate length of 2 μm. The response is consistent with n-type depletion mode operation of similar MESFETs fabricated on the mother wafer. The inset of Figure 10D presents the transfer curves recorded with different gate voltage sweep directions, illustrating the low level of hysteresis. The on/off current ratios in the saturated regime (i.e., $V_{DS} = 4$ V), as evaluated from averaged measurements on many devices, are ca. 10^6 and the pinch-off voltages in the linear regime (i.e., $V_{DS} = 0.1$ V) are –2.7 V. Although the device mobility was not extracted from these data, the value is expected to approach the intrinsic mobility of GaAs for electrons, that is, ca. 8500 $cm^2 V^{-1} s^{-1}$.

Microwave measurements can be performed on devices that use a layout as shown in the inset of Figure 10E. Each unit of the test structure contains two identical TFTs with gate lengths of 2 μm, channel lengths of 50 μm, and channel widths of 150 μm with a common gate. The corresponding probing pads match the layout of the high-speed probes. The f_T is 1.55 GHz, consistent with a simple calculated result (1.68 GHz).[78] The gate length, of course, plays an important role in determining the operating frequencies of the devices. Figure 10F compares the measured (symbols) and calculated (dashed line) f_T values of GaAs-wire TFTs with different gate lengths and channel lengths of 50 μm on PET substrates. The results suggest that f_T can be increased significantly by reducing the gate length to approach operating frequencies that are suitable for large active antennas operating in the UHF regime, even the S-band.

6.5. Evaluation of the Mechanical Bendability of TFTs on Plastics

Good mechanical bendability is a critical feature of many of the envisioned applications described in the Introduction. The flexibility of transistors fabricated with single-crystalline nano-/microstructures (described in sections 6.3 and 6.4) can be systematically evaluated by squeezing the plastic substrates with specially designed mechanical stages to generate concave (compressive strains on top device surface) and convex surfaces (tensile strains; Fig. 11A). Figure 11B shows, as an example, the variation of the mobility (in the linear regime) of a Si transistor fabricated with Si ribbons on a 25 μm thick polyimide sheet, normalized by the value in the unbent state, with bending radius and surface strain. The results indicate only small changes in device performance in this range of strains.

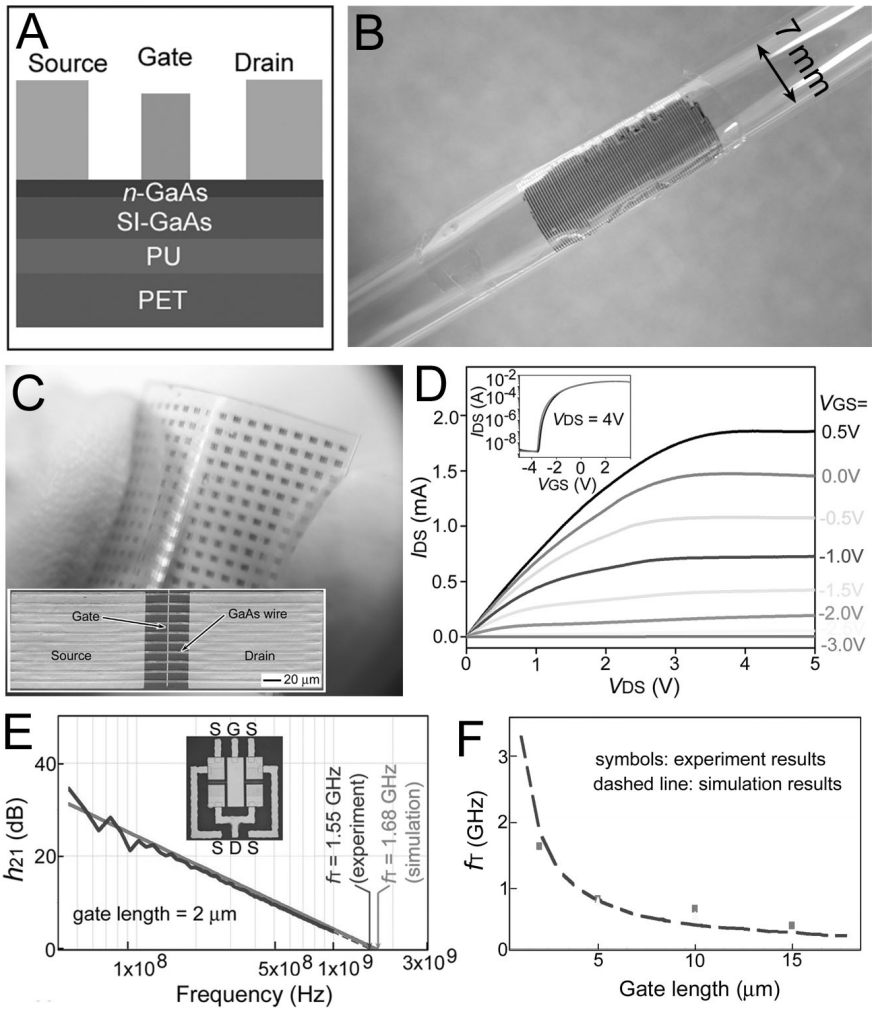

Figure 10. Characterization of MESFET type TFTs on plastics fabricated with GaAs ribbons and triangular wires. A) Schematic geometry of a TFT with GaAs nano-/microstructures on a plastic polyurethane (PU)/PET substrate. B) Photograph of a thin PU film (ca. 7 μm in thickness) that supports an array of GaAs-ribbon TFTs, wrapped on the surface of a glass rod with diameter of 7 mm, indicating the excellent flexibility of these devices. Electrical measurements of these transistors show minor changes in performance after bending. C) Optical image of a 2×2 cm^2 PET sheet with hundreds of devices fabricated with arrays of triangular GaAs wires. The inset is an SEM image of an individual device. D) Direct current and E) microwave responses of the GaAs-wire transistors with gate length of 2 μm and channel length of 50 μm. F) Dependence of f_T on gate length. The different symbols represent measurements on different devices. The dashed line corresponds to calculations. Adapted with permission from [78]. Copyright 2006 American Institute of Physics.

6.6. Flexible Circuits Formed by Integrating TFTs

Individual TFTs of the type described in the previous section can be combined to form functional circuits. For example, integrating GaAs-wire TFTs with gate lengths of 5 μm, channel lengths of 50 μm, and channel widths of 150 μm yields different circuit elements, for example, NOR gates, NAND gates, and inverters.[89] Figure 12A shows a collection of GaAs-wire transistors and simple circuits on a PET substrate, demonstrating the flexibility. The NOR gate circuit shown in Figure 12B (circuit diagram) and C (photographic image), constructed with two identical transistors as switching devices and another transistor with lower current level as a load, exhibits electrical characteristics shown in Figure 12D. In operation, biasing V_{dd} to a positive voltage (5 V versus ground, GND) turns on the load transistor. Turning on either switching transistor (V_A or V_B) by applying a high positive voltage (logic 1) provides a large current flow through the drain of the load transistor to ground, resulting in an output voltage (V_o) at a low level (logic 0). High positive output voltage (logic 1) can be achieved only when both inputs are at high negative voltages (logic 0), which turns off both switching transistors. The dependence of the output on the inputs of the NOR gate is shown in Figure 12D. Similarly, flexible Si MOSFET-type TFTs on plastics can also be integrated into functional circuits. For example, integrating five Si ribbon-based n-type TFTs (as shown in Fig. 9) with channel widths of 200 μm (serving as drivers) and five devices with channel widths of 30 μm (serving as loads) forms a five-stage ring oscillator.[90] When implemented with L_c and L_o of 4 and 2 μm, respectively, and driven at $V_{dd} = 4$ V, the oscillator exhibits a frequency of 8.1 MHz, corresponding to a stage delay of 12 ns. The speed can be further increased by reducing the contact overlaps and channel lengths. Further integration of circuits of the type shown here together with other passive elements (e.g., resistors, capacitors, inductors) offers the promise for high-speed, large-area electronic systems on plastic.

Fatigue studies (i.e., repetitive bending for many cycles, as shown in Fig. 11C) confirm the robustness and durability of these devices. After 2000 cycles of bending (at extreme bending radii of 3 mm) and unbending, the mobility, the V_{th}, and the on/off current ratio of the TFTs change by less than 20 %. Similar evaluations of GaAs-wire TFTs on PET substrates indicate similar behavior.[77,78] Bendability of the systems can be further increased by decreasing the thickness of the substrate and/or by casting or laminating layers of plastic on top of the devices to locate them in the neutral mechanical plane.[88]

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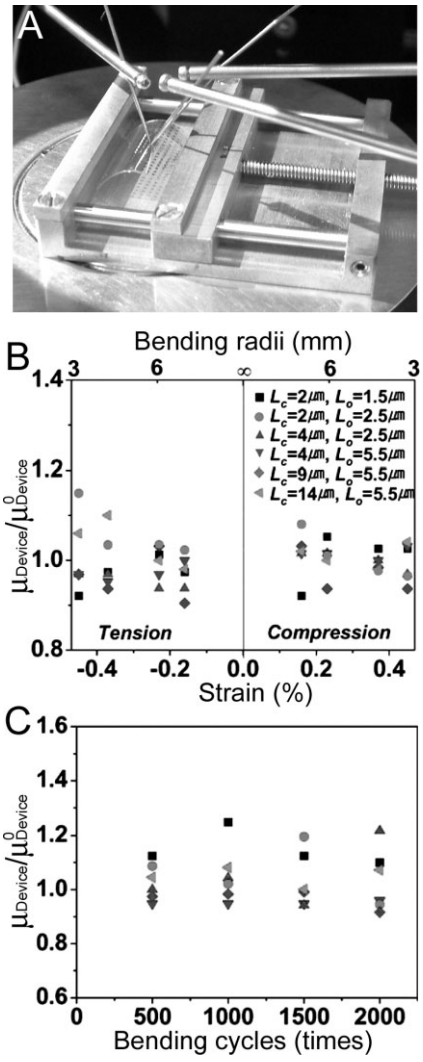

Figure 11. Mechanical characterization of Si ribbon based transistors on polyimide substrates (with thickness of 25 μm). The normalized mobility ($\mu_{device}/\mu_{device}^0$) is plotted as a function of bending-induced strain and bending radius. Adapted with permission from [75]. Copyright 2006 IEEE.

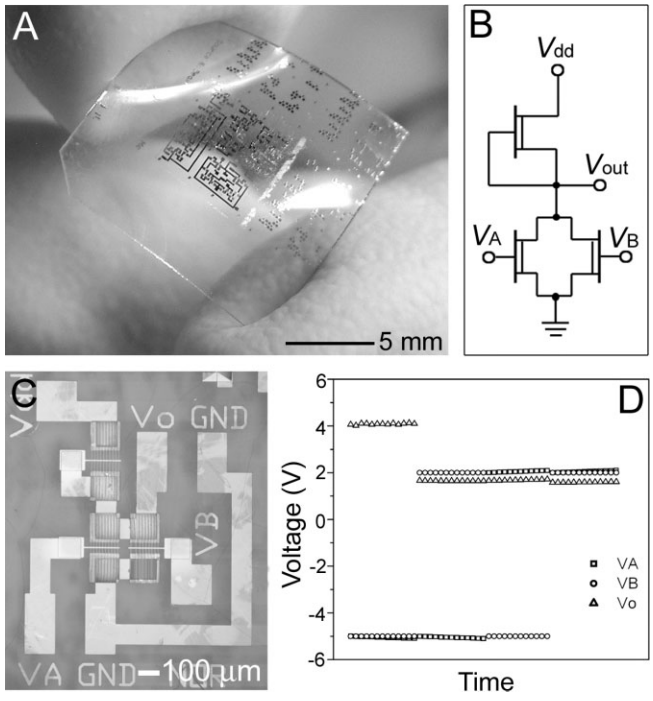

Figure 12. A) Optical image of a bent PET substrate with GaAs-wire based TFTs and various circuits fabricated with these TFTs and GaAs based diodes. B) Circuit diagram, C) optical image, and D) output–input characteristic of a NOR gate fabricated with three TFTs. The load transistor (top in C) has a channel length of 100 μm, while the switching transistors (bottom in C) have channel lengths of 50 μm. The gate lengths of all transistors are 5 μm. Each transistor comprises 10 aligned GaAs wires with width of ca. 2 μm. V_{dd} applied to the NOR gate was 5 V vs. ground (GND). The logic inputs of "0" and "1" were driven by –5 and 2 V, respectively. The logic "0" and "1" outputs were 1.58–1.67 and 4.1 V, respectively. Reproduced from [89].

7. Conclusion and Outlook

As outlined in this Review, a variety of inorganic materials in the form of amorphous, nanocrystalline, microcrystalline, and polycrystalline thin films as well as assembled arrays of nanowires/nanoribbons and nano-/microstructures can yield transistors with high mobilities and simple circuit components with good performance. Many of these materials have the potential to be grown and processed on low-temperature plastic substrates, and in several cases these capabilities have already been demonstrated. TFTs fabricated with inorganic materials on plastics can be operated at high frequencies,[25,75,78] into the ultrahigh frequency (UHF) and *S*-band regimes, allowing them, in principle, to be applied in demanding applications, such as radio frequency communications. In addition, new properties, such as transparency, can be introduced with materials such as the transparent oxides (see section 3), thereby creating new types of application possibilities. Future work will, we believe, focus on the further development of these materials and methods for incorporating them into realistic applications. Issues related to mechanical and electrical properties of interfaces and, in particular, to the semiconductor/dielectric interfaces will be important.

Alternative approaches to these systems involve organic electronic materials, including newer systems such as films of single-walled carbon nanotubes, and directed assembly of preformed circuit blocks. Small-molecule and polymer-based organic semiconductors have the advantage that they are more fully explored for electronic applications than some of the inorganic approaches presented here (e.g., nanowires, nanocrystals), but the modest performance that has, thus far, been possible with them limits the range of applications. Carbon nanotube films, on the other hand, can offer extremely high performance[91–94] and also optical transparency;[95] in addition they have the advantage that they are chemically and mechanically robust compared to most conventional organics. As a result, this class of material appears to have some promise

for macroelectronics. Another route to this type of electronics uses guided fluidic self-assembly of preformed circuit blocks.[96–98] An attractive attribute of this approach is that it exploits fully, well-developed silicon wafer-based circuit technologies. Reaching yields that are high enough to support applications in, for example, information display is challenging. Also, the reliability of interconnects and the mechanical integrity of the interfaces between the circuit blocks and the surrounding material (i.e., adhesives) are uncertain. The advantages and disadvantages of these very different approaches make it difficult to identify a clearly preferred path. Nevertheless, the large number of promising approaches that already exist leads one to be optimistic that low cost, large area, high performance flexible electronics will mature into an important technology with wide-ranging applications.

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Noted added in proof: After this Review was submitted, two papers with direct relevance to the topic were published. New types of flexible transparent TFTs (related to Section 3) were reported with the use of assembled nanowires of In_2O_3 and ZnO on plastic substrates combined with thin layers of high-k Al_2O_3 (formed via atomic layer deposition (ALD)). Typical transistors made of In_2O_3 nanowires on PET sheets exhibited mobilities of 120–167 $cm^2\ V^{-1}\ s^{-1}$.[99] TFTs made of single-crystal Si membranes on PEY substrates were reported to exhibit f_T of 1.9 GHz. These devices have similar fabrication resolution to those reported in [75] (Section 6.3) and special device layouts, such as π-shape, two-finger gates.[100]

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