NANO-TECHNIQUE ALLOWS FOR REFINED PATTERNING
Semiconductor International (Aug. 1) -- In work at the U. of I., researchers used nanoimprint lithography and carbon nanotubes to replicate features with nanometer dimensions. "We were able to demonstrate reliable patterning at the 2nm scale, and even some capability down to 1nm," said John Rogers, a professor of materials science and engineering at U of I.
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HEADLINE: Nanoimprint Lithography: A Contender for 32 nm?

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BODY:

Nanoimprint lithography (NIL) is a viable technology, already in volume production use for fine line patterning in all kinds of applications, including data storage, life sciences, MEMS, biochips, optics and photonics. It's reliable, it works, and it's very cost-effective. As one example, a New Jersey-based company called NanoOpto is using NIL to make a variety of optical components, including wave plates for modifying optical signals in DVD and CD players.1 What's particularly interesting about NIL is its ability to reach incredibly small dimensions. In work at the **University of Illinois** at Champaign-Urbana, researchers used NIL and carbon nanotubes to replicate features with nanometer dimensions.2 "We were able to demonstrate reliable patterning at the 2 nm scale, and even some capability down to 1 nm," said John Rogers, a professor of materials science and engineering at U of I. "These dimensions are comparable to the sizes of individual macro molecules." Figure 1 illustrates nanoimprint's capabilities applied to the semiconductor industry: a finFET transistor fabricated only by ultraviolet (UV) nanoimprint. The gate was aligned within 20 nm on the 19 nm small fin.

The real question for the semiconductor industry, however, is whether NIL will prove to be a viable alternative to extreme ultraviolet (EUV) lithography for the 32 nm device generation and beyond. Thousands of researchers around the world are working hard to make exactly that happen. Results have been extremely promising, and great strides have been made, but it has been an uphill battle

to convince chipmakers that it is a production-worthy process. It's just too different, people have too many questions, and with limited funding, NIL champions have yet to produce the reams of data required to be taken seriously.2 "Give me 10% of the money that you've spent on next-generation lithography and we'll give you an imprint system that will do that job," says Steve Dwyer, vice president, EV Group (Schärding, Austria).

What could possibly change the industry's way of thinking is a new concept. What if, with a little development work, it would be possible to reduce over 100 process steps in the interconnect pattering process? That would lead to huge productivity and cost gains, and be exactly the kind of "disruptive technology" the industry needs to continue to move forward. Add to that all the other advantages of NIL - unlimited resolution, low cost and easy process integration - and the challenges that have yet to be overcome don't seem too daunting (Table 1).

The idea is this: By using multi-level NIL rather than photolithography, an interconnect (trench and corresponding via) layer can be patterned in a single step. When the imprinted material is a functional dielectric material (i.e., low-k dielectric), the number of steps may be greatly reduced. With the eight or more interconnect levels common to today's IC devices, dramatic savings in processing time and cost could be realized. Multi-level NIL also avoids some of the most difficult aspects of current dual damascene processing techniques. Since the two levels are patterned in a single lithography step, it is not necessary to image a second level over the topography of the first level. Alignment of via and trench levels is performed during the mask fabrication step, with all subsequent imprints being close replicas of the mask/template.3

As you will soon see, a major challenge still exists in doing this: New photocurable materials are required for the dielectric and etch barrier. It's hard to imagine the semiconductor industry embracing a new low-k dielectric that requires both UV and thermal curing, but stranger things have happened given the right incentives.

Also, a multi-level template is required, which isn't easy since template/maskmakers are now struggling to reliably create even single-level versions with acceptable tolerances and defect levels, at least for very small dimensions. The advantage of dual damascene structures - at least most of them - is that their dimensions are relatively large. Three-dimensional (3-D) templates can be written and inspected by commercial mask houses. In terms of just two-dimensional (2-D) templates, commercial mask shops have implemented high-resolution write capabilities that have been demonstrated in imprints down to 32 nm half-pitch (HP) and template write feasibility down to 22 nm HP, according to Molecular Imprints Inc. (Austin, Texas).

The nanoimprint process

So what is nanoimprinting? The basic idea involves pressing a stamp or template into a compliant layer, typically a thin monomer or polymer film (such as methacrylate) whose structure can be chemically and/or thermally solidified to retain the pattern from the template. There are a few varieties, which can be loosely divided into hot embossing, molding, and stamping techniques.4 Each has uses in various applications such as data storage and optics, but only one technique is seriously being considered for advanced semiconductor applications: UV-NIL. It is also called SFIL, the standing for step-and-flash imprint lithography; the SFIL acronym is widely used but trademarked

by Molecular Imprints.

"Step-and-flash imprint is the most suited for semiconductor applications," said Hiroshi Ito, a lead researcher at IBM Almaden (and one of the world's foremost experts on chemically amplified resists). "It's a room temperature process, and most compatible with standard lithography technologies."

The SFIL process (Fig. 2) uses photopolymerization of an organosilicon solution through a rigid transparent imprint template (typically the same quartz/chrome material now used for photomasks) to define the pattern topography on a substrate. Typically, the imprinting process is performed over a blanket layer of organic polymer, creating a bilayer structure.

Flood exposure to achieve cure is commonly used in mask aligners, photolithography steppers, and scanners for layer-to-layer alignment, but in NIL, it is a 1:1 process; most lithography tools today are 4:1 reduction steppers (i.e., the features on the mask are 4× larger than what is printed on the wafer).

The use of a low-viscosity UV curing solution allows imprinting at room temperature with minimal applied pressure. UV curable materials are selected on the basis of a mixture of pre-polymers, photo initiator and solvents, and can be spin-coated or, as in the case of Molecular Imprints, dispensed by droplets. "The ideal UV-resist material must exhibit a high UV sensitivity (to minimize the exposure time and consequently to increase the throughput), but should also exhibit a good adhesion to silicon (and silicon dioxide) substrate and rather weak adhesion to the template surface in order to ease its separation," noted Jumana Boussey of LTM, a French research lab.

"The UV-curing solution or etch barrier formulation in the normal SFIL process serves the same role as that of a photoresist in a bilayer type process," noted Grant Willson, professor, University of Texas (Austin, Texas). But of course, unlike normal photoresist processing where material that has not been cross-linked through exposure is removed in a subsequent development process, the pattern in NIL is created by the molding of the material by the template.

One trick to accurately transferring the pattern from the etch barrier into the transfer layer is to keep the residual layer thin at the bottom of the trenches. "If the residual layer is very thick, it's a big problem," said Ito. The thicker the residual layer, the greater the erosion of high features.

"A large amount of silicon is incorporated, which acts as an oxygen RIE [reactive ion etch] barrier and allows production of a high-aspect-ratio image derived from the anisotropy of the oxygen RIE," said Willson. There is also an inverse tone version of the process that does not incorporate silicon and offers distinct advantages for certain layers, he added.

This removes the need to imprint high-aspect-ratio features, since the pattern-aspect ratio can be subsequently amplified by dry etching. Because the pattern is imprinted into the etch barrier, then into the transfer layer, and finally the wafer, the aspect ratios of the transfer layer do not have to be very big - as small as 2:1 - thereby minimizing the thickness of the UV-curing film. Through etch amplification, aspect ratios can then be made at up to 10:1.

Another trick to the process is the release layer that enables the template to come free of the cured material. Several approaches are under development. At CEA-Leti, researchers are looking at liquid and vapor phase deposition techniques and measuring the stability of the monolayer, life duration, measurement of the adhesion force, etc. Molecular Imprints uses a proprietary fluorinated material.

3-D Nanoimprinting

For dual damascene applications, two different process flows are under development. In the easiest, the material that is imprinted is a sacrificial etch barrier designed to have the same etch rate as a chemical vapor deposition (CVD) low-k dielectric. "One produces the wire and via in a single imprint step and then transfers the 3-D structure in the planar CVD dielectric by RIE. This is analogous to the 'SLAM process' Intel uses to wire its chips, except it saves many litho and etch steps," said Willson.

In the second version of the process, a dielectric is imprinted that stays on the chip. "That removes still more steps but requires qualification of a new material that stays in the device. That takes time and effort, but we are making good progress toward the materials goals," said Willson.

One of the promising material systems under investigation is based on silsesquioxane: The polyhedral oligiomeric silsesquioxane (POSS) cage structure is particular interesting as a starting material. The cage's corners may be functionalized with a wide variety of reactive groups that can either undergo photochemistry or thermal curing to produce solid resins. Each POSS cage may also be functionalized with multiple groups to help meet different requirements, such as photo-curing speed or overall mechanical strength.3 Research in Willson's group, for example, starts with the POSS cage and adds methacrylate and benzocyclobutene (BCB). Willson explains how this works: "The acrylate makes the system photosensitive, but the acrylic linkage is not thermally stable, has a high dielectric constant, and shrinks when photopolymerized. Luckily, the acrylic section is lost during the high-temperature bake and can produce porosity, which lowers the dielectric constant. The BCB cures to stabilize the mechanical properties in a post-exposure bake step. It does not shrink due to the ring opening nature of the polymerization, and it produces thermally stable linkages. We use the minimum of acrylate functionality to provide a stable structure after photopolymerization. The images do not flow upon cure of the BCB. The ratio of acrylate to BCB required seems to be about 3:5."

The properties of an ideal photo-curable dielectric material are listed in Table 2. One of the biggest challenges here is to obtain a low viscosity. "The viscosity of the formulations we have had to work with to date is at least 10× higher than we would like," Willson said. "Very recently, we have seen some samples with viscosity low enough to be dispensed by inkjet devices, but the data are very preliminary. We are working on implementation of hardware that enables dispensing controlled droplets of more viscous materials and continuing to work on the structure of the POSS materials to try to lower the viscosity."

In work at Sematech, Jeff Wetzel, manager of the emerging technologies group at Advanced Technology Development Facility (ATDF), reports that they are integrating candidate materials from Willson's group and also evaluating potential issues along the lines of adhesion, mechanical

strength and thermal stability. "These are material characteristics that one would look at to ensure compatibility with a standard process line," Wetzel said.

The collection of SEM photos shown in Figure 3 illustrates the potential of the technology. They were produced by Willson's group of Longhorns at the University of Texas in Austin and Sematech's ATDF.

The template challenge

Michael Lercel, directory of lithography at Sematech, sees the advantages of a dual damascene NIL process, but notes that the template requirements could present a major challenge: "It is quite fascinating that you could use it for that technique [dual damascene], and anything you do to reduce the large number of steps in semiconductor process flow is highly desirable. You still have to make a very difficult two-level template and control defects and overlay to make that successful. What you do is actually move some of the process complexity from the wafer up to the template, which could be a good thing, but you need a viable template manufacturing process for that to be successful."

Lercel recently compared nanoimprint template requirements with optical mask requirements and noted that because NIL uses a 1× template, the target dimensions are one-fourth the size (of 4× masks/reticles used for EUV). "That's going to put a huge burden on the mask patterning capabilities and especially defect sizes. Nanoimprint is so good at printing what's on the template; you have to be very careful that there are no defects on the template. That's going to be a huge challenge. Already the photomask industry is so stretched by the challenges of trying to meet the very fast roadmap for semiconductor processing; putting nanoimprint in effectively advances the clock by a couple of years."

William M. Tong, a researcher at Hewlett-Packard, added, "The two perceived disadvantages for nanoimprint templates are EBL [e-beam lithography] resolution and defects. For EBL, nanoimprint templates do not require the use of OPC, phase shifting, or other RET features that drive up the EBL cost, so there actually will be saving in this area. For defects, while the inspection limit will have to improve 4×, the template surface is 'cleaned' every time an imprint is made. This self-cleaning property is unique to nanoimprint and could actually drive the cost down," said Tong.

Conclusion

Although technical challenges still need to be solved in terms of defectivity, alignment and overlay registration, results to date are promising. NIL is on Intel's roadmap, with a scheduled introduction in 2009, and was included for the first time in the latest International Technology Roadmap for Semiconductor (ITRS). It is also the focus of a new Medea+ program called FANTASTIC that is about to be launched. Led by CEA-Leti, it will include IC manufacturers STMicroelectronics, Infineon and Philips, with this mandate: "The FANTASTIC project will close the gaps and generate convincing data by precise and comprehensive analysis and a complete assessment for integration of this technology into the 32 nm CMOS node fabrication."

What could most catch the industry's attention is the potential of 3-D patterning, particularly for dual damascene interconnect structures.

Table 2. Photocurable Dielectric Material Requirements

Property/Characteristic	Requirement
Low viscosity	<20 cP
Photocurable	Chain reaction polymerization
Cure shrinkage	<15%
Dielectric constant	k?3
Thermal stability	<1% wt loss/hr @ 400°C
Mechanical properties	Young's modulus ?4 GPa
CTE	<30 ppm/°C
Water absorption	<1% wt

When you contact any of the following manufacturers directly, please let them know you read about them in Semiconductor International.

EV Group	www.evgroup.com
Hewlett-Packard	www.hp.com
Molecular Imprints Inc.	www.molecularimprints.com
Nanonex	www.nanonex.com
Obducat	www.obducat.com
SUSS Microtec	www.suss.com
Vistec Semiconductor Systems	www.vistec-semi.com

Table 1. Step-and-Flash UV Nanoimprint Lithograhy

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Advantages

Capable of extremely small geometries - potentially the only technique viable for 16 nm generation and beyond.

Some work underway for EUV, such as mask cleaning, could be applied to NIL.

Less expensive: $5M for NIL tool vs. $40M for EUV stepper.

Process integration: Imprint will integrate into the fab just like optical lithography, including track processing. Imprint materials will etch similarly to photoresists and etch processes have been developed to use industry-standard etch tools.

Capable of producing 3-D structures in one step, such as the vias and channels in dual damascene.

This would eliminate process steps and reduce manufacturing costs.

Applications in data storage, life sciences, optics and other industries will help advance equipment and template development and overall infrastructure.

Commercial tools are available from a variety of suppliers, including EV Group, Molecular Imprints, Nanonex, Obducat, and SUSS Microtec.

Research, although small in comparison to EUV efforts, has been underway for years around the world, with promising results.

It is included in the International Technology Roadmap for Semiconductors (ITRS).

A consortium of supplier companies exists (mostly European) focused on commercialization/development of templates, resists, processes, equipment, and metrology. Called Nilcom, more information can be found at www.nilcom.org .

Medea+, a cooperate R&D program in Europe, is about to launch a two-year program called FANTASTIC, aimed at providing the manufacturability of the technology. Led by CEA-Leti, it will include major IC manufacturers STMicroelectronics, Infineon, and Philips. For more information, www.medeaplus.org .

Disadvantages

Fundamental shift from traditional lithography.

Must compete with alternative next-generation lithographic (NGL) concepts, including EUV, maskless lithography and e-beam (direct write or projection).

Limited funding: Most industry funding is not going to EUV lithography.

Production worthiness yet to be demonstrated for advanced semiconductor applications.

Advances still required in overlay registration, alignment and defectivity.

Templates (quartz/chrome blanks patterned by e-beam) are expensive and time-consuming to produce, and must be near perfect. Metrology advances are required to adequately inspect/measure them.

Potential problems with die at the edges of the wafer.

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