Mechanically flexible thin-film transistors that use ultrathin ribbons of silicon derived from bulk wafers

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This letter introduces a type of thin-film transistor that uses aligned arrays of thin (submicron) ribbons of single-crystal silicon created by lithographic patterning and anisotropic etching of bulk silicon (111) wafers. Devices that incorporate such ribbons printed onto thin plastic substrates show good electrical properties and mechanical flexibility. Effective device mobilities, as evaluated in the linear regime, were as high as 360 $cm^2\ V^{-1}\ s^{-1}$, and on/off ratios were $>10^3$. These results may represent important steps toward a low-cost approach to large-area, high-performance, mechanically flexible electronic systems for structural health monitors, sensors, displays, and other applications. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2206688]

Confinement-related properties and broadly usable form factors make low-dimensional materials interesting for new applications in electronics, photonics, microelectromehanical systems (MEMS), and other areas. For example, high-performance mechanically flexible electronic devices can be constructed using micro/nanowires, ribbons, or tubes that are cast,[1–3] painted,[4] or printed[3,5–11] onto plastic substrates. Thin, high aspect ratio material structures allow bendability[6–8] and, in certain structural forms, stretchability[11] in single-crystalline semiconductors that are inherently fragile in bulk. As a result, these types of semiconductors offer intriguing alternatives to vacuum and solution processable poly/noncrystalline organic materials, which usually display significantly lower performance in terms of carrier mobility.[12] Recently described top-down methods[5–11] generate semiconductor wires, ribbons, and sheets from wafer based sources of material. These techniques provide a high level of control over the geometry, spatial organization, and composition of the resulting structures. The economic attractiveness of this approach, however, especially for applications that demand large-area coverage, is limited by the per-area cost of the wafers.

In this letter we report a type of thin-film transistor (TFT) that uses aligned arrays of silicon ribbons with submicron thicknesses derived from low-cost bulk Si (111) wafers. We begin with a description of the procedures for fabricating these structures and transfer printing them onto plastic substrates via elastomeric stamps. We present structural characterization of the shapes of the ribbons, their thicknesses, and surface morphologies. Electrical measurements made on Schottky barrier TFTs formed with these printed ribbons exhibit *n*-type field effect mobilities of 360 $cm^2\ V^{-1}\ s^{-1}$ and on/off ratios of 4000.

Figure 1 illustrates a top-down method that generates thin ($<1\ \mu m$) ribbons from a Si (111) wafer (Montco, Inc., *n*-type, 0.8–1.8 Ω cm). The process begins with near-field phase shift photolithography[13] followed by metal lift-off and SF_6 plasma etching [Plasmatherm reactive ion etching (RIE) system, 40 SCCM (SCCM denotes cubic centimeter per minute at STP) SF_6, 30 mTorr, 200 W rf power for 45 s] to produce an array of ~1 μm deep, 1 μm wide trenches in the Si wafer [Fig. 1(a)]. The spacing between the trenches defines the width of the ribbons (generally 10 μm). Next, 100 nm of thermal oxide is grown on the wafer at 1100 °C. Angled electron beam evaporation of Ti/Au (3/30 nm) provides partial coverage of the trench sidewalls [Fig. 1(b)]. The conditions of the trenching etch and the angle of evaporation control the extent of "shadowing" during angled evaporation and, therefore, the ribbon thickness. A CF_4 plasma etch (40 SCCM CF_4, 2 SCCM O_2, 50 mTorr base pressure, 150 W rf power for 5 min) removes exposed oxide. Finally, a hot KOH solution [3:1:1 H_2O:KOH:IPA (isopropyl alcohol) by mass, 100 °C] undercuts the ribbons. This type of anisotropic etching has been used previously to produce freestanding MEMS structures.[14–16] The etch front advances in the ⟨110⟩ directions while preserving the (111) planes [Figs. 1(c) and 1(d)] and produces freestanding ribbons that cover a large portion (75%–90%) of the original wafer. The etch mask is designed to leave each of the ribbons anchored to the wafer at the ends of the trenches [Figs. 2(a) and 2(d)]. Removing this mask with KI/I_2 (2.67/0.67 wt %) in water followed by HF completes the fabrication. Ribbons generated in this manner are thin, flat, and mechanically flexible [Fig. 1(e)], similar to those produced using previously described approaches with expensive silicon-on-insulator wafers.[5–7,11] Atomic force microscopy [Fig. 3(a)] shows that the thickness ranges from ~115 to ~130 nm across a typical ribbon (trench width and depth of 750 nm and 500 nm, respectively, evaporation angle of 60° from normal to wafer). These variations show up as slight color variations in optical micrographs [Fig. 2(e)]. The roughness as measured by atomic force microscopy (AFM) of a $5\times5\ \mu m^2$ region of the underside of a thicker (550 nm) ribbon, displayed in Fig. 3(b), is 0.5 nm. This value is larger than the top polished surface (0.12 nm) or the underside of a ribbon generated from a silicon-on-insulator (SOI) wafer[5–7,11] (0.18 nm) measured by the same methods. The source of the thickness variations, lateral width variations, and, to a lesser extent, the roughness is partly the edge roughness in the trenches, which in turn

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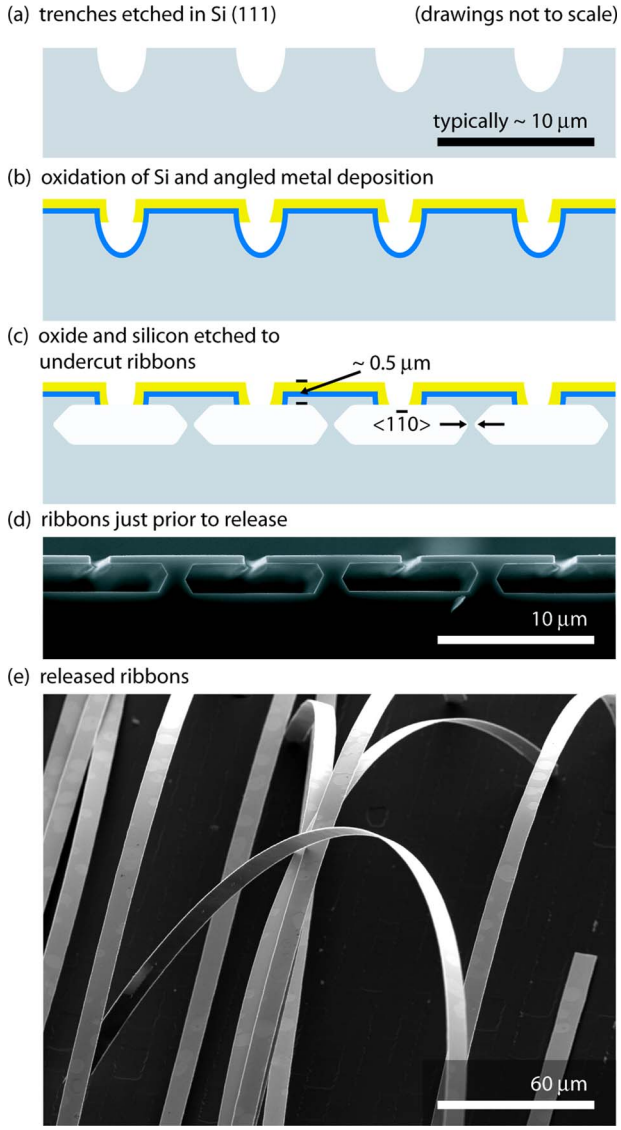

FIG. 1. (Color online) Schematic process flow of single-crystal silicon ribbon fabrication. (a) SF_6 plasma etch trenches in a (111) Si surface. (b) Thermal oxidation and angled evaporation of Ti/Au passivate the sidewalls. (c) Hot KOH/IPA/H_2O solution undercuts the Si ribbons. (d) Cross-sectional SEM image of partially undercut ribbons. (e) Released, flexible ribbons.

causes roughness in the sidewall passivation during angled evaporation. As we show in the following, however, transistor devices with good performance can be constructed with ribbons fabricated using the procedures described here.

The ribbons can be transferred to another (flexible) substrate via a high (>95%) yield printing process, as outlined in Fig. 2. To perform the printing process, a polydimethyl siloxane (PDMS) stamp is laminated against a wafer that supports freestanding ribbons anchored to the wafer at their ends [Figs. 2(a) and 2(d)]. The stamp is then peeled back quickly to retrieve the ribbons. This type of process relies on kinetic control of adhesion to the stamp.[10] The stamp, thus "inked," [Figs. 2(b) and 2(e)] can print the ribbons by contact to another substrate. Ribbons printed onto an indium tin oxide (ITO)-coated 0.2 mm thick polyethylene terephthalate (PET) substrate can be used to make high-performance flexible bottom-gate TFTs on plastic with ITO as the common gate electrode. A layer of epoxy (SU-8, Microchem) freshly deposited onto the ITO gate immediately prior to printing

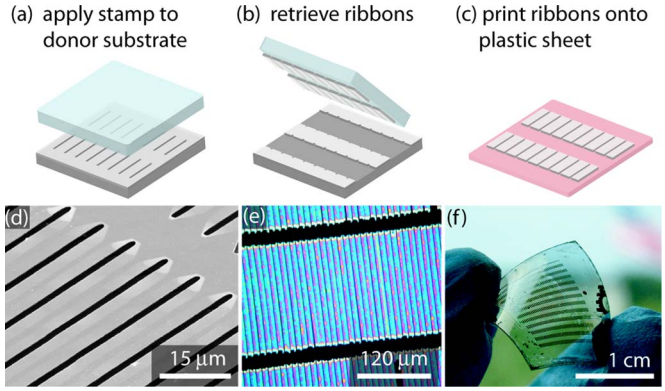

FIG. 2. (Color online) Schematic process flow for transferring silicon from a "donor" wafer to a plastic substrate. (a) A PDMS stamp laminates against a chip with undercut ribbons that are anchored to the wafer. (b) Ribbons bond to the stamp and can be removed from the wafer by peeling away the stamp. (c) Ribbons are then printed from the stamp to a plastic substrate. (d) SEM image of near-completely-undercut ribbons anchored to the donor wafer. (e) Optical micrograph of ribbons removed from the donor and adhered to the stamp. (f) Photograph of a flexible plastic "chip" that houses TFTs made from transferred silicon ribbons.

serves as a gate dielectric and a glue to facilitate ribbon transfer.[6] During printing, the stamp is joined to the PET, and the ribbons sink into SU-8 such that their tops are flush with the surface of the glue. After 1 min on a warm (70 °C) hot plate, the stamp and PET substrate are separated manually, leaving the ribbons attached to the PET. Scratching a transfer-printed sample with a scribe exposed the ITO-SU-8 and SU-8-Si interfaces, allowing the dielectric thickness ($\sim 2\ \mu$m) to be determined by AFM. Thick ($\sim 0.2\ \mu$m) Ti pads contacts defined by photolithography (100 μm length $\times 100\ \mu$m width, spanning ten ribbons) and wet etching with HF/H_2O_2 form Schottky barrier contacts for the source and drain electrodes. These bottom-gate devices display characteristic *n*-type enhancement mode metal-oxide-semiconductor field-effect transistor (MOSFET) gate modulation (see Fig. 4). Transistors achieved on/off ratios of $\sim 10^3$ with device-level mobilities, as determined using standard equations for the operation of MOSFETs,[17] as high as $\sim 360\ cm^2\ V^{-1}\ s^{-1}$ (linear) and $100\ cm^2\ V^{-1}\ s^{-1}$ (saturation, evaluated at a source-drain bias, V_d, of 5 V). The mobility of the ribbons themselves should be about 20% higher than the device level mobility[$440\ cm^2\ V^{-1}\ s^{-1}$ (linear) and $120\ cm^2\ V^{-1}\ s^{-1}$ (saturation)], since they fill only about 83%

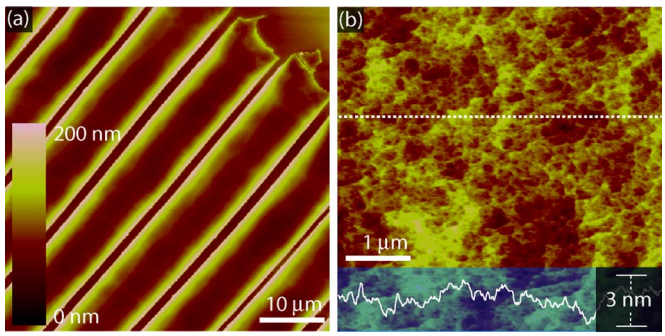

FIG. 3. (Color online) Atomic force microscopy of silicon ribbons generated by anisotropic wet etch undercut. (a) AFM height image of ribbons on a PDMS stamp, with the underside exposed. Ribbons are 115–130 nm thick, as measured at their edges, and bow downward in the middle. (b) AFM image of the underside of a 550-nm-thick ribbon revealing nanoscale roughness introduced by the KOH/IPA/H_2O undercut.

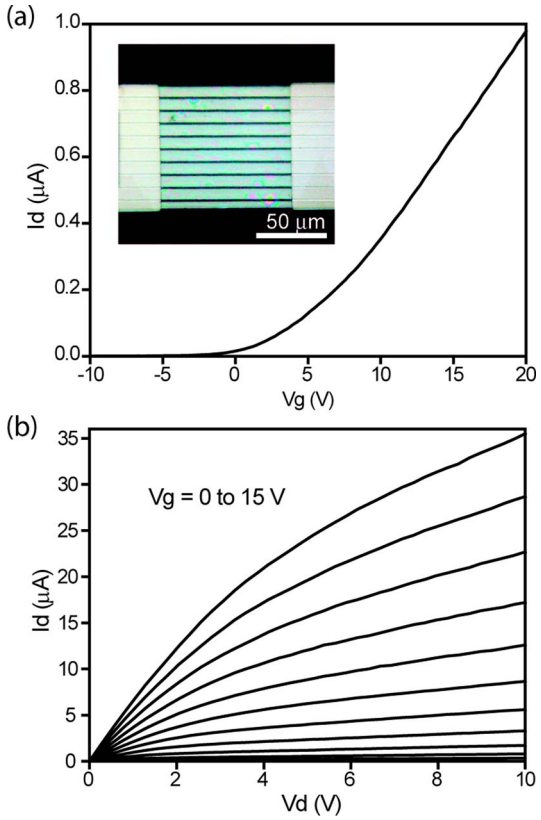

FIG. 4. (Color online) Electrical characterization of a single-crystalline silicon bottom-gate transistor on a PET/ITO substrate; $L=100\ \mu$m, $W=100\ \mu$m, linear mobility $=360\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$, saturation mobility $=100\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$. (a) Transfer characteristics ($V_d=0.1$ V) ratio with inset top view of a device. The on/off current for the transfer characteristics is >4000. (b) Current-voltage (I-V) characteristics.

of the channel. The effects of the Schottky contacts on the device behavior can be significant.[7] The ribbon devices survive when the substrate is bent to modest (15 mm) radii but degrade seriously at sharper (5 mm) bends for the 0.2 mm thick substrates that were used.

In summary, this letter demonstrates a high-yield fabrication strategy for producing printable single-crystal silicon ribbons from a bulk silicon (111) wafer. Refinishing the bulk wafer's surface after fabrication might make multiple repetitions possible, producing tens or even hundreds of square feet of ribbons from 1 $\mathrm{ft^2}$ of starting material. TFTs made from these ribbons on plastic demonstrate their use as high-performance flexible semiconductors. These devices and the strategies to fabricate them could be useful not only for large-area flexible electronics but also for applications that require three dimensional or heterogeneous integration or other features that might be difficult to achieve using conventional silicon microfabrication approaches.

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