

Bulk Quantities of Single-Crystal Silicon Micro-/Nanoribbons Generated from Bulk Wafers

Heung Cho Ko, Alfred J. Baca, and John A. Rogers*

Department of Materials Science and Engineering, Department of Chemistry, Beckman Institute for Advanced Science and Technology, and Frederick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

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ABSTRACT

This Letter demonstrates a strategy for producing bulk quantities of high quality, dimensionally uniform single-crystal silicon micro- and nanoribbons from bulk silicon (111) wafers. The process uses etched trenches with controlled rippled structures defined on the sidewalls, together with angled evaporation of masking materials and anisotropic wet etching of the silicon, to produce multilayer stacks of ribbons with uniform thicknesses and lithographically defined lengths and widths, across the entire surface of the wafer. Ribbons with thicknesses between tens and hundreds of nanometers, widths in the micrometer range, and lengths of up to several centimeters, can be produced, in bulk quantities, using this approach. Printing processes enable the layer by layer transfer of organized arrays of such ribbons to a range of other substrates. Good electrical properties (mobilities $\sim 190 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, on/off $>10^4$) can be achieved with these ribbons in thin film type transistors formed on plastic substrates, thereby demonstrating one potential area of application.

Introduction

Nanostructured elements of single-crystal silicon, in the form of wires, ribbons, and particles, are of interest for a number of applications in electronics, optoelectronics, sensing, and other areas. The ribbon geometry is important for certain devices because it provides, for example, large planar surfaces for chemical sensing and photodetection, and geometries that can efficiently fill the channel regions of transistors. Growth techniques related to the well-developed chemical synthetic approaches used for silicon nanowires¹ have been adapted and applied with some success to produce Si nanoribbons.² The levels of dimensional control and yields of ribbons provided by these procedures and similar ones for materials such as oxides (ZnO, SnO₂, Ga₂O₃, Fe₂O₃, In₂O₃, CdO, PbO₂, etc.),³ sulfides (CdS, ZnS),⁴ nitride (GaN),⁵ and selenides (CdSe, ZnSe, Sb₂Se₃)⁶ are, however, modest. By contrast, approaches that rely on the lithographic processing of top surfaces of semiconductor wafers enable well-controlled thicknesses, widths, lengths, crystallinity, and doping levels. These methods can form membranes, tubes, and ribbons, with thicknesses in the micrometer to nanometer range, composed of Si, SiGe, bilayered Si/SiGe, GaAs, GaN, and others.^{7–12} Furthermore, various processes can transfer these elements, in organized arrays, to other substrates for

device integration. This “top down” approach has three main disadvantages compared to the growth techniques. First, elements with widths less than $\sim 100 \text{ nm}$ are difficult to fabricate, due to practical limitations in the lithography. Second, only those materials that can be grown in thin film or bulk wafer form can be used. Third, and most significant for many applications, the production of bulk quantities of micro-/nanostructures requires large numbers of wafers, each of which can be expensive. The first disadvantage is irrelevant to the many applications that do not require structures with such small dimensions. The second does not, of course, apply to many important materials, including silicon. This paper presents results that address the third limitation. In particular, it introduces a simple method for generating large numbers of high-quality Si ribbons, with thicknesses down to tens of nanometers, from standard bulk Si wafers, in a single processing sequence. Briefly, the approach begins with controlled deep reactive ion etching of silicon wafers through an etch mask to produce trenches with well-defined rippled sidewall morphologies. A collimated flux of metal deposited at an angle onto these ripples creates isolated metal lines that act as masks for highly anisotropic wet etching of the silicon along planes parallel to the surface of the wafer. This single etching step creates bulk quantities of silicon ribbons in multilayer stacked geometries. These ribbons can be removed from the wafer

* Corresponding author. E-mail: jrogers@uiuc.edu. Tel: 1-217-244-4979. Fax: 1-217-333-2736.

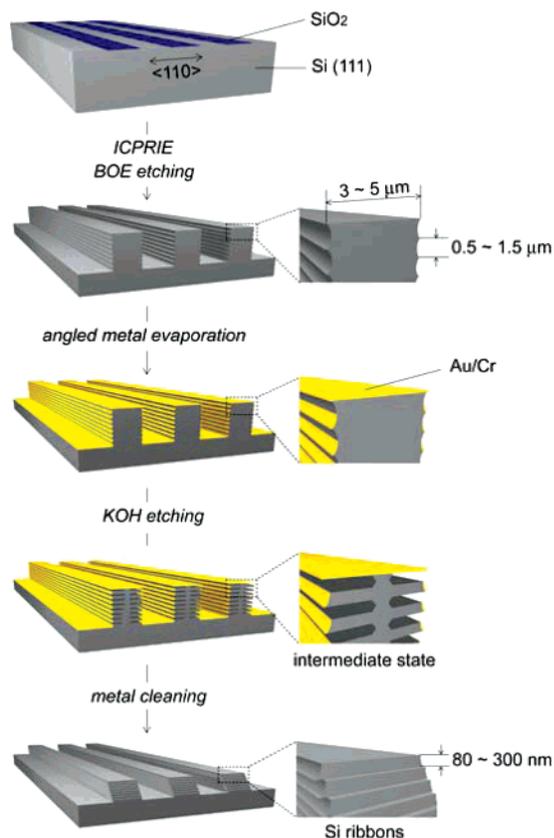


Figure 1. Schematic illustration of steps for fabricating bulk quantities of single-crystal silicon micro-/nanoribbons, in multilayer stacked configurations, from a conventional bulk Si(111) wafer. The process exploits the combined use of specialized etching procedures to generate trenches with sculpted sidewalls, shallow angle directional physical vapor deposition, and anisotropic wet chemical etching. The dashed boxes on the left illustrate the zoomed regions that appear on the right. BOE stands for buffered oxide etchant.

and solution cast or dry transfer printed onto desired substrates, with or without preserving their lithographically defined spatial order, for integration into devices such as transistors. This approach relies only on standard cleanroom processing equipment. As a result, it can be useful to researchers with interest in silicon micro-/nanostructures but without the specialized growth chambers and recipes needed to create them in large quantities using direct synthetic techniques.

Figure 1 presents a schematic illustration of the fabrication sequence. In the first step, dry thermal oxidation at 1100 °C for 2 h produced a thin (~150 nm) layer of SiO₂ on the surface of the wafer. After coating an adhesion promoter, 1,1,1,3,3,3-hexamethyldilazane (HMDS, Acros Organics), contact mode photolithography (Shipley 1805 photoresist (PR) and MF-26A developer) followed by annealing at 110 °C for 5 min provided a PR mask. Wet etching in a buffered oxide etchant (BOE, Transene Co.) solution for 1 min 30 s and cleaning the residual PR in acetone generated lines of SiO₂ on the wafer. These lines provided masking layers for inductively coupled plasma reactive ion etching of the silicon (STS-ICPRIE, STS Mesc Multiplex Advanced Silicon Etcher). The lines were oriented perpendicular to the <110> direction

as shown in Figure 1, such that the sidewalls of the etched trenches exposed the {110} planes. ICPRIE tools are principally designed to produce high aspect ratio structures and flat, vertical sidewalls by use of alternating cycles of etching the silicon and depositing a fluoropolymer to protect the sidewalls against the etch.¹³ We instead modified the process cycles to sculpt well-controlled rippled structures of relief into these sidewalls, through suitable control of gas flow rate, electrode power, chamber pressure, and etching cycle duration (See Supporting Information). Ripples with periods and amplitudes in a range of 80 nm to 1.5 μm and 50–450 nm, respectively, could be achieved reproducibly and uniformly over the processed areas (4 in. wafer size). As an example, parameters that produced periods and amplitudes of 540 and 130 nm, respectively, were as follows: gas flow, O₂/SF₆ = 13/130 sccm (cubic centimeter per minute at STP) for etching and C₄F₈ = 110 sccm for deposition; gas pressure, 94 mTorr; etching power, 600/12 W for inductive coupled plasma (ICP)/platen (P); deposition power, 600/0 W for ICP/P; etching duration, 7 s; deposition duration, 5 s. The etching conditions between the deposition cycles define these ripple structures. Because the SF₆/O₂ mixture gives nearly isotropic etching, the amplitudes and periods of the ripples are related. The smallest ripple structure has a period of 80 nm with an amplitude of 50 nm; the largest has a period of 1.5 μm and an amplitude of 450 nm. Immersing the etched samples in NH₄OH/H₂O₂/H₂O = 1:1:5 at 100 °C for 10 min removed the fluoropolymer on the sidewalls (see Supporting Information). Dipping the sample in a BOE solution for 2 min followed by rinsing in deionized water removed the residual SiO₂ layer. Next, angled electron beam evaporation (15° from the normal axis of a wafer) of Cr/Au (3/47 nm) with a collimated flux formed physical etch masks along the lower, but not upper regions, of all of the ripples, due to shadowing associated with the overhang relief. The evaporation angle controls the extent of this shadowing (see Supporting Information). Anisotropic wet chemical etching with a KOH solution (PSE-200, Transene Co., 110 °C) removed Si along the <110> direction, beginning in all regions of exposed Si along the sidewalls. The etching rate of KOH along the {110} planes is much faster, by up to several hundred times, than that along the {111} planes because the {110} planes have a lower density of atoms and higher density of dangling bonds than the {111} planes.¹⁴ As a result, this etch proceeded completely from one side of each trench to the adjacent side in a direction parallel to the surface of the wafer, thereby releasing multilayer stacks of individual ribbons with thicknesses determined by the angled evaporation and the ripple structure (i.e., period and amplitude). Removing the Cr/Au with a KI/I₂(aq) solution (2.67/0.67 wt %) and further cleaning with HCl/H₂O₂/H₂O = 1:1:1 by volume and HF(aq) completed the fabrication. Sonication released the ribbons into solution (e.g., CH₃OH) to prepare them for casting onto other substrates.

To facilitate integration of these elements into devices, it is valuable to maintain their lithographically defined alignments and positions. For this purpose, we introduced breaks (width = 10–20 μm) in the SiO₂ lines such that the ends of

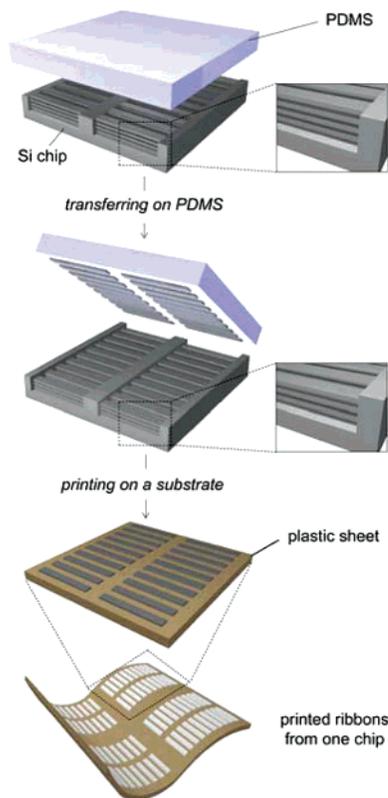


Figure 2. Schematic illustration of steps for transfer printing, one layer at a time, organized arrays of silicon micro-/nanoribbons from multilayer stacks created on the surface of a silicon wafer. The arrays of ribbons can be printed onto a wide range of substrates, including flexible plastics as illustrated here. The dashed boxes on the left illustrate the zoomed regions that appear on the right.

each ribbon remained anchored to the Si wafer even after complete undercut etching with KOH. Soft printing techniques that use elastomeric elements of poly(dimethylsiloxane) (PDMS) can lift up organized arrays of such anchored Si ribbons,^{7,15} one layer at a time, from the source wafer for transfer to a target substrate. Figure 2 schematically illustrates this process, as applied to a flexible plastic substrate. Applying slight pressure on the PDMS to enable contact with progressively lower Si ribbon layers and quickly peeling it away released ribbon arrays with the highest transfer efficiencies ($> \sim 90\%$ up to a third layer).¹⁵ Using small pressures allowed conformal contact but at the same time avoided breaking and/or distorting the ribbons. In this approach, the ribbons adhere to the PDMS through van der Waals interactions that are, as integrated along the lengths of the ribbons, sufficiently strong to fracture the ribbon anchors upon peelback. Contacting the Si ribbon-coated stamps to a substrate (thickness = 0.2 mm, PET, -Delta Technologies) with a thin, spin cast adhesive layer (thickness = 135 nm, SU-8, Microchem) and heating at 70 °C for 1 min produced strong bonding between the ribbons and the substrate. Peeling away the PDMS removed the ribbons from the PDMS. Flood exposing the adhesive (photopolymer) layer to ultraviolet light ($\lambda = 365$ nm, 13 mW/cm², 10 s) and further heating (120 °C, 5 min) enhanced the adhesion between the ribbons and the substrate. Multiple cycles of transfer printing with a single wafer source of ribbons can

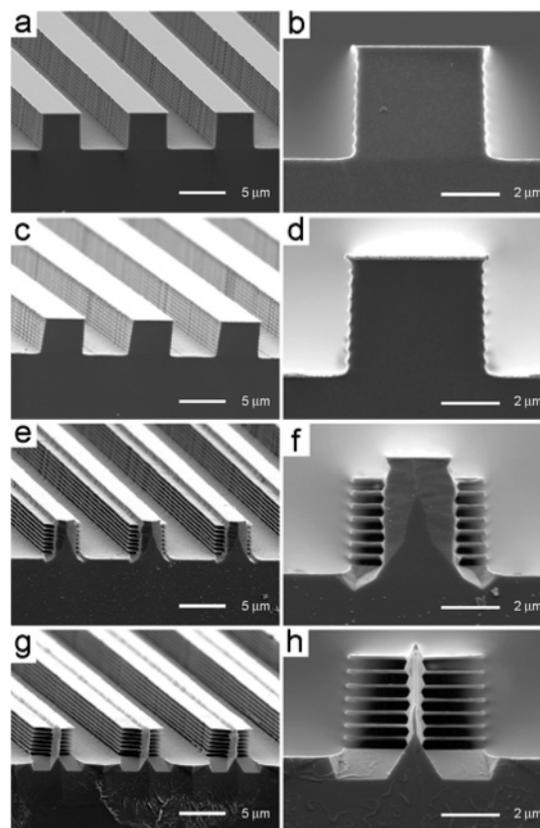


Figure 3. Scanning electron micrographs of a Si(111) wafer in angled (a, c, e, g) and cross-sectional (b, d, f, h) views at various stages of the fabrication of multilayer stacks of ribbons: (a and b) after vertical etching (ICPRIE) to produce trenches with rippled sidewalls; (c and d) after shallow angle physical vapor deposition of metal masking layers; (e through h) after anisotropic wet chemical etching (KOH) for 2 min (e and f) and 5 min (g and h) followed by removal of the metal.

produce large area coverage (compared to the wafer) on plastic, as illustrated in Figure 2, or other substrates.

Figure 3 shows scanning electron microscope (SEM) images of a Si(111) wafer (Montco, Inc., n-type, 1–10 Ωcm) at various stages of the process illustrated in Figure 1. The thicknesses, in the intermediate processing state corresponding to parts g and h of Figure 3, were 100 ± 10 nm. Fully released ribbons had thicknesses of 80 ± 15 nm, due to extended exposure to the KOH etchant. The thickness uniformity is excellent in a given multilayer stack, as well as across the wafer, except for the top most ribbon which is somewhat thinner (by ~ 10 nm in this case) than the others due to a slight undercut in the ICPRIE below the SiO₂ mask (see Supporting Information). The lengths and widths of the ribbons are uniform within a variation of ± 120 nm using conventional contact mode photolithography. For this range of thicknesses, widths of 3–5 μm, and lengths up to several centimeters, the ribbons did not collapse into contact with one other during the KOH etching, until they were completely undercut. By change of the amplitudes and periods of the sidewall ripples, thicknesses between 80 and 300 nm could be achieved, uniformly across the wafer (see Supporting Information). The variations in thicknesses of individual ribbons define the smallest thicknesses that can be achieved

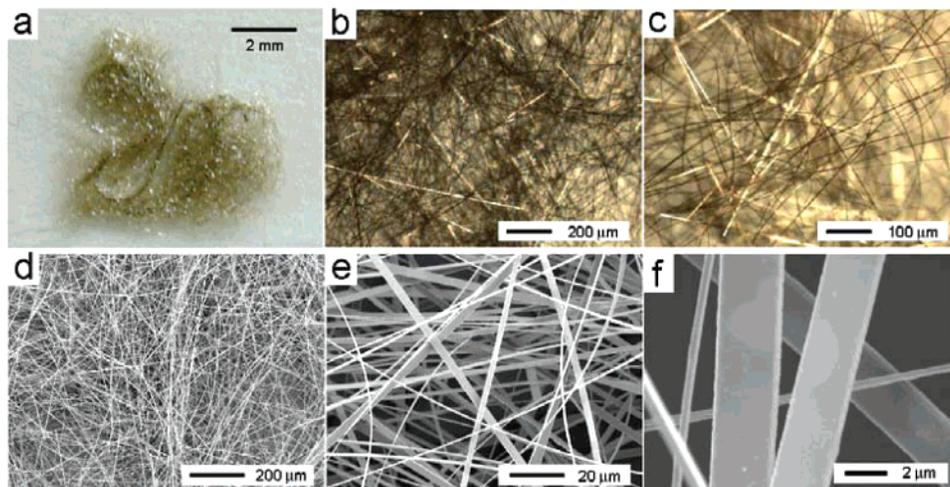


Figure 4. (a) Photograph and (b and c) optical micrographs of Si(111) ribbons after release from the wafer. (d–f) Scanning electron micrographs of the ribbons shown in (a) at various levels of magnification.

reliability. These variations have four main sources. The first two are the roughness on the edges of the SiO₂ masks and on the rippled sidewalls, both of which directly translate into thickness variations. Third, grain structure in the angle evaporated metal masks can cause similar effects. Fourth, slight misalignments of the ICPRIE etched trenches from the Si {110} planes and inhomogeneities (i.e., local temperature and concentration) in the KOH etching bath can also lead to variations.¹⁶ These factors place practical bounds on the smallest reliably achievable ribbon thickness at ~80 nm, with the procedures described here. Widths as small as ~1 μm are possible using a standard contact mode photolithography tool. We estimate that combined improvements in the lithography (e.g., use of electron beam or imprint lithography), etching (e.g., temperature controlled ICPRIE), and deposition (e.g., smaller grain sizes in the metal resist lines) could substantially (i.e., by two times or more) reduce these minimum dimensions. The other limit associated with this process is on the ratio of width to thickness; ratios larger than ~60 are difficult to achieve, due to aspects associated with the KOH etching, such as its finite degree of anisotropy as well as mechanical collapse of the ribbons and/or delamination of the metal mask lines before complete undercut.

Figure 4 shows collections of these ribbons deposited from solution onto a glass slide, after releasing them from the wafer by sonication. The uniformity in the widths and lengths of these ribbons is high (variation = ±120 nm). The ~6 × 10³ ribbons (thickness = 250 nm, width = 3 μm, and length = ~1.5 cm), shown here were collected from an area of 1.5 × 1.5 cm²; this sample represents 90 m of ribbons with a mass of 0.16 mg. Experimental data suggest that scaling the process up to as many as 10 layers, with wafers having diameters of up to 150 mm is readily possible. In this case, a single processing sequence (Figure 1) would generate 32 mg of ribbons. It is important to note, in this case, that large substrates require some care in order to achieve uniform deposition angles for the metal masking layers. For a typical evaporator system, such as the one used for the studies reported here, variations in deposition angles are 0.72°, 1.36°,

and 13.8° for substrate diameters of 8, 15, and 150 mm, respectively. Increasing the distance between the source and substrate, or other easily implementable strategies, can reduce these variations substantially.

The high level of disorder present in the ribbons shown in Figure 4 highlights the need to achieve well-defined configurations suitable for device integration. The anchoring approach illustrated in Figure 2 represents one possibility, in which the lithographically defined alignment and orientation of the ribbons are maintained throughout the fabrication and integration process. Figure 5 shows images of a Si chip (total pattern size: 8 × 8 mm²) with aligned four-layered stacks of ribbons (width = 4 μm, length = 190 μm, thickness = ~250 nm) anchored to the wafer at their ends. The optical micrograph of Figure 5a shows 1.5 × 10⁵ ribbons. The scanning electron micrographs highlight the anchors and the etch planes (Figure 5b–e). The KOH etch front advances in the <110> direction, but the front terminates at {111} planes (i.e., slowest etching plane), as seen in Figure 5e where the structure tapers into triangular-shaped anchors that meet at a point where two {111} planes intersect. Soft printing processes can transfer these ribbons, one layer at a time, onto other substrates, using the procedures of Figure 2. Figure 6a shows an example of Si ribbon arrays (thickness = 235 nm, width = 4.8 μm, length = 190 μm) transferred from the top layer onto a PDMS substrate. The thickness variations arising from previously mentioned factors appear as color variations in the optical image of Figure 6a, tapered thickness profiles in Figure 6b, and discontinuities when the ribbons are very thin (e.g., lower than 40 nm). The atomic force microscopy (AFM) image reveals well-separated steps (or terraces, with heights of up to 10 nm) on the surfaces of the ribbons. The surface roughness of areas (1 × 1 μm²) that do not include these steps is ~0.6 nm, compared to ~3 nm in similar sized areas that include these steps. Similar structures have been observed on the surfaces of Si(111) wafers etched by KOH.¹⁵ Such structures cause some color variations in the optical images. The roughness value of 0.6 nm is somewhat larger than that of the top polished surface of the wafer (0.12 nm), of structures generated from a silicon-on-

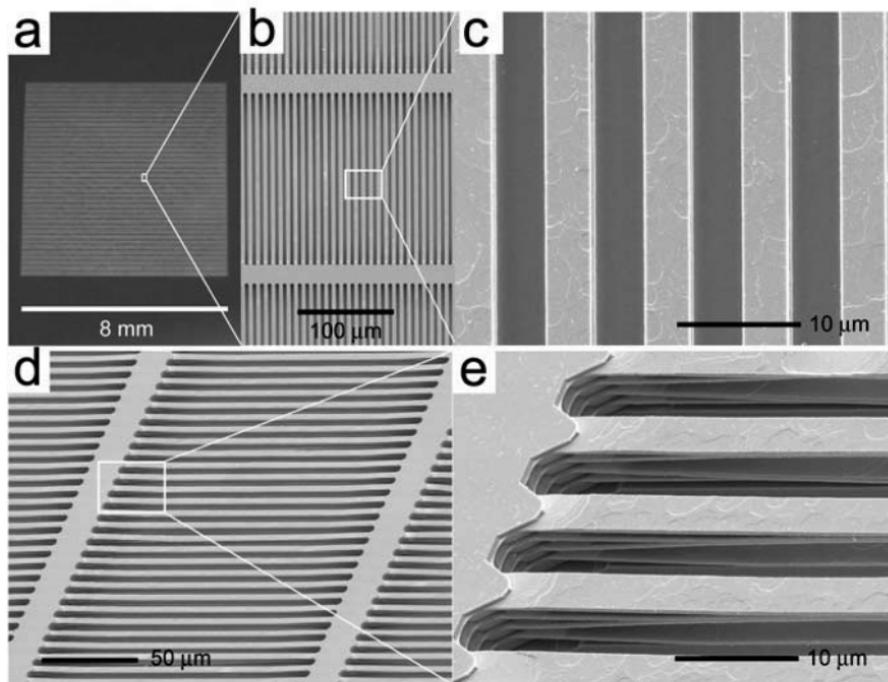


Figure 5. (a) Photograph of a large, aligned array of a four-layer stack of Si(111) ribbons. (b and c) Top view and (d and e) angled view of scanning electron micrographs of the sample shown in (a). The anchor structures at the ends of the ribbons leaves them attached to the underlying wafer, in a manner that preserves their lithographically defined positions, even after they have been completely undercut by the anisotropic etchant.

insulator (SOI) substrates (0.18 nm), or of ribbons generated from the top surface of a Si wafer (0.5 nm). The roughness originates from the same effects that determine the variations in thickness, as discussed previously. Thickness variations along typical ribbons were $\sim\pm 15$ nm. Variations in the average thicknesses of ribbons in a given array were $\sim\pm 3$ nm. Figure 6c displays four areas of ribbon arrays formed on an ITO-coated PET substrate by four cycles of printing, using a single processed Si wafer. The yields on the printed ribbons were 98% for the first layer, 94% for the second layer, 88% for the third layer, and 74% for the fourth layer. The lower yield for the fourth layer was mainly due to imperfect transfer from the wafer to the PDMS. Incomplete transfer from an upper layer leaves partially detached ribbons on the wafer that can interfere with subsequent printing cycles.

To demonstrate one possible use of printed ribbon arrays in electronics, we fabricated field effect transistors (Figure 7a,b). The substrate was polyimide (PI, thickness = $25\ \mu\text{m}$), the gate electrode was Cr/Au (thickness = $3/40$ nm), and the gate dielectric consisted of a layer of SiO₂ (thickness = 170 nm) and the SU-8 adhesive coating from the procedures of Figure 2. The transferred Si ribbon arrays sank approximately 35 nm into the SU-8, leaving a residual 100 nm of SU-8 between the bottom surface of the Si ribbons and the SiO₂ gate dielectric, as measured by AFM. Thick electrode pads (Ti, 250 nm) defined by photolithography ($100\ \mu\text{m}$ length \times $100\ \mu\text{m}$ width, spanning 10 Si ribbons) and wet etching with Ti etchant (TFTN, Transene Co.) formed Schottky barrier contacts for the source and drain. These bottom-gate devices showed n-type enhancement mode gate modulation (Figure 7c,d), consistent with similar devices

formed on SOI wafers using similar processing conditions. The transistors exhibited on/off ratios of $\sim 3 \times 10^4$. The linear regime, per ribbon mobilities (fill factor 35%) correspond to $190\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$ for the first layer and $130\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$ for the second layer. These values are somewhat lower than those that we have obtained using SOI wafers and otherwise similar device processing steps.^{7,11} We speculate that the larger roughness in the ribbons used here is partly a cause of this difference. Also, it is well-known that the interface charge density on the {111} plane is almost 10 times larger than that on the {100} plane for the Si–SiO₂ interface; annealing in hydrogen can reduce the value significantly.¹⁷

In summary, this Letter demonstrates a simple fabrication strategy for producing bulk quantities of single-crystal silicon micro-/nanoribbons from bulk silicon (111) wafers. Each layer in the multilayer stacks produced by this approach can be separately transfer printed onto other substrates, for integration into devices such as transistors. The simplicity of the procedures, the ability to form organized arrays for devices, the high quality of the materials, and the potential for other device possibilities such as sensors, photodetectors and perhaps photovoltaics, in addition to electronic circuits, suggest potential value for this type of approach to silicon ribbons.

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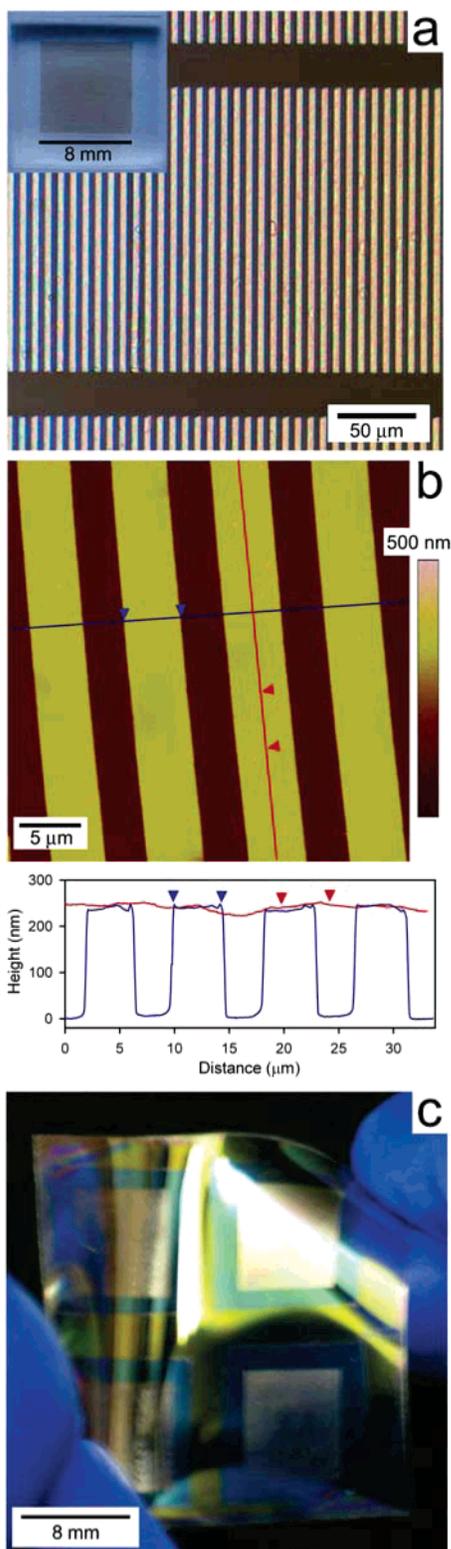


Figure 6. (a) Optical images of aligned Si(111) ribbons transfer printed onto a substrate of poly(dimethylsiloxane). (b) Atomic force microscope image and line scan from four ribbons from the array shown in (a). Photograph of a flexible polyester film that supports four separate patches of Si(111) ribbon arrays produced by four cycles of transfer printing using a single processed Si chip.

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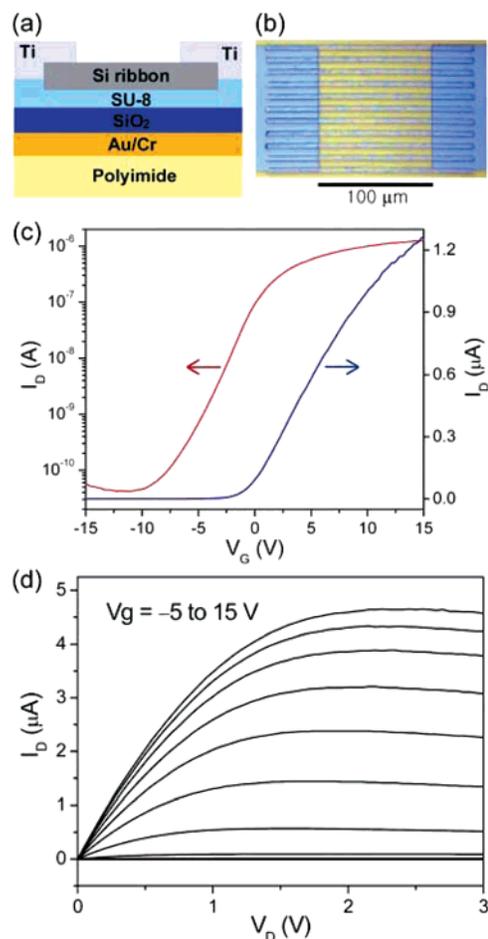


Figure 7. (a) Schematic cross sectional diagram of a transistor that uses silicon ribbons for the semiconductor. (b) Optical micrograph top view of a device. (c) Transfer curve and (d) full current/voltage characteristics from a typical device.

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Supporting Information Available: Photomicrographs of various sidewalls according to different STS-ICPRIE conditions and silicon nanoribbons with different thicknesses, the extent of shadowing mask vs angles for electron beam evaporation, and seven-layered Si ribbons and spectra from a EDAX energy dispersive spectroscopy (EDS) study. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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