Gallium arsenide arrays

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Printed Arrays of Aligned GaAs Wires for Flexible Transistors, Diodes, and Circuits on Plastic Substrates**

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Micro- and nanoscale wires, ribbons, platelets, and so on, of single-crystal inorganic semiconductors represent attractive building blocks for functional devices (e.g., optics, optoelectronics, electronics, sensing, etc.) that can be used in many applications.[1–4] For example, Si nanowires that are synthesized through “bottom-up” approaches can be assembled into aligned arrays using Langmuir–Blodgett techniques (or microfluidics) and used as transport channels for flexible thin-film transistors (TFTs) on plastic substrates.[5,6] In a different approach, micro/nanoscale elements of Si (microstructured silicon, μs-Si) in the form of ribbons, with thicknesses of $\approx$100 nm and widths ranging from several to hundreds of micrometers, can be generated from high-quality, single-crystalline bulk sources (e.g., silicon-on-insulator (SOI) wafers or bulk wafers) through “top-down” approaches.[7,8] This type of material can be used to fabricate flexible TFTs on plastic with device mobilities as high as 500 $cm^2V^{-1}s^{-1}$.[7–9] The high quality of the wafer-based source material (in terms of well-defined doping levels, uniformity in doping, low surface roughness, and density of surface defects) leads to a silicon-based semiconductor material with similarly good properties, which are beneficial for reliable, high-performance device operation. The top-down fabrication process is attractive because it also offers the possibility of preserving the highly ordered organization of nano/microstructures defined at the wafer level during “dry transfer printing” to the final (e.g., plastic) device substrate.[8,9] Although high performance is possible with Si, even better characteristics (e.g., operating speed) can be achieved with, for example, GaAs, due to its high intrinsic electron mobility of $\approx$8500 $cm^2V^{-1}s^{-1}$. Our previous work demonstrated techniques for generating, using anisotropic chemical etching steps, nano/microwires with triangular cross sections from GaAs wafers with top-down fabrication steps.[10] By forming ohmic contacts on these GaAs wires while they are still tethered to the wafer and then transfer printing them to plastic substrates, it is possible to build mechanically flexible metal-semiconductor field-effect transistors (MESFETs) with excellent properties.[11] These transistors show unity current-gain frequency in the gigahertz regime.[12] The work presented here demonstrates the ability to build, with transfer printing as the assembly/integration strategy, various elemental units of functional circuits, such as inverters and logic gates, on plastic substrates using this type of MESFET, as well as GaAs-wire-based diodes as active components. These types of systems could be important in large-area electronic circuits for steerable antennas, structural health monitors, and other flexible devices on lightweight plastic substrates that have demanding requirements of high speed and high performance.[13]

Figure 1a depicts the major steps for fabricating GaAs transistors, diodes, and logic gates on plastic. The basic approach relies on top-down fabrication techniques to generate micro/nanowires with high purity and well-known doping profiles from bulk-single-crystal GaAs wafers. Ohmic contacts, formed on the wafer before fabricating the wires, consist of AuGe (120 nm)/Ni (20 nm)/Au (120 nm) deposited and annealed (450 °C for 1 min in a quartz tube with flowing N_2) on an epitaxial layer of 150-nm n-type GaAs on a (100) semi-insulating GaAs (SI-GaAs) substrate. The contact stripes lie along the $(0\bar{1}\bar{1})$ crystallographic orientation and have widths of 2 μm. In the case of transistors, the gaps between the ohmic stripes define the channel lengths. Photolithography and anisotropic chemical etching generate arrays of GaAs wires with triangular cross sections (inset of Figure 1b) and widths of $\approx$2 μm, with the wire ends connected to the wafer (Figure 1b). These connections act as ‘anchors’ to maintain the well-defined orientation and spatial location of the wires, as defined by the layout of the etching mask (i.e., photoresist pattern). Removing the etching mask and depositing a bilayer of Ti(2 nm)/SiO_2(50 nm) via electron-beam evaporation prepares the surfaces of the wires for transfer printing. The triangular cross section ensures that the Ti/SiO_2 films on the surfaces of the wires do not connect to those on the mother wafer, thus facilitating the yield of transfer printing. Laminating a slightly oxidized poly(dimethylsiloxane) (PDMS) stamp on the surface of the wafer leads to chemical bonding between the surface of the PDMS stamp and the fresh SiO_2 film via a condensation reaction[14] (see top frame of Figure 1a). Peeling back the PDMS stamp pulls the wires off the wafer and leaves them bound to the stamp. Contacting this ‘inked’ stamp to a poly(ethylene terephthalate) (PET) sheet coated with a thin layer of liquid polyurethane (PU), curing the PU, peeling off the stamp, and then removing the Ti/SiO_2 layer in a 1:10

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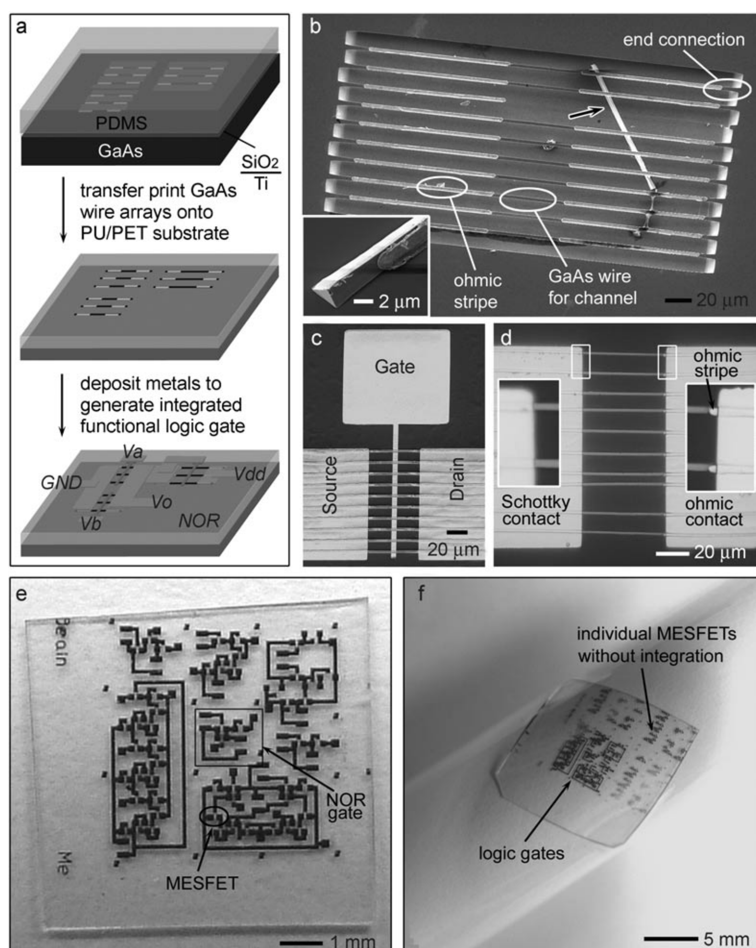

Figure 1. a) Schematic illustration of the process for fabricating transistors, diodes, and logic circuits on plastic, using transfer-printed GaAs wires integrated with ohmic stripes, prepared from a single-crystalline GaAs wafer (PDMS: poly(dimethylsiloxane), PET: poly(ethylene terephthalate), PU: polyurethane). b) Scanning electron microscopy (SEM) image of an array of GaAs wires (with ohmic stripes) with their ends connected to the mother wafer. The partial wire shown by the arrow lies underneath the arrayed wires, indicating that the GaAs wires are separated from the bulk wafer. The inset presents a free-standing individual wire, clearly showing its triangular cross section. c) SEM image of an individual MESFET with a channel length of 50 µm and gate length of 5 µm, formed with the GaAs wire array shown in (b), transfer-printed on a PET substrate. d) Optical micrograph of a Ti/n-GaAs Schottky diode on a PET sheet. The insets show that one electrode pad connects the ohmic stripes on one end of the wires, whilst the other electrode (150-nm Ti/150-nm Au) pad directly connects to the GaAs wires to form Schottky contacts. e, f) Optical images of PET substrates with various logic gates and individual MESFETs mounted on a flat surface (e) and on the curved shaft of a white marker (f).

HF solution leaves ordered arrays of GaAs wires on the PU/PET substrate, as illustrated in the central frame of Figure 1 a. The Ti/SiO_2 film not only serves as an adhesive layer to bond the GaAs wires to the PDMS but it also protects the surface of the GaAs wires from possible contamination (e.g., by solvents and PU) during the processing.

In this format, the pristine, bare surfaces of the wires and ohmic stripes are exposed for further lithographic processing and metallization to define source and drain electrodes (250-nm Au) that connect the ohmic contacts integrated on the wires. For transistors, these electrodes define the source and drain; for the diodes, they represent the ohmic electrode. Contacts (150-nm Ti/150-nm Au) formed by photolithography and liftoff on the bare parts of the wires (without any surface treatment) while they are integrated with the plastic substrates define Schottky contacts for the diodes, and gate electrodes for the MESFETs. All of the processing on the plastic substrate occurs at temperatures below 110 °C. We did not observe any debonding of GaAs wires from the substrates due to mismatches in thermal expansion coefficients or other possible effects. In the transistors, the width of the gate electrode represents the critical dimension for controlling the operating speed. The position of this electrode between the source and drain is relatively unimportant in this work. This tolerance to poor registration, which is not present in non-self-aligned high-speed metal oxide semiconductor field-effect transistor (MOSFET) devices, is critically important for reliably achieving high-speed operation on plastic substrates, where precise registration is often challenging or impossible due to slight, uncontrolled deformations that may occur in the plastic during processing. Connecting multiple transistors and diodes together in appropriate geometries generates functional logic circuits. An NOR gate is shown in Figure 1 a.

A scanning electron microscopy (SEM) image (Figure 1 c) shows ten parallel wires that form the semiconductor component of a transistor. The channel length and gate length of this device are 50 and 5 µm, respectively. These geometries were used for building the simple integrated circuits, i.e., logic gates. The Ti/Au stripe in the gap between the source and drain electrodes forms a Schottky contact with the n-GaAs surface. This electrode acts as a gate for modulating the flow of current between source and drain. Diodes (Figure 1 d) use wires with ohmic stripes on one end and Schottky contacts on the other. A collection of GaAs transistors, diodes, and simple circuits on a PET substrate is shown in Figure 1 e and f. In Figure 1 f the PET sheet with circuits is bent around the shaft of a white marker, indicating the flexibility of these electronic units.

The DC characteristics of the wire-based MESFETs on plastic (Figure 1 c) exhibited qualitatively the same behavior (Figure 2 a) as those formed on the wafer.[15] The flow of current between source and drain (I_{DS}) is well modulated by the bias applied to the gate (V_{GS}), i.e., the I_{DS} decreases with the decrease of V_{GS}. In this case, the negative V_{GS} depletes the effective carriers (electrons for n-GaAs) in the channel region and decreases the channel thickness. Once the V_{GS} is negative enough, the depletion layer equals the thickness of the n-GaAs layer, and the flow of current be-

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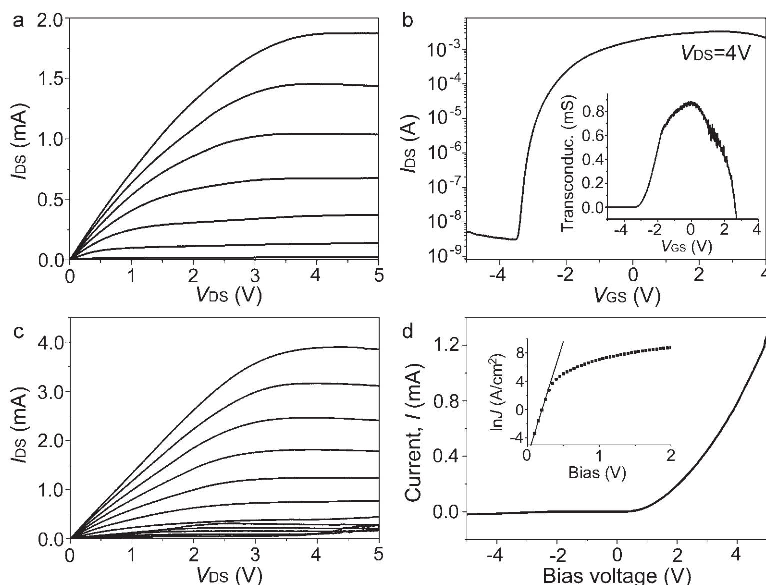

Figure 2. Characterization of GaAs-wire MESFETs with a gate length of 5 μm and different channel lengths: a, b) 50 and c) 25 μm on PU/PET substrates. a) Current–voltage (i.e., I_{DS} versus V_{DS}) curves of the transistor shown in Figure 1 c at different gate voltages (V_{GS}). From top to bottom, the V_{GS} decreases from 0.5 to −3.0 V in steps of 0.5 V. b) Transfer curve of the same transistor in the saturation region of $V_{DS}=4$ V. The inset shows the derivative of the transfer curve, revealing the dependence of the transconductance on the gate voltage. c) Source–drain current at different V_{GS} for a transistor with a channel length of 25 μm. From top to bottom, the V_{GS} decreases from 0.5 to −5.0 V in steps of 0.5 V. d) *I–V* characteristics of the as-fabricated Au/Ti-GaAs Schottky diodes, showing good rectifying capabilities. The inset shows the relationship between ln*J* and the bias voltage.

tween source and drain is pinched off (i.e., the I_{DS} becomes essentially zero). As shown in Figure 2 a, the I_{DS} drops to almost zero at a V_{GS} of less than −2.5 V. The pinch-off voltage (i.e., V_{GS}) at a drain–source voltage (V_{DS}) of 0.1 V (i.e., linear region) is −2.7 V. Figure 2 b shows the transfer curve of this transistor in the saturation region ($V_{DS}=4$ V). The ON/OFF current ratio and maximum transconductance were extracted from Figure 2 b as $\approx 10^6$ and ≈880 μS, respectively. The overall source–drain current is a function of the number of wires (i.e., the effective channel width) and the distance between source and drain (i.e., the channel length). With constant channel width, transistors with short channels can produce relatively high currents. For example, the saturated I_{DS} at $V_{GS}=0.5$ V and $V_{DS}=4$ V increases from 1.75 to 3.8 mA for transistors with channel lengths of 50 and 25 μm, respectively (Figure 2 c). Although transistors with short channels can supply high currents for certain applications, the ON/OFF current ratio tends to decrease due to the difficulty of completely pinching off the current. As shown in Figure 2 c, the I_{DS} of a transistor with a channel length of 25 μm was still of the order of tens of microamperes, and even the V_{GS} was −5 V. The leakage current can be significantly decreased by thinning the channel thickness, i.e., the thickness of the n-GaAs layer, which determines the current density at the ON status. In addition, this kind of MESFET on PET substrates with a thickness of ≈200 μm exhibits excellent mechanical flexibility (see Supporting Information Figure S 1).[11]

The GaAs-wire Sckottky diodes on plastic exhibit the typical behavior (Figure 2 d) of rectifiers, i.e., the forward current (I) increases quickly with increasing forward bias voltage (V), whilst the reverse current remains small even at reverse biases as large as 5 V. The *I–V* characteristics of these Schottky diodes can be described by the thermionic emission model,[15] which is expressed as follows at $V \gg 3kT/q$:

$$J \approx J_0 \exp\left(\frac{qV}{nkT}\right) \tag{1}$$

with

$$J_0 = A^{**}T^2 \exp\left(\frac{q\phi_B}{kT}\right) \tag{2}$$

where J represents the forward diode current density with V, k is the Boltzmann constant, T is the absolute temperature (298 K in the experiment), q is the electron charge, ϕ_B is the height of the Schottky barrier, and A^{**} is the effective Richardson constant (8.64 A cm^{-2} K^{-2}) for GaAs.[16] By plotting the relationship between ln$J$ and V (inset of Figure 2 d), the saturation current J_0 and the ideality factor n can be determined from the intercept and slope of the linear relation. The quantity ϕ_B can be estimated with Equation (2). ϕ_B and n are commonly used as the evaluation criteria of Schottky interfacial properties. Both are highly dependent on the interface charge states between metal and GaAs; an increase of charge states will cause the decrease of ϕ_B and the increase of n. For the diodes fabricated in this work, ϕ_B and n are determined from the inset of Figure 2 d to be 512 meV and 1.21, respectively. These devices have a somewhat lower Schottky barrier (512 versus ≈800 meV) and larger ideality factor (1.21 versus ≈1.10) compared with the diodes built on wafers.[17,18]

These GaAs-wire devices (i.e., MESFETs and diodes) can be integrated into logic gates for complex circuits. For example, connecting two MESFETs with different channel lengths, which have different saturation currents, forms an inverter (logic NOT gate) (Figure 3 a and b). The load (top of images) and switching transistor (bottom) have channel lengths of 100 and 50 μm, respectively, channel widths of 150 μm, and gate lengths of 5 μm. This design results in a saturation current from the load transistor that is ≈50% that of the switching transistor; this ensures that the load line intersects the $V_{GS}=0$ curve of the switching transistor in the linear region with a small turn-on voltage. The inverter was measured in the saturated region, i.e., V_{dd} bias of 5 V. When a large negative voltage (logic 0) is applied to the gate of the switching transistor (V_{in}) to turn it off, the voltage of the output node (V_{out}) equals V_{dd} (logic 1, high positive voltage) because the load transistor is always on. An increase in V_{in} turns the switching transistor on and pro-

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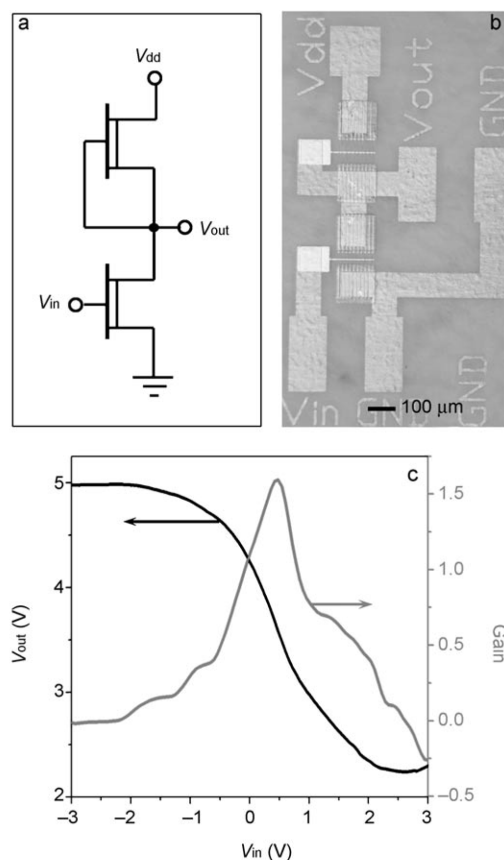

Figure 3. a) Circuit diagram, b) optical image, and c) output–input characteristics of an inverter. All MESFETs have a gate length of 5 µm. The V_{dd} was biased to 5 V versus ground (GND).

vides a large current through both the switching and load transistors. V_{out} decreases to a low positive voltage (logic 0) when the switching transistor is completely turned on, i.e., V_{in} is a large positive voltage (logic 1). Figure 3c shows the transfer curve. The inverter exhibits a maximum voltage gain ($(dV_{out}/dV_{in})_{max}=1.52$) higher than unity. The switching ability of this inverter did not show significant degradation after many cycles of ON/OFF operation (see Figure S2). The logic status of V_{out} can be shifted to voltages suitable for further circuit integration by adding a level-shifting branch composed of Schottky diodes, as shown in Figure 1d.[19]

Combining several devices of this type in parallel or in series yields more complex logic functions, such as NOR and NAND gates. For the NOR gate shown in Figure 4a and b, two identical MESFETs in parallel serve as the switching transistors. Turning on either switching transistor (V_A or V_B) by applying a high positive voltage (logic 1) can provide a large current flow through the drain (V_{dd}) of the load transistor to ground (GND), resulting in an output voltage (V_o) at a low level (logic 0). High positive output voltage (logic 1) can be achieved only when both inputs are at high negative voltages (logic 0). The dependence of the output on the inputs of the NOR gate is shown in Figure 4c. In the configuration of a NAND gate (Figure 4d and e), the current is large through all transistors only when both switching transistors are turned on by applying high positive voltages (logic 1). The output voltage exhibits a relatively low value (logic 0) in this configuration. With other input combinations, almost no current flows through the transistors, resulting in a high positive output voltage (logic 1), comparable to V_{dd} (Figure 4f). Further integration of logic gates of this type and other passive elements (e.g., resistors, capacitors, inductors, etc.) offers the promise for high-speed, large-area electronic systems on plastic.

In summary, GaAs wires with integrated ohmic contacts fabricated using top-down procedures with high-quality, bulk-single-crystal wafers provide a high-performance 'printable' semiconductor material and a relatively easy path to transistors, diodes, and integrated logic gates on flexible plastic substrates. The separation of high-temperature processing steps (e.g., the formation of ohmic contacts) from the plastic substrates and the use of PDMS stamps for transfer printing well-ordered arrays of GaAs wires are key features of the approach described here. The use of GaAs wires as the semiconductor is attractive for large-area printed electronics with demanding requirements on operating speed because i) GaAs has a high intrinsic electron mobility ($\approx 8500\ cm^2 V^{-1} s^{-1}$) and has established applications in conventional high-frequency circuits;[19] ii) MESFETs built with GaAs offer simpler processing than MOSFETs because the

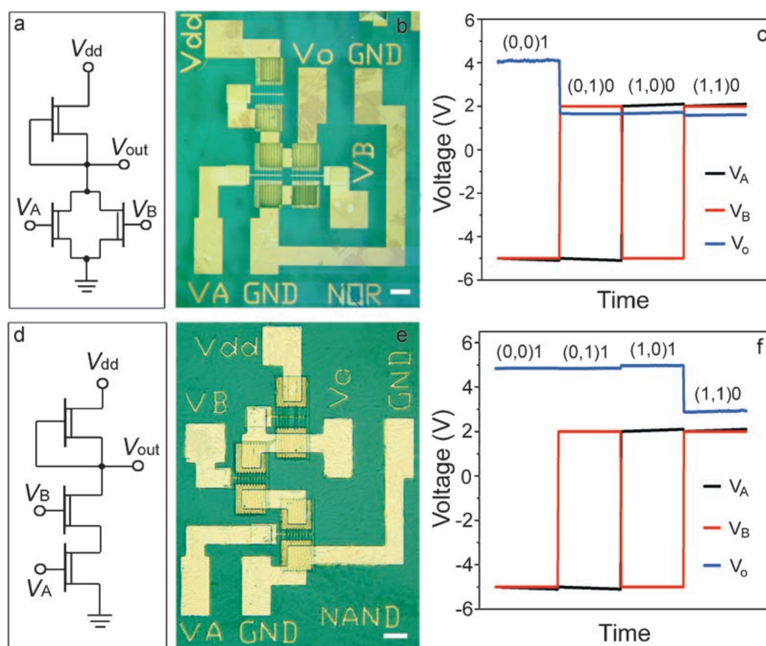

Figure 4. Circuit diagrams, optical images, and output–input characteristics of different logic gates: a, b, c) NOR gate; d, e, f) NAND gate. All MESFETs have a gate length of 5 µm. The scale bars represent 100 µm. V_{dd} applied to these logic gates was 5 V versus ground (GND). The logic "0" and "1" input signals of the NOR and NAND gates were driven by −5 and 2 V, respectively. The logic "0" and "1" outputs of the NOR gate were 1.58–1.67 and 4.1 V, respectively. The logic "0" and "1" outputs of the NAND gate were 2.90 and 4.83–4.98 V, respectively.

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MESFETs do not require gate dielectrics; iii) GaAs MESFETs do not suffer from parasitic overlap capacitances that occur in non-self-aligned MOSFETs; iv) high-speed operation in GaAs MESFETs is possible even with the modest levels of patterning registration and resolution that can be achieved easily on large-area plastic substrates. The relatively high cost of GaAs (compared with Si) and difficulty of generating complementary circuits with GaAs-wire devices represent drawbacks. Nevertheless, the relative ease with which high-performance transistors and diodes can be built on plastic substrates, and the ability to integrate these components into functional circuits, indicates some promise for this path to electronic systems where mechanical flexibility, lightweight construction, and compatibility with large-area, printing-like processing are required.

Experimental Section

The GaAs wafer (IQE Inc., Bethlehem, PA) consisted of an epitaxial Si-doped n-type GaAs layer (with a carrier concentration of 4.0×10^{17} cm^{-3}) grown on a (100) semi-insulating GaAs wafer by molecular beam epitaxial (MBE) deposition in a high-vacuum chamber. The lithography processes employed an AZ photoresist (AZ 5214 and AZ nLOF 2020 for positive and negative imaging, respectively), which were carried out at temperatures (<110 °C) compatible with the plastic substrates, i.e., PET sheets of ≈175 µm thickness (Mylar film, Southwall Technologies, Palo Alto, CA) covered with a thin layer of cured PU (NEA 121, Norland Products Inc., Cranbury, NJ). The GaAs wafers with photoresist mask patterns were anisotropically etched in the etchant (4 mL H_3PO_4 (85 wt%), 52 mL H_2O_2 (30 wt%), and 48 mL deionized water), which was cooled in the ice-water bath. All the metals were evaporated at a speed of ≈4 Ås^{-1} using an electron-beam evaporator (Temescal). The evaporation was stopped and the samples cooled (for 5 min) to prevent the plastic substrates from melting when 50-nm thick metals were deposited. After the samples were cooled, repeating the evaporation/cooling cycle deposited more metals.

Keywords:
flexible electronics · gallium arsenide · logic gates · nanowire arrays · Schottky diodes

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