Gigahertz operation in flexible transistors on plastic substrates

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The combined use of GaAs wires with Ohmic contacts formed from bulk wafers, soft lithographic transfer printing techniques, and optimized device designs enables mechanically flexible transistors to be formed on low-cost plastic substrates, with individual device speeds in the gigahertz range and with high degrees of mechanical bendability. These high-speed devices incorporate materials in simple layouts that can be fabricated with modest lithographic patterning resolution and registration. This letter describes their electrical and mechanical characteristics. The results have the potential to be important to certain large-area, "macroelectronic" systems that can provide for high-speed communication and processing capabilities. © *2006 American Institute of Physics*.
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Large-area, flexible electronic systems (i.e., macroelectronics) formed with high-mobility semiconductors are interesting for end applications, in the military and consumer areas, where high-speed communication and/or computation capabilities are required.[1] Devices with these capabilities might be used together with or as a complement to those based on well explored semiconductors based on organic semiconductors and/or *a*:Si. Flexible thin film transistors (TFTs) built with various high performance inorganic materials, such as amorphous/polycrystalline oxides and chalcogenides,[2,3] polycrystalline silicon[4] as well as single crystalline silicon nanowires[5,6] and microstructured ribbons,[7–9] exhibit mobilities ($10-300\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$) that make them potentially interesting for these applications. Our previous work demonstrated that arrays of single crystalline wires of GaAs (intrinsic electron mobility of $\sim 8500\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$) can serve as transport channels for metal-semiconductor field-effect transistors (MESFETs) on flexible plastic substrates.[10] This letter shows that with optimized designs and fabrication process, this type of device can operate with frequencies in the gigahertz regime, even with modest lithographic resolution, and with good bendability. Simple simulations of device behavior agree well with the experimental observations, and indicate that operating frequencies in the *S* band (5 GHz) should be possible.

The basic fabrication strategy is similar to that described elsewhere,[10] but with optimized device geometries and processing methods to enable high-speed operation. GaAs wire (with width of $\sim 2\ \mu$m) arrays with integrated Ohmic stripes (formed by annealing 120 nm AuGe/20 nm Ni/120 nm Au at 450 °C for 1 min in the atmosphere of N_2) were fabricated from a (100) semi-insulating GaAs (SI-GaAs) wafer with epitaxial layer of 150 nm *n*-GaAs through photolithography and anisotropic chemical etching.[10–12] A thin bilayer of Ti(2 nm)/SiO_2(50 nm) was deposited on the undercut GaAs wires to serve as the adhesive layer to facilitate the transfer printing process as well as to protect the flat surfaces of wires and Ohmic contacts from contamination by organics (primarily those that transfer from the surfaces of the stamps) involved in the process. This layer can be easily removed by dipping the samples in 1:10 HF solution to expose the clean surfaces of GaAs wires for device fabrication in the sequential steps. In addition, the thin thickness (compared with the thickness of photoresist layers which were used as the adhesive layer for transfer printing in our previous work[10]) of this Ti/SiO_2 layer resulted in the relatively flat surface of plastic poly(ethylene terephthalate) (PET) sheet, on which GaAs wire arrays were printed with the assistance of a spin-cast thin layer of polyurethane (PU). The enhanced surface flatness enables deposition of narrow gate electrodes without cracks along their longitudinal direction, thus providing an effective route to increase the operation speed of devices.

The resultant MESFETs on PET substrates [see, scanning electron microscope (SEM) image of a typical transistor with gate length of 2 μm as shown in Fig. 1(a)] exhibit dc transport properties similar to those of transistors built on the mother wafers. Figure 1(b) shows the current flow between source and drain (I_{DS}) as a function of gate voltage (V_{GS}) (inset) and as a function of source/drain voltage at different V_{GS}, for a device with gate length of 2 μm. The pinch-off voltage at V_{DS} of 0.1 V (i.e., linear region) is −2.7 V. The on/off current ratio was determined from averaged measurements on many devices to be $\sim 10^6$. The devices exhibit negligible hysteresis (inset), which is particularly important for high-speed response, and good device-to-device uniformity. The statistical results (with device number >50) of MESFETs with channel lengths of 50 μm and different gate lengths indicate that the dc characteristics are almost independent of the gate length except that devices with larger gate lengths exhibit somewhat lower on/off ratios. The gate length plays a critical role in determining the operating frequencies, as described in the following.

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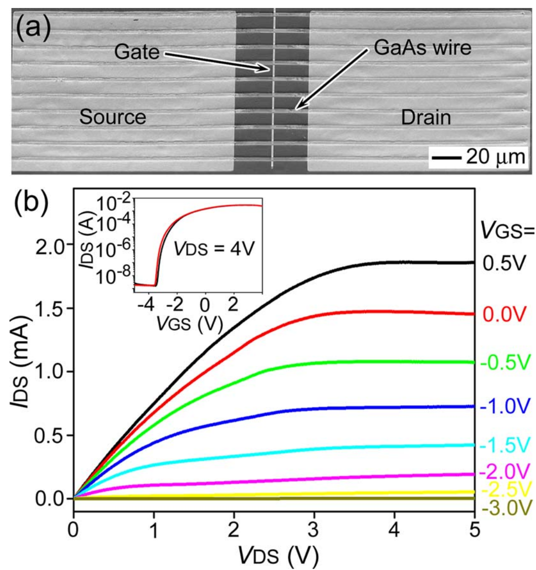

FIG. 1. (Color online) (a) SEM image of an individual GaAs-wire MESFET with channel length of 50 μm and gate length of 2 μm on PU/PET substrate, showing that each transistor was formed with ten aligned GaAs wires. (b) Current-voltage (i.e., I_{DS} vs V_{DS}) curves of a transistor shown in (a). From top to bottom, the V_{GS} decreases from 0.5 to −3.0 V at a step of 0.5 V. The inset shows the transfer curve of this transistor in the saturation region of V_{DS}=4 V.

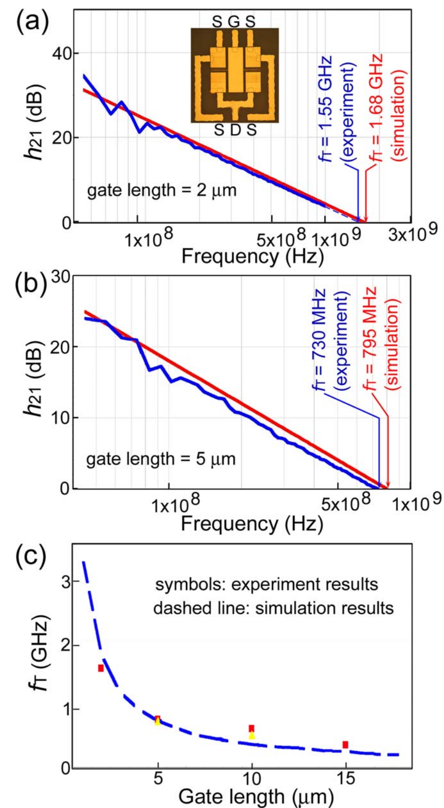

FIG. 2. (Color online) [(a) and (b)] Experimental (blue) and simulated (red) results of rf responses of GaAs-wire MESFETs with different gate lengths: 2 μm (a) and 5 μm (b). The measurements were conducted with probing configuration shown in the inset of (a). (c) Dependence of f_T on gate length. The different symbols represent measurements on different devices; the dashed line corresponds to simulation.

The inset of Fig. 2(a) shows the layout of a device designed for microwave testing. Each unit of the test structure contains two identical MESFETs with gate lengths of 2 μm and channel lengths of 50 μm with a common gate, and probing pads configured to match the layout of the rf probes. In the measurement, the drain (D) terminal was held at 5 V [versus source (S)] and the gate (G) was held at 0 V. The measurement was carried out using Agilent 8720 network analyzer calibrated from 50 MHz to 1 GHz using a standard short-open-load-through (SOLT) technique on a Cascade Microtech impedance standard substrate. The measurements described below involve no further deembedding, and therefore likely underestimate the actual device speeds.

The small-signal current gain (h_{21}) can be extracted from the measured S parameters of the device. This quantity exhibits a logarithmic dependence on the frequency of input rf signal [Fig. 2(a)]. The unity current gain frequency (f_T) is defined as the frequency at which the short-circuit current gain becomes unity.[13] This quantity can be extracted by extrapolating the curve of Fig. 2(a) according to a least-square fit of a −20 dB/decade line and locating its x intercept. The value determined in this manner is f_T=1.55 GHz. This device represents the fastest mechanically flexible transistor on plastic, with an f_T in the gigahertz regime. We also estimated the rf response of GaAs MESFETs according to the small-signal equivalent circuit model[14,15] using the measured dc parameters and the calculated capacities between electrodes. The plot from the simulation result agrees well with the experimental result and yields f_T=1.68 GHz. This model also works well for the transistors with different gate lengths, for example, the experimental f_T (730 MHz) of MESFET with gate length of 5 μm is close to that simulated quantity (795 MHz) [Fig. 2(b)]. In the model, only the intrinsic parameters of MESFET are considered because the extrinsic parameters (i.e., inductance and resistance associated with probing pads) are considered to be negligible. Figure 2(c) compares the measured (symbols) and calculated (dashed line) f_T of GaAs-wire MESFETs with different gate lengths and channel length of 50 μm. The results suggest that f_T could be increased significantly by reducing the gate length or by further optimizing the design of the layers in the GaAs mother wafers.

We previously reported some initial measurements of the effects of tensile strains on wire-based MESFETs with gate length of 15 μm.[10] Here we look more closely at the behavior of high-speed devices in both compression and tension, up to their fracture point. The measurements consisted of full dc electrical characterization as a function of bending the substrate [see Fig. 3(a)] into concave and convex shapes with different radii of curvature.[8] The convex and concave bend surfaces induce tensile (assigned a positive value) and compressive strains (assigned a negative value) on the devices. A device similar to that shown in the inset of Fig. 2(a) was used to evaluate the effect of bending-induced strain on the performance. The saturation current (i.e., V_{DS}=4 V and V_{GS}=0 V) increases by ~10% with increasing tensile strain to 0.71% (corresponding bending radius of 14 mm for the 200 μm thick substrate used in this work) and drops by ~20% with increasing compressive strain to 0.71% [Fig. 3(b)]. The current recovers when the substrate is released after bending in either direction, suggesting that deformations of the plastic substrate and the other components of the devices are elastic in this regime. Previous studies on the strained epilayers of $Ga_xIn_{1-x}As$ on (100) GaAs wafers reveal that biaxial stress as well as externally applied uniaxial

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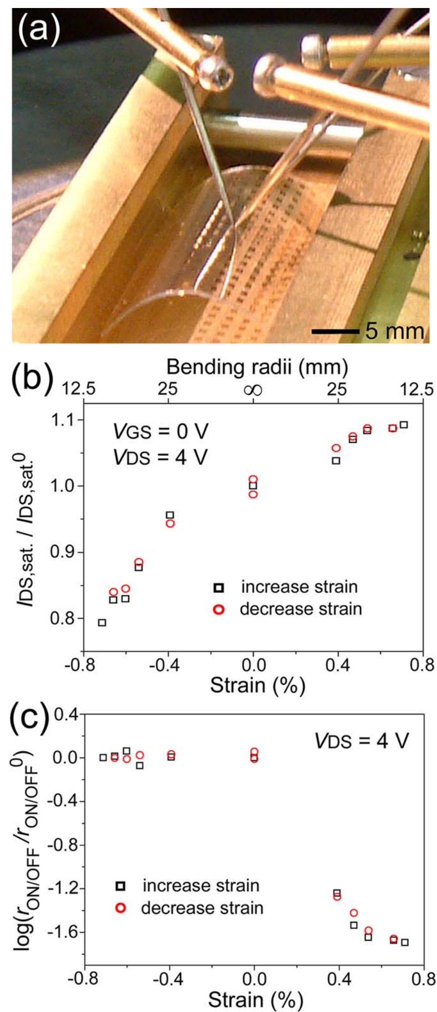

FIG. 3. (Color online) Characterization of the mechanical flexibility of high-speed GaAs-wire MESFETs (with gate length of 2 μm) on PU/PET substrates. (a) Optical image of the setup for the measurements. The effects of surface strain (positive and negative values correspond to tensile and compressive strains, respectively) on (b) the saturated current flow through source to drain at $V_{DS}=4$ V and $V_{GS}=0$ V, and (c) the on/off current ratio in the saturation region of $V_{DS}=4$ V. The superscript "0" represents the data measured from the unbent samples.

stress (the case similar to this work) can cause significant shifts in band-gap energy and valence-band splitting in the epilayers.[16,17] Tensile strains decrease the band-gap energy thereby increasing the total carrier concentration (electrons and holes) and enhancing the current flow. By contrast, compressive strains increase the band-gap energy and decrease the current flow. These phenomena are consistent with observations of our devices. At tensile strains above ~1%, device degradation occurs, due to fracture of some of the wires (or cracking of the gate electrodes).

Because the bending strains change the saturated currents by less than 20%, variations in the on/off ratio are determined mainly by changes in the off currents. The change of hole concentration in the valence band and the number of dislocations and surface defects of the *n*-GaAs layer induced by strain might contribute to the variation of the off current of the transistor. Both tensile and compressive strains can increase the number of dislocations and surface defects, thus increasing the off current of the device. The tensile strain generates additional holes as well as electrons, which will also increase the off current. Compressive strains, on the other hand, lower the hole concentration. As a result, the off current of the MESFET in tension is expected to be higher than that of an unstrained device. The compressive strain has minor effect on the off current of the device. The corresponding on/off current ratio, therefore, should decrease with tension and remains approximately the same with compression. Figure 3(c) gives the dependence of the measured on/off current ratio in the saturation region on strain, showing qualitative agreement with the discussion above.

In summary, the results presented here indicate that GaAs wire-based TFTs can achieve speeds approaching those suitable for rf communication devices and other applications, even with modest lithographic resolution. As a material, GaAs is interesting for these systems because of (i) the high intrinsic electron mobility of GaAs and its established applications in conventional high frequency circuits, (ii) the relatively simple processing and relaxed registration requirements for MESFETs, and (iii) the absence of parasitic overlap capacitances of the type that occur in non-self-aligned metal-oxide-semiconductor field-effect transistors (MOSFETs). These properties together with the good bending characteristics make GaAs wire-based transistors promising for applications where high speed, mechanical flexibility, lightweight construction, and compatibility with large-area, printinglike processing are needed.

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