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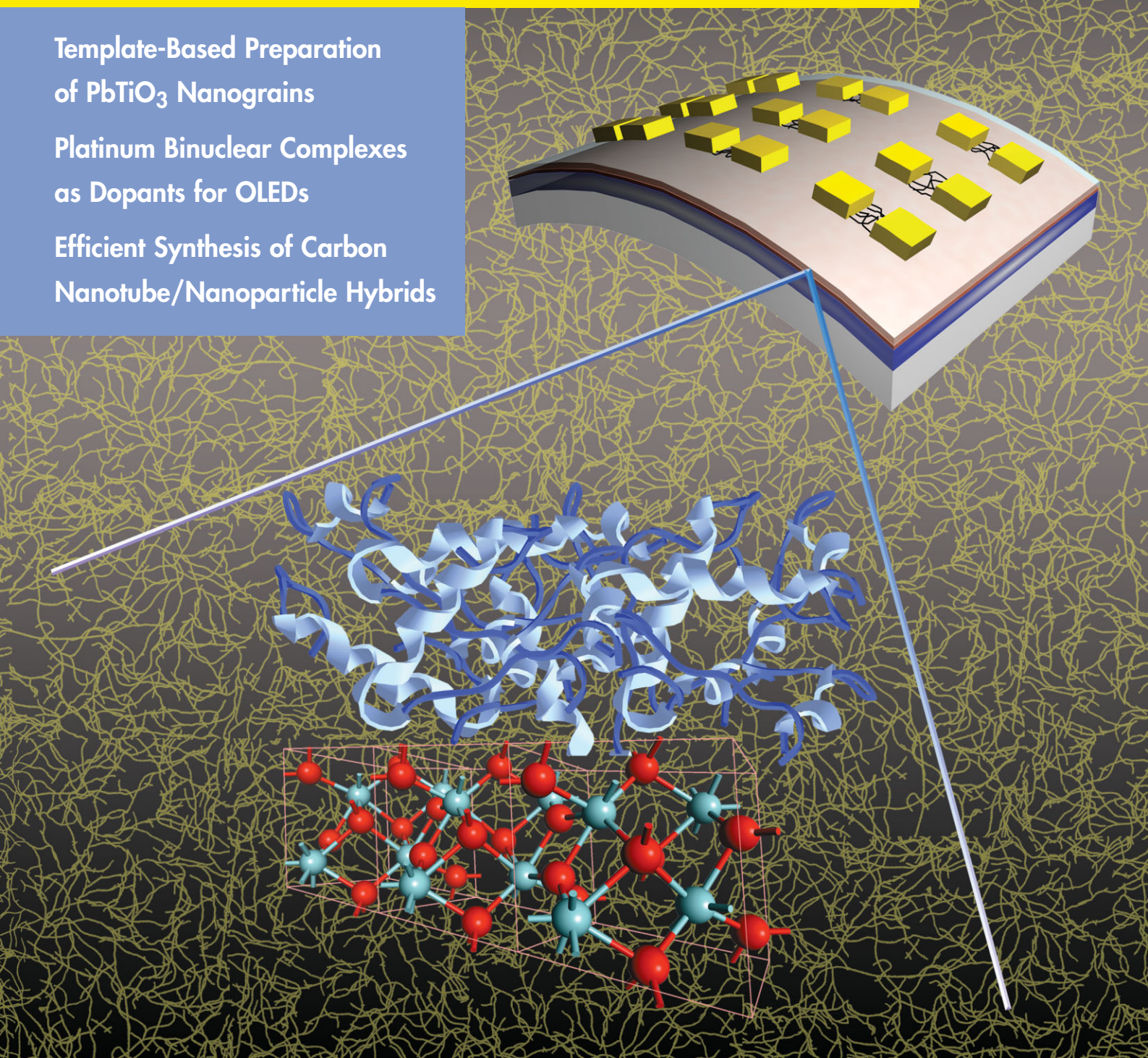
ADVANCED FUNCTIONAL MATERIALS

Organic/Inorganic Gate Dielectrics for Flexible Electronics

Template-Based Preparation of $PbTiO_3$ Nanograins

Platinum Binuclear Complexes as Dopants for OLEDs

Efficient Synthesis of Carbon Nanotube/Nanoparticle Hybrids



ADVANCED FUNCTIONAL MATERIALS

FULL PAPER

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Bilayer Organic–Inorganic Gate Dielectrics for High-Performance, Low-Voltage, Single-Walled Carbon Nanotube Thin-Film Transistors, Complementary Logic Gates, and p–n Diodes on Plastic Substrates**

By *Qing Cao*, *Ming-Gang Xia*, *Moonsub Shim*, and *John A. Rogers**

High-capacitance bilayer dielectrics based on atomic-layer-deposited HfO_2 and spin-cast epoxy are used with networks of single-walled carbon nanotubes (SWNTs) to enable low-voltage, hysteresis-free, and high-performance thin-film transistors (TFTs) on silicon and flexible plastic substrates. These HfO_2–epoxy dielectrics exhibit excellent properties including mechanical flexibility, large capacitance (up to ca. 330 nF cm^{-2}), and low leakage current (ca. 10^{-8} A cm^{-2}); their low-temperature (ca. 150 °C) deposition makes them compatible with a range of plastic substrates. Analysis and measurements of these dielectrics as gate insulators in SWNT TFTs illustrate several attractive characteristics for this application. Their compatibility with polymers used for charge-transfer doping of SWNTs is also demonstrated through the fabrication of n-channel SWNT TFTs, low-voltage p–n diodes, and complementary logic gates.

1. Introduction

The possibility of using random networks[1–3] or aligned arrays of single-walled carbon nanotubes (SWNTs)[4–6] as semiconducting or conducting thin-film-type materials in the emerging field of flexible and large-area electronics[7] has recently attracted some attention. The unique electrical, mechanical, and thermal properties of SWNTs, as demonstrated primarily through studies of single-tube devices such as transistors,[8] solar cells,[9] logic gates,[10] and ring oscillators,[11,12] make SWNTs a potentially attractive building block for thin-film devices. The absence of dangling bonds makes it possible for SWNTs to exhibit good electrical characteristics on a wide range of substrates, including plastics. This feature, combined with the ability to print the tubes at room temperature using dry transfer processes[13–15] or solution casting[16] make SWNT films potentially attractive for large-area and flexible electronics. Recent reports demonstrate that thin-film field-effect transistors (FETs) based on random networks of SWNTs can be successfully fabricated on plastic substrates, and that the resulting devices can achieve good electrical, mechanical, and even optical (e.g., transparency) properties.[13,17–20] Several major challenges must be overcome, however, in order to take full advantage of SWNT films for these applications. First, since as-grown carbon nanotubes are mixtures of metallic tubes and semiconducting tubes,[21,22] it is necessary to be able to grow semiconducting tubes only, perhaps by selective catalysis[23] or by plasma-enhanced chemical vapor deposition (CVD),[24] or to remove metallic tubes, perhaps by electrical breakdown[25,26] or chemical functionalization.[27–29] Several groups are working on these and related approaches, as they relate to applications of SWNTs in thin-film electronics as well as many other application areas. A second challenge, which is mainly related to active device applications, involves the development of materials for gate dielectrics that can be used to achieve high-performance n- and p-channel operation in SWNT TFTs, with low hysteresis, good mechanical properties, and compatibility for low-temperature plastic substrates.

The development of such gate dielectrics with high capacitance is crucial for applications of SWNT TFTs in low-power

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flexible electronics. High capacitance also leads to high transconductance (g_m) and improved subthreshold slope (S), both of which are important for switching in digital circuits. Examples of single-tube, top-gate devices have been achieved with either ultrathin SiO_2[30] deposited using CVD or high κ dielectric materials such as zirconium oxide,[31] hafnium oxide,[32] and titanium oxide[33] deposited using atomic layer deposition (ALD). Polymer electrolytes have also been used, although the switching speeds that can be achieved are modest.[34–36] The top-gate design has the disadvantage that the deposition process can, in some cases, damage the tubes and that the top-gate structure makes it difficult to apply electrical breakdown procedures to remove metallic pathways or to perform chemical functionalization of the nanotubes. Self-assembled mono-[37] and multilayer[38] dielectrics have been successfully used as high-capacitance dielectrics for TFTs that use small-molecule or polymer semiconductors in a bottom-gate configuration.[39] This type of design was also recently implemented with SWNT networks to yield promising properties including low-voltage and hysteresis-free operations.[40] These specialized materials have the disadvantage, however, that they must be deposited in a multiple-step dipping sequence whose implementation in large-area, high-speed processes will require further development. Other work demonstrated with small-molecule and polymer TFTs seeks to avoid these limitations through the use of ultrathin crosslinked polymers,[41,42] anodized metals,[43–45] ALD inorganic films,[46] and other materials for high-capacitance dielectrics.

We report, in this article, a high-capacitance dielectric based on a bilayer of high κ HfO_2 film deposited using ALD and an ultrathin layer of crosslinked epoxy formed by spin-casting. The resulting films can be formed easily, over large areas, and on a range of substrates including low-temperature plastics. Their properties are studied independently and through measurements of bottom-gate SWNT TFTs formed by transfer printing SWNT networks onto layers of these dielectrics deposited on either Si wafers or plastic substrates. Additional experiments demonstrate the ability to use polymer functionalization to obtain n-type SWNT TFTs, p–n diodes, and CMOS-type (CMOS: complementary metal oxide semiconductor) inverters.

2. Results and Discussion

2.1. Device Structure and Dielectric Synthesis

Figure 1a provides a schematic illustration of a bottom-gate SWNT TFT. Transfer-printing techniques that use poly(dimethylsiloxane) (PDMS; Sylgard 184, Dow Corning) stamps were used to form the devices, according to procedures described previously.[13] The behavior of SWNT TFTs can be described by the Shockley model for metal–insulator–semiconductor (MIS) FETs, although their operation can also be influenced by Schottky barriers at the contacts.[47] The drain–source current (I_{DS}) can be modulated by a gate–source voltage (V_{GS}) applied across the gate dielectric and can be expressed by

$$I_{DS} = \mu C_i W [(V_{GS} - V_T - 1/2\ V_{DS})V_{DS}]/L \quad (1)$$

in the linear region and

$$I_{DS} = \mu C_i W (V_{GS} - V_T)^2/2L \quad (2)$$

in the saturation region, where μ is the effective device mobility, W and L are the device channel width and channel length, respectively, V_T is the threshold voltage, and C_i is the capacitance of the gate dielectric. Increases in C_i enable operation at reduced V_{GS}, thereby decreasing the power consumption and increasing the switching speed and transconductance ($g_m = dI_{DS}/dV_{GS}$).

To form high C_i gate dielectrics for this application we used conventional ALD methods to deposit, at temperatures of

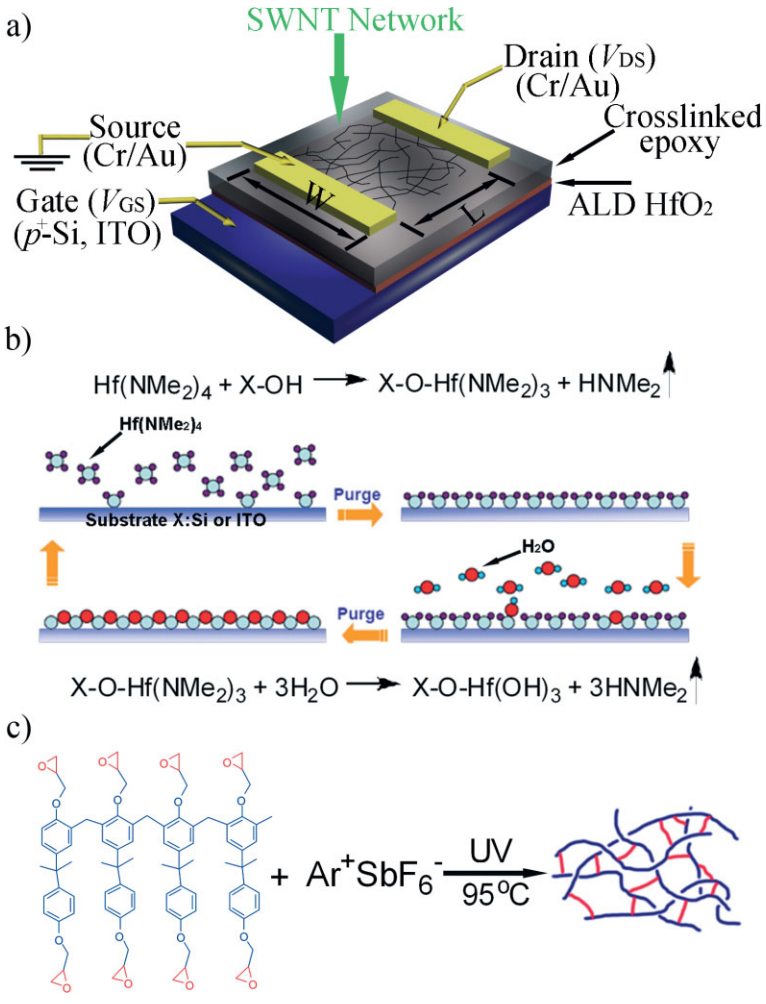

Figure 1. a) Schematic illustration of a bottom-gate single-walled carbon nanotube network TFT with a high-capacitance HfO_2–epoxy bilayer gate dielectric. V_{GS}: gate–source voltage; V_{DS}: drain–source voltage; ITO: indium tin oxide. b) ALD reaction sequence. c) Chemistry of the epoxy component of the bilayer dielectric.

ca. 150 °C, ultrathin films of HfO_2 on either Si wafer substrates or poly(ethyleneteraphtalate) (PET) films coated with indium tin oxide (ITO). The ALD cycle consists of a series of self-limiting surface reactions (Fig. 1b) to ensure the precise control of film thickness and to enable the formation of dense and pinhole-free films.[48] The approach can be applied to large areas with excellent reproducibility[49] and at low temperatures.[50] The crosslinked epoxy film that is implemented on top of the ALD layer is formed by spin-coating a precursor solution prepared using procedures described in the Experimental. The film thickness can be controlled by varying the concentration of precursors or the spinning speed. The precursors are polymerized by a cationic process initiated by the photogeneration of a Lewis acid (Fig. 1c). This epoxy film serves as an adhesion layer for high-yield transfer printing of the SWNT networks.

2.2. Dielectrics Characterization

Good surface uniformity of the gate dielectric is crucial for reliably fabricating devices over large areas and for decreasing possible scattering of carriers due to surface roughness.[51–53] Figure 2 shows atomic force microscopy (AFM) images of ALD HfO_2 and HfO_2–epoxy nanodielectrics on both Si wafer and PET substrates. For all cases the images indicate smooth (root-mean-square surface roughness 0.2–0.6 nm), defect-free films. The spin-cast epoxy layer increases this roughness slightly. The AFM images on ITO–PET were collected over 1 μm × 1μm areas to minimize the influence of substrate nonplanarity on the measurement.

Leakage current and capacitance measurements provided direct information on the dielectric characteristics of the HfO_2–epoxy bilayers. Capacitance–voltage (*C–V*) and conductance–voltage (*G–V*) measurements on MIS structures yielded both quasistatic and high-frequency (10^3 to 10^6 Hz) behaviors (Fig. 3a). The measured response was typical of MIS devices for voltage sweeping from accumulation (negative bias with respect to the metal contact) to inversion (positive bias with respect to the metal contact) with a p^+-Si wafer as the semiconductor substrate. The 0.2–0.4 V hysteresis in the high-frequency *C–V* curves and significant shift of the quasistatic *C–V* curves indicate that the HfO_2–epoxy layers have certain quantities of fixed positive charges and interface states. The fixed charges shift the flat-band voltage from the metal-semiconductor work-function difference; their density is estimated to be 4×10^{11} to 8×10^{11} cm^{-2}.[54] Application of the Hill method[55] yielded the interface state density. *C–V* and *G–V* data evaluated at 100 KHz were used for this calculation so that no correction on the parasitic resistance was required on the measured value.[56] Thus, the interface state density is of the order of 10^{12} eV^{-1} cm^{-2}, which is typical for high κ dielectrics (κ: dielectric constant).[57] Note here that this interface is between HfO_2 and Si, which is not directly relevant to the devices examined here. The interface trap density between the epoxy and SWNT is expected to be less due the absence of dangling bonds at the surface of the SWNTs.[58]

We measured the capacitances of a series of capacitors with different electrode areas. The capacitances were modeled as

$$C_{\text{total}} = PC_{\text{edge}} + AC_{\text{area}} \quad (3)$$

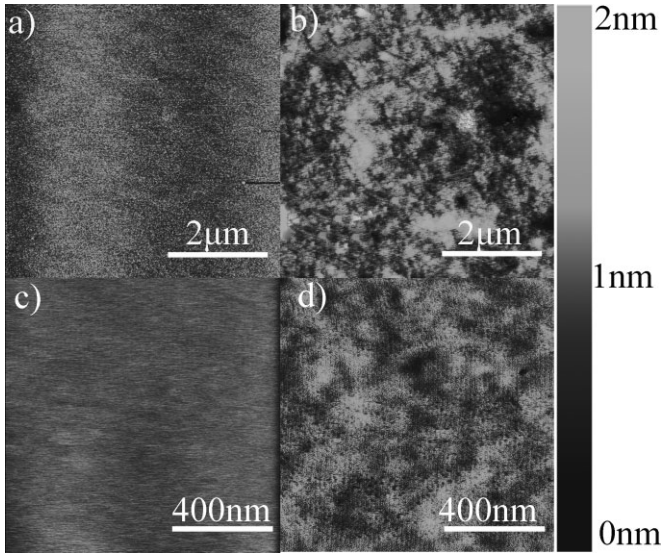

Figure 2. Tapping-mode AFM images of a) 5 nm HfO_2 on a p^+-Si wafer, b) 5 nm HfO_2 and 10 nm crosslinked epoxy on a p^+-Si wafer, c) 5 nm HfO_2 on ITO–PET, and d) 5 nm HfO_2 and 10 nm crosslinked epoxy on ITO–PET.

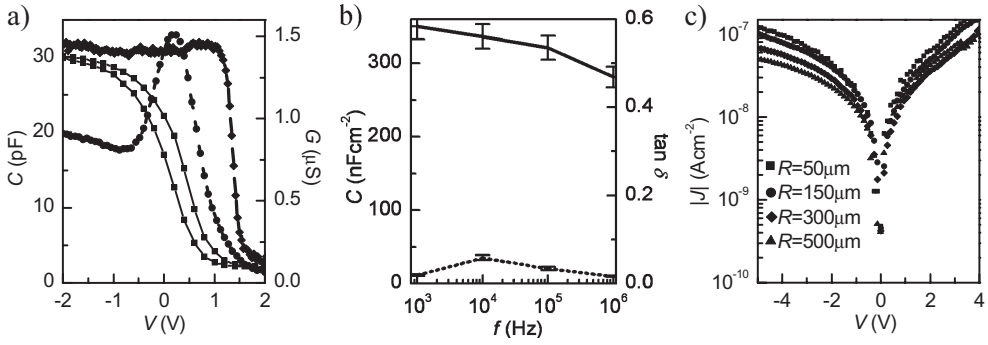

Figure 3. a) Quasistatic (dashed line) and high-frequency (10^5 Hz) *C–V* (solid line) and *G–V* (dotted line) curves of a disk-shaped MIS capacitor with a diameter of 100μm. b) Frequency (*f*) dependence of the capacitances (solid line) and dissipation factors (dashed line) evaluated between 10^3 and 10^6 Hz. c) Leakage *J* versus voltage (*V*) for HfO_2/crosslinked epoxy bilayer dielectrics measured on disk-shaped capacitors with different radii, *R*.

where C_{total} is the total capacitance of the given capacitor, P is the circumference of the round-shape metal pad, C_{edge} is the capacitance per unit length because of the edge effect, A is the area of the metal pad, and C_{area} is the capacitance per unit area. C_{area} is equal to 336 ± 15 nF cm^{-2} at 10^5 Hz with slightly higher values at lower frequencies. This capacitance is much higher than that of dielectrics (e.g., 100 nm SiO_2, ca. 30 nF cm^{-2}) that are often used for SWNT TFTs; it is also twice as large as recently reported results for multilayered organic nanodielectrics (ca. 170 nF cm^{-2}). The dissipation factors are in the range 10^{-1} to 10^{-2}, greater than those of thermal SiO_2. Figure 3c depicts the leakage current density (J) versus voltage for MIS capacitors with different metal-pad sizes. These consistently low current densities suggest that leakage is not dominated by isolated sparse defects, and that the low leakage can be obtained reproducibly. The low defect density of HfO_2–epoxy bilayer dielectrics is further corroborated by the high yield (>90 % for ca. 200 measured devices).

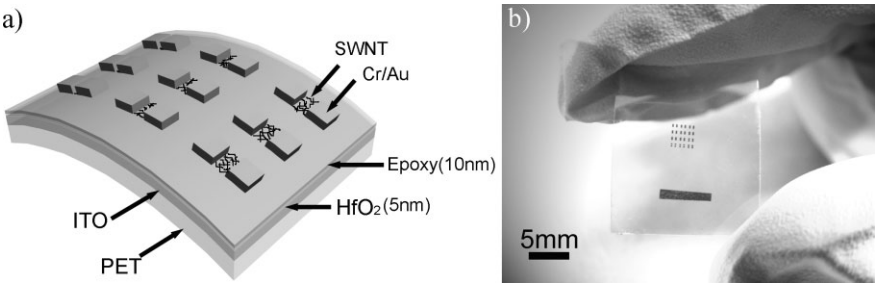

Figure 4. a) Schematic illustration and b) optical image of flexible, SWNT TFT devices that use HfO_2–epoxy bilayer dielectrics on an ITO–PET substrate.

2.3. Flexible SWNT TFTs Fabrication and Characterization

SWNT TFT arrays were fabricated on flexible ITO (ca. 100 nm)/PET (ca. 180 μm) substrates with HfO_2–epoxy nanodielectrics. Figure 4a shows a schematic illustration of these SWNT TFT arrays. A piece of PET film coated with ITO served as a flexible substrate and back gate. We thermally cycled the ITO/PET between 30 and 180 °C while it was laminated against a thin piece of PDMS chemically bonded to a glass slide (Corning Glass) to improve its dimensional stability during ALD processing.[59] Exposing the ITO/PET to ultraviolet induced ozone created a hydrophilic surface on which the HfO_2 (5 nm) and epoxy (10 nm) layers were deposited. Transfer-printing techniques placed networks of SWNTs grown by CVD on SiO_2/Si substrates directly onto the epoxy–HfO_2–ITO–PET substrate stacks. This process used previously published approaches,[13] but with neutral gold etchants ($KI + I_2$) and basic chromium etchants ($K_3Fe(CN)_6 + NaOH$) to avoid etching of the ITO gate. Photolithography and liftoff defined source–drain electrodes of Cr/Au directly on top of the transfer-printed SWNT layer. Cutting strips (5 μm wide spaced by 5 μm, and oriented parallel to the direction of current flow in the channels) in the SWNT networks with oxygen plasma etching (Plasmatherm reactive-ion-etch system, 20 sccm O_2 flow with a chamber base pressure of 100 mTorr (1 Torr = 133.322 Pa), 100 W RF power for 60 s) through a photopatterned layer of photoresist (Shipley 1805, Shipley, USA) electrically isolated individual TFTs and completed the fabrication process.[26] Figure 4b shows an optical image of the device arrays on the PET substrate.

Current–voltage (I–V) measurements were performed on devices fabricated with SWNT networks whose tube densities are much higher than the percolation threshold[60,61] (see Fig. 5a). Figure 5b shows the transfer curves of devices with different channel lengths. The devices exhibit little hysteresis, which is in sharp contrast with devices built on thicker gate dielectrics and is similar to our previous devices utilizing ultrathin organic multilayers as the gate dielectric.[40] The threshold voltage (V_T) is 0.3 ± 0.05 V and does not vary substantially with channel length over this range. The on current (I_{ON}) scales linearly with the reciprocal of the channel length, consistent with device operation that is not contact limited. I_{DS}–V_{DS} curves of these devices show current saturation when $V_{DS} > V_{GS} - V_T$ (Fig. 5c), which is typical for well-designed transistors. Figure 5d shows

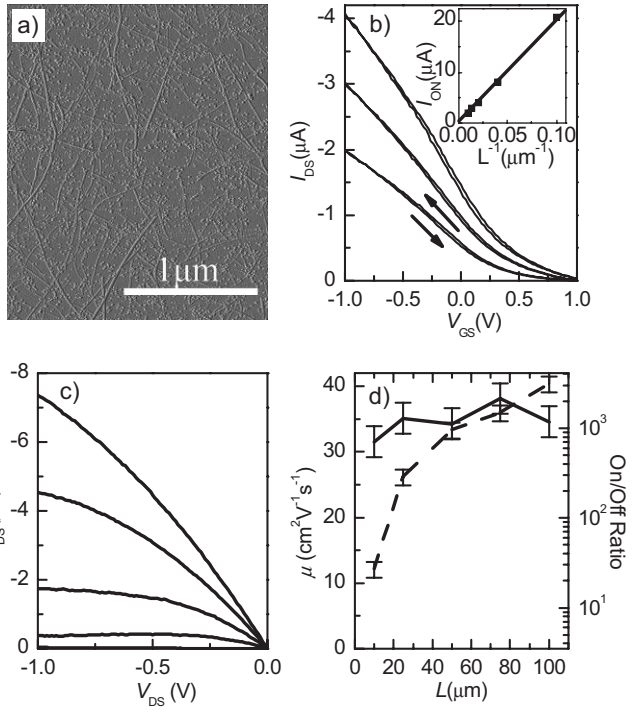

Figure 5. a) AFM image of part of a SWNT network in the channel region of a TFT device. b) Transfer curves of SWNT TFTs with an HfO_2–epoxy dielectric, supported by a plastic substrate, and with channel lengths, from top to bottom, of 50 μm, 75 μm, and 100 μm. The channel width in each case is 250 μm. V_{DS} is –0.2 V. Inset: I_{ON} versus the reciprocal of channel length ($1/L$). c) I–V characteristics of a device with a channel length of 100 μm and channel width of 250 μm. The gate voltage varies between –1 and 1 V in steps of 0.5 V. d) Effective mobilities (μ, solid line) calculated considering the effect of fringing field and on/off ratios (dash line) as a function of channel length for a typical set of devices.

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linear region effective device mobilities, which are calculated considering the fringing field effect on the device gate capacitance,[18,62] and on/off ratios as a function of channel length. The detailed analysis and studies of the fringing field effect on capacitance coupling, which is important for the analysis of data obtained from these devices, and hysteresis will be reported elsewhere.[63] The mobilities, extracted while taking the effect of fringing field into consideration, are comparable to devices made on Si wafers with either HfO_2–epoxy nanodielectrics or with thick (ca. 100 nm) thermal SiO_2 dielectrics (to the extent that they can be estimated reliably in the presence of large hysteresis). The channel length independent device mobilities are consistent with contact resistances that are negligible for the range of channel lengths studied here. The on/off ratio depends strongly on channel length because of the increasing probability of all metallic transport pathways with decreasing channel length. At long channel lengths, on/off ratios of ca. 10^3 can be achieved. Both the SWNT networks and HfO_2–epoxy nanodielectrics are inert materials. We did not observe any change in device characteristics over several months of storage in ambient air.

The mechanical robustness of the devices, which is limited mainly by the flexibility of HfO_2–epoxy nanodielectrics, was examined through a series of bending tests with systems described previously.[64] Figure 6a shows the change of transfer curves of a typical device under tensile strain. Only small variations were observed for strains up to 1 %. The small decrease of on current and device mobility (Fig. 6b) may be caused by the influence of strain on the contact between Au electrodes and SWNT films.[13] For strains larger than 1 %, large leakage currents resulting from gate shorting were evident in most devices. Although the fracture strain of HfO_2–epoxy nanodielectrics is inferior to most polymer dielectrics,[65] the degrees of bendability achieved here are sufficient for most applications in flexible electronics.

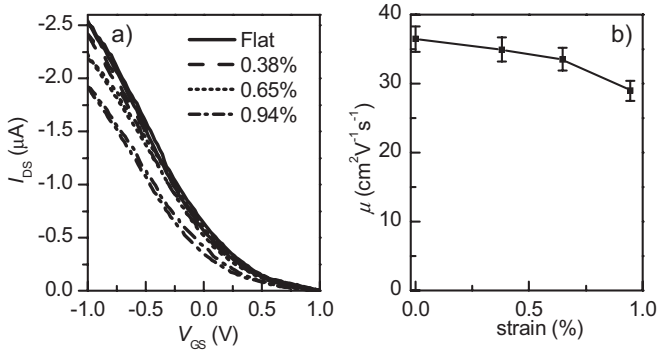

Figure 6. a) Transfer curves of a device with channel length of 75 μm and channel width of 250 μm at various levels of bending-induced tensile strains. V_{DS} is fixed at –0.2 V. b) Variation of device mobility (μ) with tensile strain.

2.4. Subthreshold Behavior of SWNT TFTs Based on HfO_2–Epoxy Nanodielectrics

For many circuit applications, the subthreshold slope (S) is an important characteristic because it determines the change in gate voltage needed to turn the device off and on. Low-power circuits demand small S and V_T. The value of the S is determined by the gate capacitance and the capacitance resulting from interface traps, C_{IT}, according to

$$S = (k_B T/e)\ln(10)(1 + C_{IT}/C_i)^{[66]} \quad (4)$$

The room-temperature limit, 60 mV dec^{-1}, can be accomplished in single-tubed devices with either electrolyte gating[34] or 2–3 nm ALD HfO_2 dielectrics deposited conformally on DNA-functionalized SWNTs.[67] However, in network devices, only relatively large S values (800–2500 mV dec^{-1}) have been reported. With HfO_2–epoxy dielectrics, S as small as 280 mV dec^{-1}was achieved in devices with 100 μm channel lengths (Fig. 7a). This low value results partly from a small C_{IT}/C_i, because of a large C_i. This value represents substantial progress over devices fabricated with lower capacitance dielectrics, but it is still much higher than the theoretical limit. There are three possible reasons for this nonideal value. First, C_{IT} could be much larger than C_i even for devices based on high-capacitance nanodielectrics. To test this argument, we fabricated a set of devices using only the HfO_2 layer (5 nm) as the gate dielectric, by using a kinetically controlled transfer-printing technique.[68] Such devices exhibit, however, only a marginal improvement of S, that is, from 280 to 260 mV dec^{-1} (Fig. 7b), despite the significant increase of C_i. This result suggests that the interface traps between the SWNT film and gate

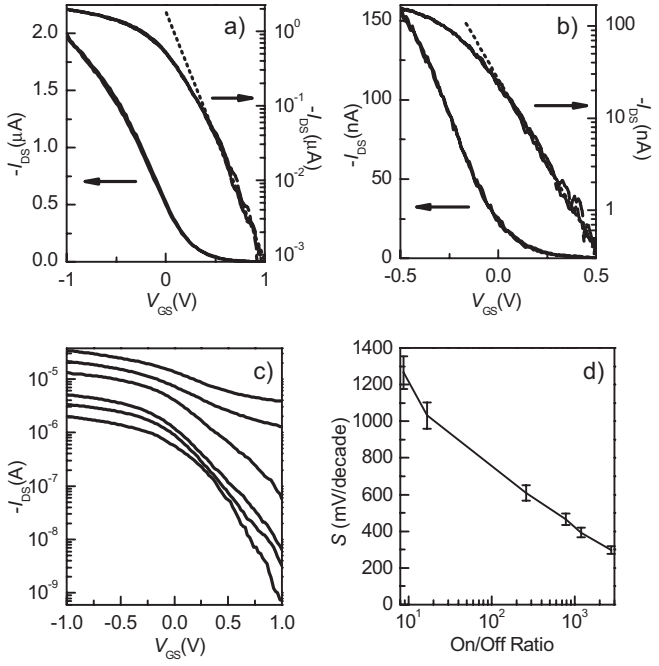

Figure 7. Transfer characteristics plotted for devices that use a) 5 nm HfO_2 and 10 nm crosslinked epoxy or b) 5 nm HfO_2 as the gate dielectric. In both cases, the channel width and length are 250 and 100 μm, respectively. V_{DS} is –0.2 V. The dotted lines indicate the slope used to determine S. c) Transfer characteristics of devices with different channel lengths. The channel lengths are, from top to bottom, 5, 10, 30, 50, 75, and 100 μm. The channel widths are 250 μm. The V_{DS} is –0.2 V. d) S versus device on/off ratios.

dielectrics are not the major reason for the higher than expected S values. (The lower current levels of devices with only the HfO_2 layer as the dielectric results from the poor transfer-printing efficiency in this case.) A second possibility is that the relatively low on/off ratios degrade the subthreshold performance because conduction through the metallic tubes does not change with V_{GS}. A channel-length scaling analysis of S, which shows that S decreases rapidly with increasing on/off ratio, suggests that conduction through metallic network pathways is the most important reason for nonideal performances (Fig. 7c and d). This effect is not explicitly included in Equation 4, which applies to devices with high on/off ratios. The third possibility is that the cylindrical shape of the SWNTs makes the bottom-gate structure inferior to top-gate structures in terms of electrostatic coupling between V_{GS} and the channel, which may account, together with the capacitance difference, for the larger S with our HfO_2–epoxy nanodielectrics than that obtained from polymer-electrolyte gatings at similar on/off ratios.[36]

2.5. n-Type Devices and Complimentary Logic Gates

Controlling charge-carrier type is crucial for electronic circuit design. Pristine nanotubes typically lead to p-channel operation in transistors, when high-work-function metals are used for the source and drain. Single-tube devices with n-channel operation can be achieved by charge-transfer doping with alkaline metals[69,70] or amine-containing molecules,[71–73] by surface passivation,[74] by use of low-work-function metal contacts[75] or by nitrogen-atom doping.[76] Here, we demonstrate the compatibility of the HfO_2–epoxy dielectrics with charge-transfer induced polarity switching with polyethyleneimine (PEI) coatings[77] using procedures described previously.[26] In n-channel mode, the devices exhibit very low hysteresis (Fig. 8a) with good scaling properties with channel lengths, similar to observations on p-channel devices. The average device mobility extracted from linear region considering the fringing field effect was at $13 \pm 2\ cm^2\ V^{-1}\ s^{-1}$. Sweeping the gate voltage from negative to positive leads to a negative shift of threshold voltage in the reverse scan, which indicates that holes are trapped at the dielectrics in these n-type devices. This behavior is opposite to the electron trapping observed in p-type devices and indicates that surface traps mainly affect the more abundant carrier type. Figure 8b shows I_{DS}–V_{DS} characteristics of a typical n-channel device.

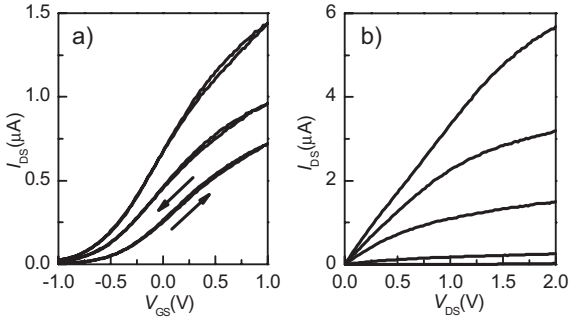

Figure 8. a) Transfer curves of SWNT TFTs that use HfO_2–epoxy dielectrics with channel lengths, from top to bottom, of 50, 75, and 100 μm after uniformly coating the channel regions with PEI. The channel widths are 250 μm. V_{DS} is 0.2 V. b) I–V characteristics of a device with a channel length and width of 100 and 250 μm, respectively. The gate voltage varies between –1 and 1 V in steps of 0.5 V.

As a consequence of the compatibility of the HfO_2–epoxy dielectrics with both p- and n-channel SWNT TFTs, the fabrication of p–n diodes and complementary logic devices is possible. Such diodes are important in microelectronics and nanotube-based p–n diodes have been demonstrated by means of chemical doping[78] and electrostatic doping.[79,80] The p–n diodes here were fabricated by covering half of the channel of the SWNT TFTs with PEI. Transport measurements clearly show current rectification and low turn-on voltage (Fig. 9a). A complementary type inverter was fabricated by integrating a p-channel and an n-channel SWNT TFT. These two devices were biased in the configuration depicted in the inset of Figure 9b. The high transconductances and on/off ratios enable gains (ca. 8) that are much better than those achieved with thick dielectrics;[81–84] they are comparable to SWNT network CMOS inverters fabricated with organic multilayer nanodielectrics[40] and single-tube inverters based on local bottom-gated devices.[11]

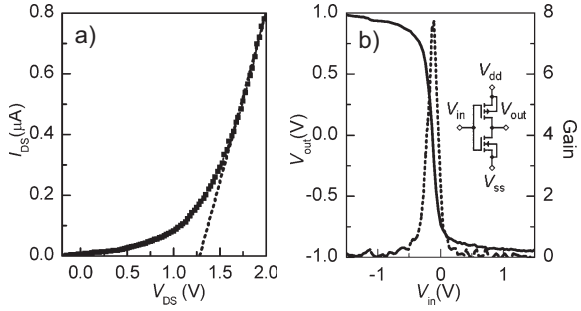

Figure 9. a) Transfer characteristics of a p–n diode (L = 100 μm, W = 200 μm). The dotted line shows the turn-on voltage of this diode. The p–n diode is formed by patterning PEI onto one half of the channel region, such that one half of the channel is p-type and the other half is n-type. b) V_{out} versus V_{in} curve for an inverter formed with p- and n-type SWNT TFTs based on HfO_2–epoxy dielectrics. The inset shows the circuit diagram of this inverter.

3. Conclusions

This paper demonstrates that a bilayer stack of HfO_2 and epoxy affords a robust, smooth, pinhole free, high capacitance, and low-leakage gate dielectric for SWNT TFTs that can be fabricated easily on both Si wafers and plastics by use of transfer-printing methods. The experimental results illuminate properties of these dielectrics and their behavior in TFTs. Transistors based on SWNT networks, including hysteresis-free p- and n-type SWNT TFTs with small subthreshold slope, p–n diodes, and high-gain complementary logic gates that operate at low voltages were realized. The results indicate that this type of dielectric can be useful in the development of nanotube-based thin-film-type electronic systems.

4. Experimental

Reagents: HfO_2 ALD films were grown using H_2O and $Hf(NMe_2)_4$ (Me: methyl, Aldrich, 99.99 + %). The carrier gas in the ALD reactor was N_2 (Matheson Tri-Gas, 99.9995 %). Photocurable epoxy solutions were prepared by diluting commercially available precursors (SU-8 2, Microchem) with cyclopentanone (SU-8 2000 thinner, Microchem) at different volumetric ratios. The gold etchant was prepared by mixing 5 % I_2 (Sigma–Aldrich, 99.99 %), 10 % KI (Sigma, 99.0 %) and 85 % dionized water. The chromium etchant was prepared by dissolving a small amount of NaOH (Sigma–Aldrich, 85.0 %) in saturated $K_3Fe(CN)_6$ (Sigma–Aldrich, 99.99 %) aqueous solution.

Materials: p^+-Si wafers (Montco Silicon Tech) and ITO-coated PET films (≤10 Ω/sq, Delta Technologies) were cleaned according to standard procedures [85] and exposed to UV ozone for 3 min before ALD deposition to remove possible fluorine contamination [86] and to render the surface hydrophilic.

Film Fabrication: SWNT networks were synthesized as previously described [20]. The ALD HfO_2 film was deposited with a commercial ALD reactor (Savannah 100, Cambridge Nanotech.). One ALD reaction cycle consisted of one dose of water followed by a 2 s exposure and 5 s purge and then one dose of $Hf(NMe_2)_4$ followed by another 2 s exposure and 5 s purge. During deposition, the nitrogen flow was fixed at 20 sccm and the chamber temperature was set at 150 °C. The deposition rate for hafnium oxide was 0.093 nm per cycle. For crosslinked epoxy film fabrication, the precursor solution was spin-coated at 4000 rpm, baked at 65 °C and 95 °C for 1 min each, exposed with an i-line (365 nm) UV lamp at an intensity of 15.0 mW cm^{-2} for 12 s, and then cured at 95 and 120 °C for 1 min to afford a 10 ± 1 nm thick film.

Film Characterization: The thicknesses of the hafnium oxide ALD films, the tube density of SWNT networks, and the surface morphologies of all thin films were evaluated using AFM (Dimension 3100 atomic force microscope, Digital Instruments) in tapping mode. The thicknesses of the epoxy films were measured using a profilometer (Dektak 3030).

Electrical Measurement: SWNT TFT measurements were carried out in air using a semiconductor parameter analyzer (Agilent 4155C), operated using an Agilent Metrics I/CV Lite program and GBIP communication. Triaxial and coaxial shielding was incorporated into a Signatone probe station to achieve better signal/noise ratio. Agilent 4282A precision LCR (inductance, capacitance, and resistance) meter was used for capacitance and impedance measurements.

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