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the protein adsorption assay, and onto a glass substrate for the cell and platelet adhesion assay. The samples were subsequently heated to 100 °C under vacuum for 1 h. It was confirmed by XPS (O/C atomic ratio) that the surface structure of the present sample (heated at 100 °C for 1 h) was almost the same as that of the equilibrated sample[8], which was heated at 140 °C for 12–24 h.

Surface Analysis: The surfaces of the samples were observed using an SEM (XL30, FEI Japan Ltd., Japan), a profile measurement microscope (VF-7500, Keyence Co., Japan), and an XPS (Quantum 2000, Ulvac-Phi Inc., Japan). In the XPS measurements, monochromated Al Kα X-rays were used as the source, and the photoelectron take-off angle was set at 45°.

Protein Adsorption Assay: The samples were immersed in 2 mL of a phosphate-buffered saline (PBS), supplemented with fibrinogen (40 μg mL^{-1}, Sigma-Aldrich, USA) or albumin (460 μg mL^{-1}, Sigma-Aldrich., USA) at 37 °C for 2 h. After removal from the saline solution, the samples were gently rinsed with PBS three times, and then dried. The N/C atomic ratio on the sample surface was determined from XPS measurements.

Cell Adhesion Assay: The samples were placed in a 24-well PS plate. The L929 cells (Riken Bioresource Center, Japan) were suspended in Dulbecco's modified eagle medium supplemented with 5 % horse serum at a concentration of 1.2×10^5 cells mL^{-1}. 2 mL of the cell suspensions were added to the samples in each well, and the cells were cultured at 37 °C in a 5 % CO_2 atmosphere for 20 h. After cell culturing, the samples were gently rinsed with PBS three times. Cells adhering to the sample surface were detached from the samples using an ethylenediaminetetraacetic acid (EDTA)-trypsin solution, and then stained with trypan blue. The number of stained cells was counted using a hemocytometer.

Platelet Adhesion Assay: Blood was collected in a heparin-containing polypropylene tube from a 22-year-old man with his consent. The blood, containing 2 U mL^{-1} of heparin, was centrifuged twice at 160 g to obtain platelet-rich plasma. This was then centrifuged at 1300 g for 10 min to separate the platelets from the plasma. The platelets were labeled with 5- or 6-(*N*-succinimidyloxycarbonyl)-3′,6′-*O*,*O*′-diacetylfluorescein at 37 °C for 30 min, and then centrifuged at 1300 g for 10 min. The labeled platelets were then suspended in the supernatant fluid separated centrifugally from the platelet-rich plasma at a near physiological concentration of 1.0×10^5 platelets mL^{-1}. The samples, PMMA (negative control), and HUVEC (positive control) were subjected to a shear flow of the platelet suspension at a rate of 50 s^{-1} using a cone and plate-type viscometer[9] equipped with a microscope and a silicon-intensified target camera. The number of platelets adhering to the sample was counted at 5, 10, and 15 min after imposing the shear flow.

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Large-Area, Selective Transfer of Microstructured Silicon: A Printing-Based Approach to High-Performance Thin-Film Transistors Supported on Flexible Substrates**

By *Keon Jae Lee*, *Michael J. Motala*, *Matthew A. Meitl*, *William R. Childs*, *Etienne Menard*, *Anne K. Shim*, *John A. Rogers*, and *Ralph G. Nuzzo**

The advanced information technologies that shape the structure of modern society depend critically on the use of microelectronic devices, ones that involve ever-increasing higher densities of integration. From the initial integrated circuits (ICs) of the late 1950s, ones that incorporated fewer than four transistors,[1] current state-of-the-art ICs now integrate millions of transistors in an essentially equivalently sized package.[2] There has been an increased interest, however, in developing new device form factors, ones in which the capabilities of semiconductor devices are embedded in structures involving either large-area and/or flexible-material supports using fabrication methods that attempt to decrease costs while maintaining high device-performance levels.[3–7] Such device

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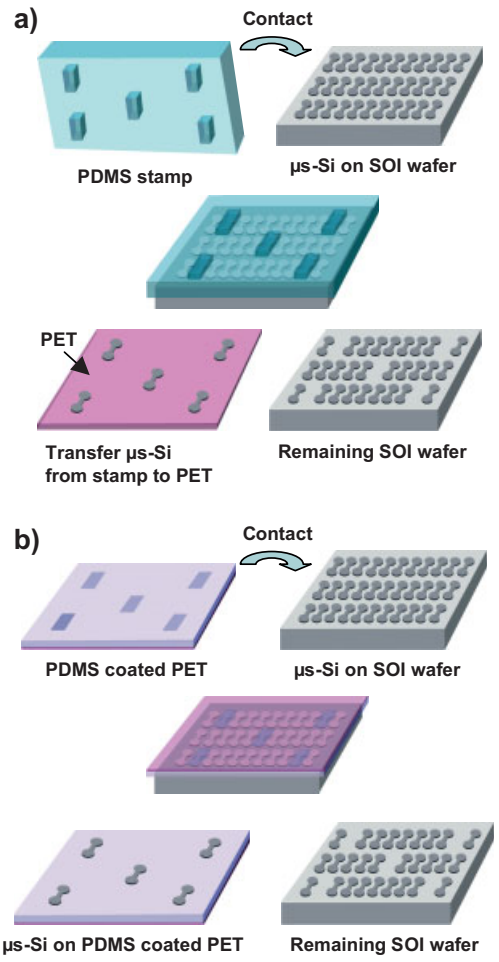
technologies could find wide application as active-matrix pixel display drivers and components of radio frequency identification (RFID) tags.[7–10] Recent reports detail the use of solution-processing methods to construct models of such circuits, notably ones based on semiconductor nanowires (NWs)[11] or networked nanotubes.[12] The devices prepared in these ways show great promise, with effective mobilities of ~2 $cm^2 V^{-1} s^{-1}$[11] and ~40 $cm^2 V^{-1} s^{-1}$[12], respectively, being obtained in simple thin-film transistors (TFTs). In a previous publication, we described a "top–down" fabrication strategy using microstructured single-crystalline silicon (μs-Si) ribbons harvested from silicon-on-insulator (SOI) wafers for use in ultra-high-performance TFTs.[3] This fabrication technique is a reasonably general one and has been extended recently to other industrially useful semiconductor materials that include GaN, InP, and GaAs.[13–15]

We describe in this paper an important step in the advancement of this technology: the development of a method which allows the selective transfer and accurate registration of silicon ribbons across large areas, a printing procedure applicable to both rigid (i.e., glass) and flexible plastic substrates. We specifically report here two methods that can be used to selectively remove μs-Si from an SOI wafer and subsequently transfer them in patterned forms onto a plastic substrate. The processes, for convenience referred to here as Method I and Method II, use different mechanisms of adhesive bonding to effect the printing-based pattern transfer of μs-Si. Method I exploits physical bonding between a molded Sylgard 3600 polydimethylsiloxane (PDMS) stamp (a new experimental, high-modulus PDMS product provided by the Dow Corning Corp.) and μs-Si objects. Method II uses a recently developed masterless soft-lithography technique[16] to chemically bond the μs-Si to a PDMS-coated substrate.

In Method I, shown in Scheme 1a, a peanut-shaped photoresist pattern was developed on top of a SOI substrate using standard photolithography techniques. Plasma etching, followed by resist stripping, yielded μs-Si "peanuts" that were supported on top of a buried oxide layer. This sample was then incompletely etched using HF to give undercut peanuts held only by a residual oxide layer present at the dumbbell ends of the μs-Si. The SOI wafer was then laminated with a hard 3600 PDMS stamp molded with features corresponding to the latent image of the desired pattern. The raised features of the stamp correspond to regions where μs-Si was removed selectively from the SOI surface due to strong autoadhesion to the PDMS. The stamp, after peeling it away from the SOI wafer, was then placed in contact with a poly(ethylene terephthalate) (PET) sheet coated with polyurethane (PU) that had been partially cured using a UV lamp. A bar-coating technique was used to deposit the PU adhesion layer to ensure a uniform coating thickness over the large area of the 600 cm^2 plastic substrate. The stamp bearing the μs-Si was then placed in contact with the PU-coated side of the plastic sheet, and a second UV/ozone (UVO) exposure was then performed from the PET side of the sandwich to fully cure the PU and enhance its bonding to the μs-Si. Peeling the stamp from the plastic substrate resulted in the detachment of the μs-Si from the PDMS, completing the transfer to the PU-coated substrate.



Scheme 1. Schematic illustration of steps for selective transfer of μs-Si onto poly(ethylene terephthalate) plastic substrate a) using patterned hard PDMS (Method I); b) using masterless soft lithography (Method II).

Method II is depicted in Scheme 1b. This recently reported decal-transfer lithography (DTL) technique[16] effects the pattern transfer by using a flat, unmolded PDMS slab that is photochemically treated to provide spatially modulated strengths of adhesion. To do so, an UVO treatment was patterned across the surface of a slab of conventional Sylgard 184 PDMS using a microreactor photomask to pattern the UVO modification with high spatial resolution. After exposure, the photochemically modified PDMS-coated PET was placed in contact with a peanut-presenting SOI wafer and heated to 70 °C for 30 min. The fabrication of the peanut shapes on the SOI wafer followed the same procedures of Method I, with the addition of evaporating a thin film of SiO_2 (5 nm) onto the surface after the HF-etching step. This layer facilitates strong chemical bonding to the PDMS. After heating, the PDMS was peeled from the SOI, resulting in patterned transfer of μs-Si to the UVO-modified regions of the PDMS.

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Figure 1a shows the design of the so-called peanut-shaped μs-Si objects. The peanut shape was selected because its ends are slightly wider than the body of the structure. Upon etching the underlying oxide layer in an HF solution, the timing can

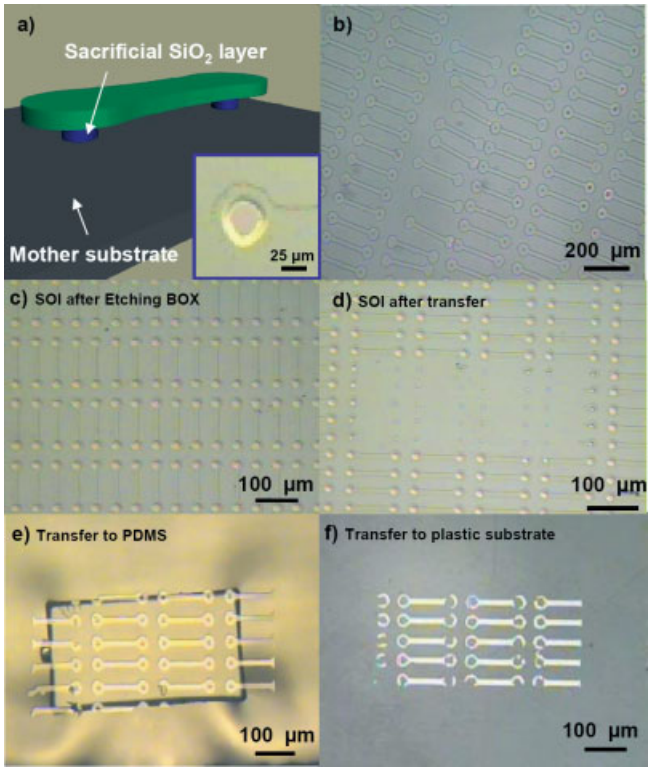

Figure 1. Top image: a) Schematic illustration of the μs-Si peanut that was supported by an underlying sacrificial SiO_2 layer. Without this sacrificial layer, the μs-Si objects would be lost in the HF solution. Inset: the optical image shows the result of optimized HF etching conditions where the buried oxide under the channel is removed while a sacrificial SiO_2 portion remains. b) Si objects to start to float in the HF solution when the sample was over-etched in HF solution. c–f) Micrographs depicting each step of the μs-Si transferred by Method I. c) The μs-Si on the SOI wafer after optimized HF etching. d) SOI wafer after the PDMS stamp removed a portion of the μs-Si. e) μs-Si portion on the PDMS stamp. f) The μs-Si that adhered to the PU support on the plastic.

be optimized such that the oxide layer under the center is completely removed while a sacrificial portion of SiO_2 still remains at either end (the dumbbell region seen in Fig. 1a, inset). It is this residual SiO_2 layer that holds the μs-Si in its original position; without this oxide bridge layer, the order of the μs-Si created on the SOI wafer by photolithography would be lost (an example of which is shown in Fig. 1b). When the μs-Si is removed from the SOI wafer by either Method I or II, fracture occurs at the edges of the sacrificial region. Figures 1c–f show a series of micrographs that depicts the progression of each step of the μs-Si transfer as effected using Method I. Figure 1c shows the μs-Si on the SOI wafer after the HF undercut-etching step. As shown in Figure 1d, the PDMS stamp has removed a portion of the μs-Si, leaving the neighboring regions intact on the SOI. Since the unused microstructured silicon objects on the SOI wafer are retained at their original positions, they can be picked up by a stamp and transferred in subsequent printing steps (see below). An example of the μs-Si structures transferred to the PDMS stamp is shown in Figure 1e. The missing center of each end of the μs-Si ribbons reveals the pattern of the fracture that occurs during the transfer of the microstructured silicon from the SOI to the PDMS stamp. Figure 1f shows a representative result for a second transfer of the μs-Si (this time from the PDMS stamp to the PU-coated plastic substrate).

Multiple transfers are possible from a small PDMS stamp to a larger plastic surface. Figure 2a shows an example of a large area (15 cm × 15 cm) transfer where the μs-Si was sparsely transferred onto a plastic substrate by multiple transfers

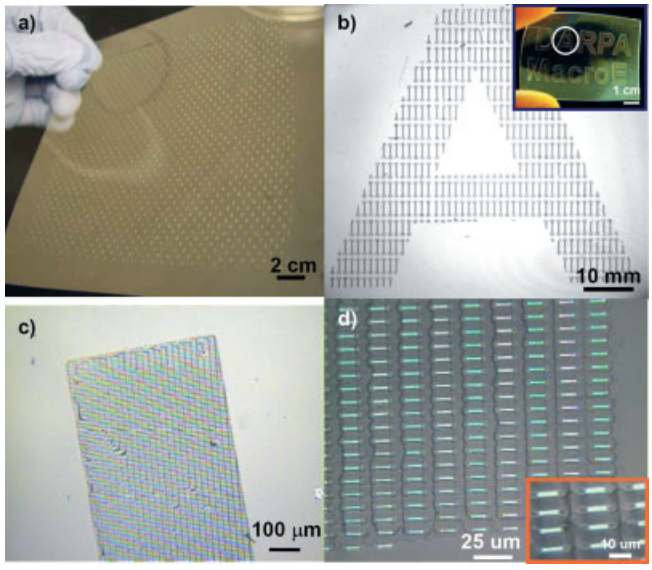

Figure 2. a,b) Optical images of the selective transfer of μs-Si onto a PU/PET sheet by a 3600 PDMS stamp (Method I). a) Large-area (15 cm × 15 cm) transfer where the μs-Si was deposited on the plastic by multiple transfers from a one-fourth-sized mold. Each pixel of the array shown in (a) consists of a microarray of semiconductor structural elements of the same configuration as that shown in Figure 1f and follows the same protocol described for Figures 1c–e. b) A blowup image of "DARPA macroE" written on the PET substrate showing how it is composed of smaller peanut-shaped μs-Si objects (the inset shows the overall image). c,d) The optical images of the selective transfer of μs-Si onto PDMS/PET sheet by masterless soft lithography (Method II). c) μs-Si was transferred selectively to the rectangular unit of the PET sheet corresponding to the 184 PDMS area that was irradiated by UVO. d) A blowup image of μs-Si selectively transferred to a PET sheet.

using a 8 cm × 8 cm stamp. Each pixel of the array shown in Figure 2a consists of a microarray of semiconductor structural elements of the same configuration as that shown in Figure 1f and follows the same protocol described for Figures 1c–e. The inset of Figure 2b shows a more complex molded form: "DARPA macroE" was written with peanut μs-Si objects smaller in size than those highlighted in Figure 1. The high

pattern fidelity of the transfer is illustrated by the qualities of the objects defining the letter "A" (circled in the inset image) as shown in Figure 2b. These data demonstrate that only those areas directly touched by the stamp ultimately transfer to the plastic substrate. We note that this transfer is not possible using conventional Sylgard 184 PDMS for two reasons. First, Sylgard 184 sags when the separation distances between features exceeds twenty times the feature height.[17,18] The examples shown here embrace such design rules, and thus preclude high-fidelity transfers using the lower-modulus polymer. Second, we also found that Sylgard 184 does not have enough adhesive force to pick up every μs-Si peanut from the SOI wafer, and defects were quite common using stamps prepared from this polymer. The 3600 PDMS from Dow Corning does not appreciably sag, even at an aspect ratio of 1:200. More importantly, this polymer—as a result of its greater modulus—has a higher yield stress than the conventional Sylgard polymer. This results in a much improved fidelity in the pattern transfer for the modest strain rates used in this work.

An example of a μs-Si transfer carried out using Method II is shown in Figures 2c,d. Figure 2c is an optical micrograph of a section of a Sylgard 184-coated PET substrate to which the μs-Si has been chemically bonded and subsequently transferred. A higher magnification image of the μs-Si transferred in this way is shown in Figure 2d. It should be noted that the dimensions of the peanuts used in this demonstration are smaller still than those previously discussed (ribbon widths of 25 μm). We found, interestingly, that these smaller features have a different fracture point when they are removed from the SOI wafer. In the enlarged inset of Figure 2d, one also notes that the PDMS surface is also no longer flat. The reason for this is because of the fact that sections of the PDMS are in fact reciprocally transferred to the SOI, being ripped out of the bulk in contacting regions activated by the patterned UVO treatment, regions where the PDMS sagged and touched the wafer surface between the peanuts.

We have successfully fabricated a test device using the peanut-shaped μs-Si based on a transfer using Method I.[3b] Figure 3a illustrates the device geometry used. To construct these devices, an indium tin oxide (ITO)-coated PET sheet was used as the substrate. The ITO served as the gate electrode, and diluted SU-8 5 photoresist (measured capacitance = 5.77 nF cm^{-2}) was employed as a gate dielectric. As illustrated by the current–voltage, *I–V*, curves shown in Figure 3b, these plastic-supported, peanut-shaped μs-Si TFTs show accumulation-mode n-channel transistor behavior. The channel length of the device, as shown in the inset image of Figure 3c, is 100 μm, and the width of the device is 400 μm. The transfer characteristics, measured at a constant source–drain voltage (V_{sd} = 1 V) (Fig. 3c), indicated that the threshold voltage (V_{th}) is –2.5 V with an effective mobility of 173 cm^2 V^{-1} s^{-1}. These values are consistent with the performance characteristics expected for a 100 nm thick bottom-gate structure of this type.[3a]

The selective-transfer methods described in this communication constitute an efficient route for transferring microstructured silicon from a SOI wafer to a flexible, macroelectronic system. Using these techniques, and in contrast with conventional solution-casting methods, the microstructured silicon objects can be transferred from an SOI mother wafer with precise registration and utilized in ways that minimize waste. The mechanical properties of the new 3600 PDMS investigated in this work demonstrates that it has a number of important advantages as compared with the commercial Sylgard 184 PDMS resin, notably its dimensional stability and higher surface-adhesion properties. The printing techniques also proved to be compatible with the construction of macroelectronic systems that incorporate high-performance μs-Si thin-film transistors. We are currently exploring strategies for applying these methods to other semiconductor micro- and nanoelements such as InP, GaAs, and GaN.[13–15]

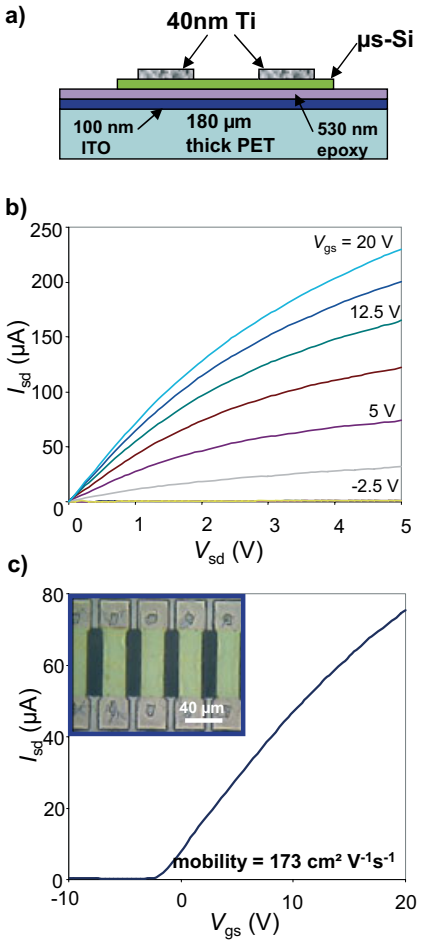

Figure 3. High-performance device formed from the peanut-shaped μs-Si on a plastic substrate using the Method I transfer technique. a) Schematic illustration of device geometry. b) *I–V* curves of μs-Si TFTs at a range of gate voltages (V_{gs} from –2.5 V to 20 V). Device shows an n-channel accumulation-mode behavior. The channel length of the device is 100 μm, and the width of the device is 400 μm. c) The transfer characteristics, measured at a constant source–drain voltage (V_{sd} = 1 V), indicated the effective mobility was 173 cm^2 V^{-1} s^{-1}. The inset shows an optical micrograph of the actual device.

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Experimental

Method I: The fabrication of the μs-Si objects was carried out using a commercial SOI wafer (SOITEC, p-type, top Si thickness = 100 nm, resistivity = 13.5–22.5 Ω cm, 145 nm buried oxide layer). Photolithography (Shipley 1805 resist) was used to pattern the SOI wafer into the desired peanut-shaped geometry (midsection length: 200 μm, width: 25 μm, diameter of peanut: 50 μm). Dry etching (Plasmatherm reactive ion etching [RIE] system, SF6 flow, 40 sccm, 50 mtorr [6.65 Pa], RF power = 100 W, 45 s) was then used to remove the exposed silicon. The underlying SiO_2 was then etched for 80 s in an HF (49 %) solution. For the 3600 PDMS stamp of Method I, a specialty PDMS (Dow Corning, 3600, elastic modulus = 8 MPa) and Sylgard 184 (Dow Corning, elastic modulus = 1.8 MPa) were mixed in a 1:1 ratio and cured using standard soft-lithographic patterning methods [17]. A UV source (ozone active mercury lamp, 173 μW cm^{-2}) was used to cure the PU thin-film adhesion layer (Norland Optical Adhesive, No. 73). These latter films were coated onto a PET substrate (180 μm in thickness, Mylar film, Southwall Technologies) using a bar-coating procedure (Meyer bar, RD Specialties) [19]. This protocol was essential to obtain uniform thin-film coatings of the PU prepolymer over large substrate areas.

Method II: For Method II, the sizes of the peanut shapes used were smaller than the ones used in Method I (midsection length: 10 μm, width: 2 μm, diameter of ends: 5 μm). A similar fabrication protocol was used to produce these structures with the exception that the RIE etching time was reduced to 25 s (to minimize sidewall etching) and the buried oxide layer was etched for 30 s in a concentrated (49 %) HF solution. After the latter etching step, the sample was rinsed in a water bath and dried in an oven at 70 °C for 5 min. A 50 Å SiO_2 layer was then evaporated on top of the sample (Temescal FC-1800 electron-beam evaporator). To bind a thin layer of PDMS onto the PET substrate, a layer of PU was first cast by spinning onto the PET at 1000 rpm for 30 s, which was then exposed to UVO (173 μW cm^{-2}) for 4 min. A film of PDMS was then spin-cast at 1000 rpm for 30 s onto the PU and cured thermally at 65 °C for 3 h.

The selective-area soft-lithographic patterning procedure, following literature procedures [16], consisted of placing the unpatterned PDMS side of the coated PET substrate in contact with the patterned side of the UVO photomask. The fabrication of this microreactor mask followed procedures described by Childs et al. [16]. The pattern consisted of two interlocking rectangular arrays (1.2 mm × 0.6 mm). The PDMS was then irradiated through the UVO photomask for 3 min at a distance of ~3 cm from a mercury bulb (UVOCS model T10 × 10/OES). After exposure, the PDMS stamp was peeled away from the UVO photomask, and the exposed PDMS face was placed into contact with the peanut-bearing SOI wafer. After heating at 70 °C for 30 min, tweezers were used to slowly peel the PDMS away, removing segments of the μs-Si in registry with the areas of irradiation.

Device Fabrication: SU-8 5 with 66 vol.-% SU-8 2000 thinner was spun onto the ITO side of a coated PET sample at 3000 rpm for 30 s. The SU-8 epoxy was then pre-cured at 60 °C on a hot plate for ~1 min. The PDMS stamp (Method I) with the μs-Si on its surface was then brought into contact with the epoxy layer for 30 s and peeled back to transfer the μs-Si to the epoxy. The SU-8 dielectric was then fully cured at 115 °C for 2 min, exposed to UV for 10 s, and post-baked at 115 °C for 2 min. Metal for titanium contacts (40 nm) was then added by e-beam evaporation, with the source–drain area patterned using standard photolithographic methods in conjunction with etching using a 1 % HF solution.

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Photogeneration of Fluorescent Silver Nanoclusters in Polymer Microgels**

By *Jiguang Zhang*, *Shengqing Xu*, and *Eugenia Kumacheva**

Intense interest in inorganic nanoparticles arises from their size- and shape-dependent optical, magnetic, or electronic properties.[1] In particular, nanoparticles of noble metals have been known for a long time for their optical, electronic, and catalytic properties.[2] Recently, Dickson and co-workers[3] re-

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