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Additive Soft-Lithographic Patterning of Submicrometer- and Nanometer-Scale Large-Area Resists on Electronic Materials

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ABSTRACT

We describe a novel soft-lithographic technique possessing broad utility for the fabrication of large area, nanoscale (~100 nm) multilayer resist structures on electronic material substrates. This additive patterning method transfers ultrathin poly(dimethylsiloxane) (PDMS) decals to an underlying SiO_2-capped organic planarazation layer. The PDMS patterns serve as a latent image through which high-quality multilayer resist structures can be developed using reactive ion-beam etching.

Introduction

Photolithography constitutes what is perhaps the most advanced process technology practiced commercially in the world today,[1] directly enabling more than $200 billion in world trade driven by the integrated circuit industry.[2] The capabilities of this technology are without peer. Recent advances in photolithography, for example, now permit the high-volume commercial manufacture of dynamic random access memories and microprocessor units with 90 nm resolution on the feature sizes they embed.[3] Perhaps more striking is the fact that these same devices integrate more than 300 million transistors and 900 m of electrical interconnections per square centimeter, a density of design that speaks directly to the low defect rates achievable with this process technology.[3,4] Further advances in this technology will ultimately allow smaller feature sizes based on reductions in the wavelength of the light source used[5] and development of new optical elements—most notably immersion optics for subnanometer design rules.[6] There remain, however, substantial challenges that must be overcome in this regard, and it is likely that their solution will add to the already exponentially increasing costs associated with the construction of new semiconductor fabrication facilities.[7] This has motivated significant efforts in research to develop alternative nanopatterning techniques, ones that could come to replace projection mode and related electron-beam and X-ray lithographies. For this reason, nanoimprint[8] and soft lithographies[9,10] have attracted considerable interest in research. Nanoimprint lithography (NIL), for example, appears to be a very interesting prospect technology that could come to supplement or replace photolithography because of its potential for both low cost and high-throughput capability.[8] Soft lithography also offers the potential for enabling high spatial resolution patterning[11] and, because of the compliant nature of the elastomeric patterning tools used, complements conventional NIL in being able to generate patterns on curved or contoured substrates as well.[12]

The spatial resolution of soft lithographic patterning processes depends very sensitively on the method of implementation. Microcontact printing, for example, has demonstrated capabilities for high-fidelity patterning for feature sizes that extend well beyond the sub-tenth-micrometer range (e.g., 35 nm).[13] It can also replicate (via molding) extremely small features (30 nm).[14] The resolution of embossing-based protocols (such as MIMIC[15]) is generally

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less than that of nanoscale imprint lithographies using hard masters[8] and somewhat more difficult to apply to complex feature designs[12] and large area substrates.[17] In part to address these latter limitations and to enable useful new approaches to large area patterning, we have developed a new form of soft lithography called decal transfer lithography (DTL).[18] The present work describes a new advance in one form of DTL patterning that appears to hold exceptional promise as a means for transferring submicrometer feature sizes, ones appropriate for use as resists in electronics fabrication processes, over large substrate areas. This method uses cohesive mechanical failure (CMF) patterning, a class of DTL that exploits the transfer of poly(dimethylsiloxane) (PDMS) patterns to a substrate via a sequence of interfacial adhesion and mechanical decohesion of PDMS from a molded elastomeric patterning tool. The conventional CMF process is most useful for delivering micrometer-sized PDMS patterns and has been shown to deliver microstructures that can serve as etch masks for reactive ion etching (RIE) or wet etching processes.[18,19] Submicrometer-sized patterns, however, are more difficult to transfer by CMF, and their utility as resists remains limited because of the very thin nature (10−70 nm) of the PDMS patterns transferred. This limitation is one directly related to the low moduli of the conventional PDMS polymers used in soft-lithographic patterning.[20]

In the present study, we report a new combination of CMF and RIE techniques that broadly circumvent the limitation noted above. The new method enables an extremely facile patterning of submicrometer, high-aspect-ratio resist structures on silicon (and presumably other) substrates with feature sizes (one's limited by the mastering protocols used in this work) reaching to 0.1 μm. The procedures used are illustrated schematically in Figure 1. The process follows reported methods of CMF pattern transfer, with several explicit modifications.[18] Briefly recounting the process here, a PDMS prepolymer (Dow Corning, Sylgard 184) is cast onto a master bearing a relief pattern (i.e., patterned photoresist) and cured at 65 °C. The cured PDMS stamp is peeled from the master, the patterned PDMS surface is exposed to an unfiltered UV/ozone (UVO) environment for 150 s,[18] and the treated surface is immediately placed in conformal contact with an appropriately modified substrate. Given that CMF-based DTL transfers yield extremely thin PDMS resists when very small features are being patterned (i.e., the decohesive debonding of the PDMS occurs near the interfaces of the bonded decal, Figure 1), we modified the substrate by adding additional layers of thin film materials that would serve to increase the aspect ratio of the resists once developed using an RIE protocol. Toward this end, we used substrates that had first been coated with an organic planarization layer (PL) and subsequently overcoated with a thin layer of SiO_2 deposited using an electron beam protocol. A low-pressure mercury lamp (BHK, 173 μW/cm^2) was used for UVO treatment of the PDMS, and after curing at 65 °C, the PDMS pattern was transferred by mechanically peeling away the bulk PDMS. In the present study, a 400 nm thick PL layer (Microposit, Shipley 1805) was spin-cast

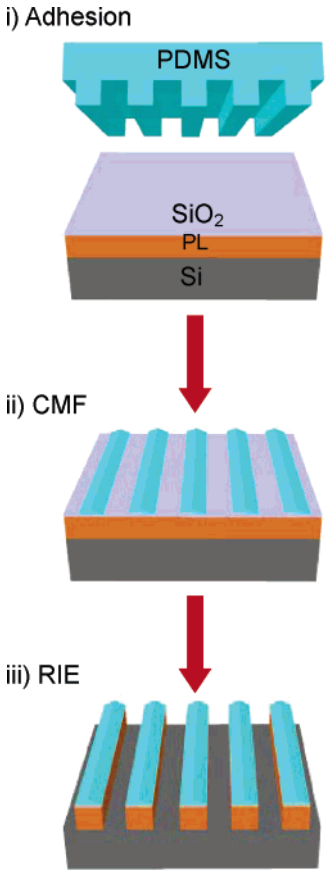

Figure 1. Schematic illustration of the procedure for preparing high-aspect-ratio resist structures on a silicon substrate using a combination of CMF and RIE.

onto a Si(100) substrate (this feature height is easily manipulated by changing the spinning rate used to deposit the PR) and treated with an oxygen plasma to increase adhesion in conjunction with a 3 nm thick SiO_2 film as an adhesion layer and secondary etch stop.

Figure 2a shows a cross-sectional scanning electron microscopy (SEM) image of the interface formed between the PDMS replica and the substrate before peeling off the bulk PDMS layer. Parts b and c of Figure 2 show an atomic force microscopy (AFM) image and cross section of the PDMS lines obtained after peeling the PDMS replica from the substrate (corresponding to Figure 1-ii in the schematic representation of the process). The AFM cross section (Figure 2c) reveals that the transferred PDMS lines are in fact sharply tapered and the average height at the center is about 18 nm. The data reveal that the PDMS lines are ∼370 nm wide and the gap between them is ∼230 nm. Figure 2d shows a top view SEM image of the same sample after dry etching of the SiO_2 for 33 s and anisotropic etching of the PL. Debris from the etching procedure (which can be removed, see below) is seen near the line edges. The RIE resist development procedure (Uniaxis 790) is a two-step process. First, the SiO_2 film is removed using conditions of 50 mTorr of total gas pressure, 40 sccm flow rate of CF_4, and 30 W of rf power. Anisotropic etching of the PL is then carried out using 20 mTorr of total gas pressure, an O_2 flow rate of 10 sccm, and 100 W of rf power for 5 min. The average width and

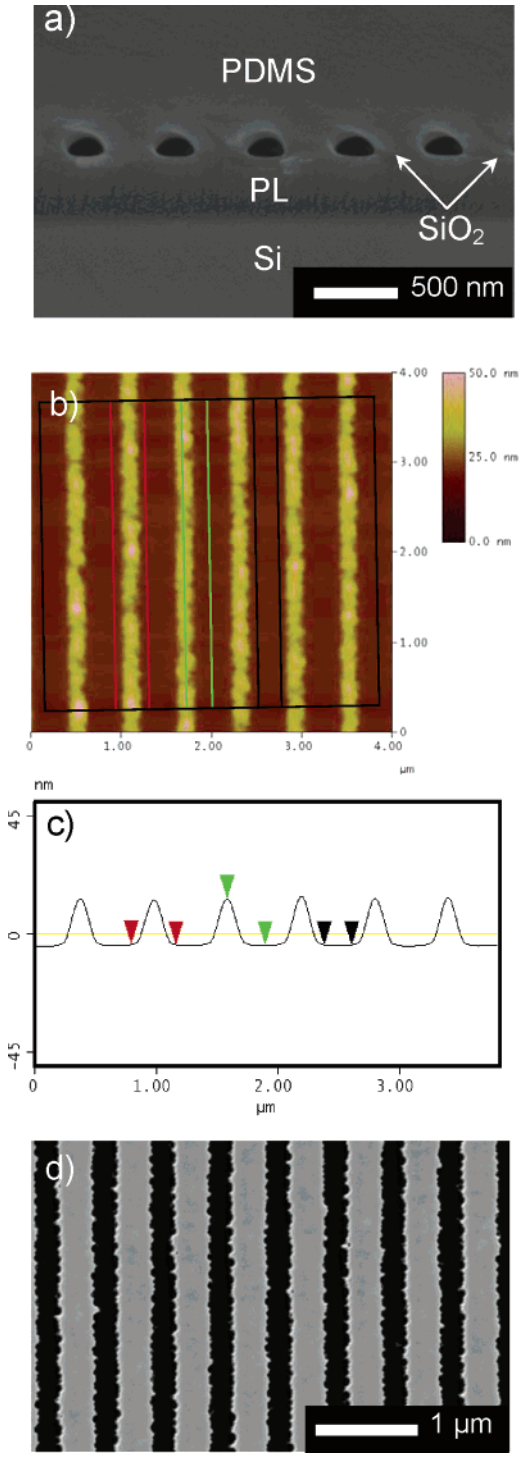

Figure 2. (a) Cross-sectional SEM images of the interfaces between a PDMS replica and the substrate before peeling off the PDMS. An AFM image (b) and AFM cross section (c) of the PDMS lines on an SiO_2/PL/Si(100) substrate before SiO_2 etching that corresponds to Figure 1-ii.. (d) Top-view SEM image of the resulting PDMS/SiO_2/PL resist structures on Si(100) substrates that corresponds to Figure 1-iii. SiO_2 layers have been etched using CF_4 plasma for 33 s.

gap of the lines obtained are 360 and 240 nm, respectively. Comparing the data in parts b and c of Figure 2 suggests that the width of the lines slightly decreases due to the nature of the etching process used. We believe the RIE process can be optimized to improve the anisotropy of the etching steps.[21]

One attractive aspect of this procedure, however, is that it also allows us to explore feature sizes that exceed those of the original master (as the CF_4 plasma used for dry etching the SiO_2 layer removes not only that material but also PDMS as well).

Figure 3 shows cross-sectional SEM images of PDMS/SiO_2/PL resist structures on Si(100) substrates that result at several stages of development. The structures shown were derived from an SiO_2 etching step carried out by RIE for various times and followed by anisotropic etching of the PL for 5 min. As shown in the figures, the width of the patterned lines decreases as the duration of the dry etching of the SiO_2 increases. The average widths of the lines seen in parts a−d of Figure 3 are 250, 180, 130, and 100 nm, respectively. These figures demonstrate that the PDMS/SiO_2 layers can successfully serve as an etch mask for anisotropic O_2 RIE of a PL and that the width of the lines can be varied in a controlled way down to at least 100 nm (and likely beyond).

The patterning demonstrated above provides an additional and somewhat interesting point for making comparisons with imprint lithographies. Conventional imprinting techniques using solid/glassy polymers, which are performed at high temperature (i.e., above the glass transition temperature of the resist polymer), cannot be used to imprint multiple patterns on the substrate because the previously imprinted patterns may be degraded by heating.[8] There are only a few reports available related to room-temperature imprinting in which multipattern imprinting was enabled but the generality of the approach appears to be limited, at best.[21] Imprint lithographies using liquid prepolymers also appear to be restricted to single printing levels (patterned features would hinder the run out of residual prepolymer). The methodology described in the present study has different pattern transfer mechanics, ones that lend themselves well to multistep patterning. To demonstrate this, we carried out model transfers of PDMS lines of varying design rules directly on top of a previously transferred CMF decal, followed by development of the PL resist pattern by RIE. These process steps are illustrated schematically in the Supporting Information. The procedures used are identical to those described above for a single printing level. In the examples shown in Figure 4, two CMF decals comprised of straight lines were aligned optically and printed in sequence along perpendicular directions on the SiO_2/PL layer and subsequently developed by RIE. Figure 4 shows SEM images of the model resists obtained after etching. Masters with line patterns having widths of 300 nm were used to generate the structures shown in Figure 4a. An overlayer of 300 nm and 2 μm CMF decals (pitch of 2 in each case) was used to generate the complex grating architecture shown in Figure 4b. The design rules enabled in this way, and the fact that areas exceeding 2 cm^2 can be patterned with facility, suggest the method holds promise for several areas of application including optics and microelectronics. Finally, we note that the utility of resists (Shipley 1805) of the type shown in Figures 3 and 4 to serve as effective latent images in subsequent fabrication processes (e.g. plasma and wet etching, lift-off, etc.) has been documented fully in the literature for feature sizes near the

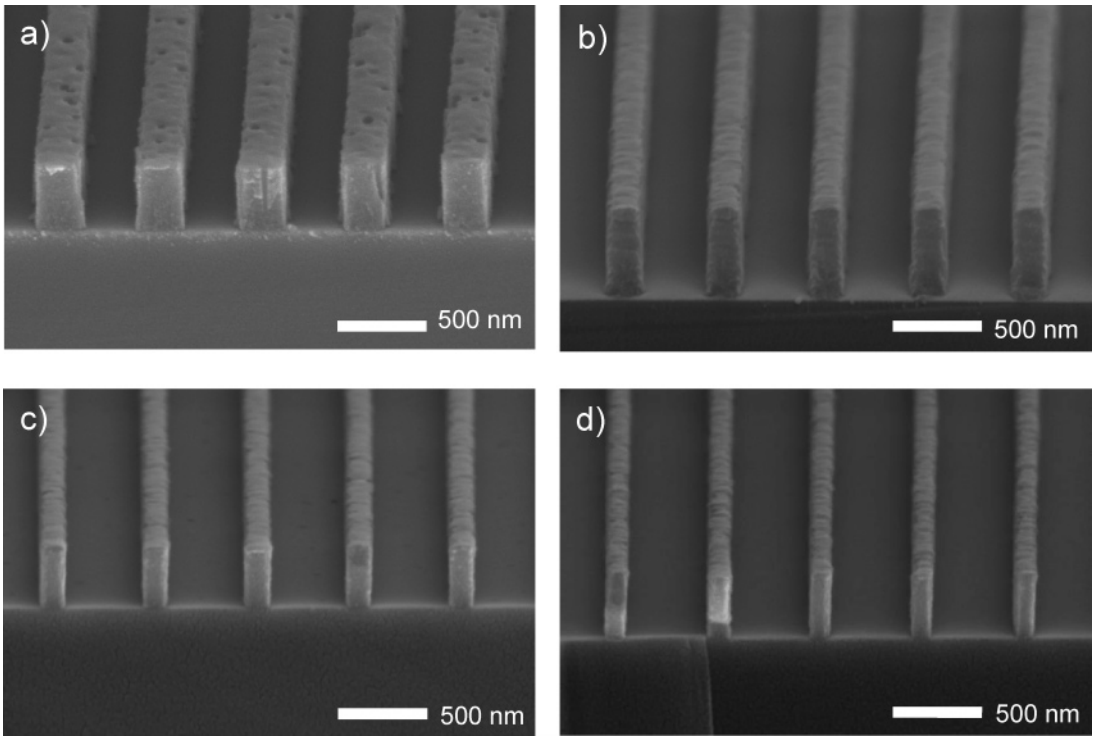

Figure 3. Cross-sectional SEM images of the resulting PDMS/SiO_2/PL resist structures on Si(100) substrates after RIE of SiO_2 for (a) 35 s, (b) 40 s, (c) 45 s, and (d) 50 s and anisotropic etching of PL for 5 min.

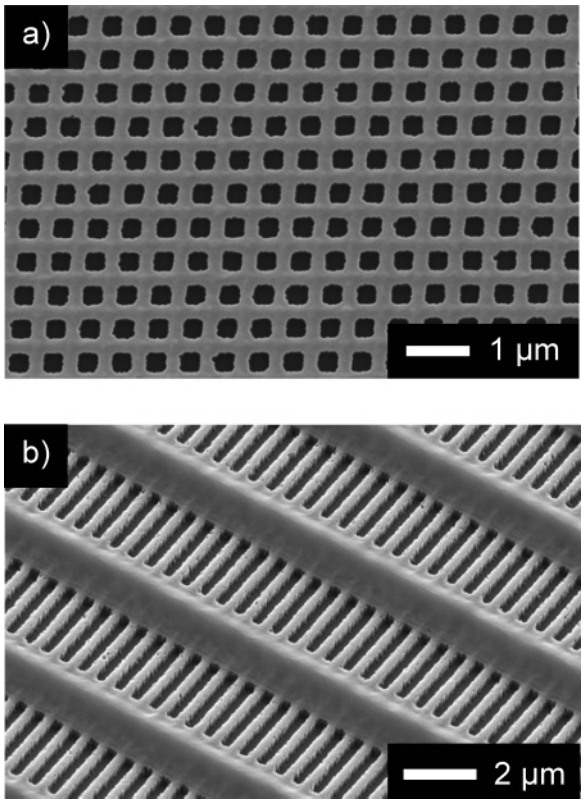

Figure 4. Top-view (a) and tilted-view (b) SEM images of the multiply transferred PDMS lines after RIE of SiO_2 and PL layers. 300 nm (a) and 2 μm (b) wide line patterns have been used for the second set of PDMS lines.

~100 nm benchmarks established in the present work.[23] This provides, then, a strong foundation upon which to develop extensions of this process that might eventually displace more conventional procedures based on photolithography.

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Supporting Information Available: Illustration of steps for preparing perpendicularly superimposed PDMS lines on an SiO_2/PL/Si(100) substrate using the CMF patterning technique. This material is available free of charge via the Internet at http://pubs.acs.org.

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