Printed thin-film transistors and complementary logic gates that use polymer-coated single-walled carbon nanotube networks

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This paper reports on the electrical properties of thin-film transistors (TFTs) that use polymer-coated networks of single-walled carbon nanotubes (SWNTs) as the semiconductor with source and drain electrodes formed by high-resolution printing techniques. *P*-channel, *n*-channel, and ambipolar TFTs are demonstrated with bare SWNT networks, networks coated with polyethylene imine and with polyethylene oxide, respectively. Studies of the scaling of properties with channel length and tube density reveal important information about the operation of these devices. Complementary inverters made with *n*- and *p*-channel devices show gain larger than one and illustrate the potential use of these types of TFTs for complex logic circuits. © *2005 American Institute of Physics*.
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I. INTRODUCTION

Semiconductor materials that can be deposited, preferably by printing, as thin films onto plastic substrates are of interest as enabling technologies for emerging types of large area, printed flexible electronic systems, known as "macroelectronics." Organic small molecules and polymers, organic-inorganic hybrids, inorganic micro-/nanomaterial building blocks, and single-walled carbon nanotubes (SWNTs) have all been explored for this purpose. Of these materials, networks[1–3] and arrays[4–6] of SWNTs are particularly interesting because the very high mobilities of the individual tubes suggest that networks or arrays of them could provide exceptionally high effective thin-film mobilities. Furthermore, single-tube transistor studies show that the operation of the devices can be controlled, from *p* channel to *n* channel to ambipolar, simply by the use of insulating coatings of polymers that have different interactions with the tubes.[7] This flexibility provides, in a single class of material, the ability to achieve complementary logic and even devices such as *p*-*n* diodes and more complex systems. This paper demonstrates some of these capabilities in network-based SWNT thin-film transistors (TFTs) that use source and drain electrodes formed by high resolution using printing-based approaches. The results are important for potential applications of this class of material in macroelectronics, sensor systems, and other devices.

The paper begins with a description of the fabrication steps, which incorporate a patterning method known as

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nanotransfer printing (nTP),[8–11] for nanotube TFTs that exhibit *p*-channel, *n*-channel, and ambipolar behaviors when operated without any polymer coatings, with coatings of polyethylene imine (PEI) and polyethylene oxide (PEO), respectively. The scaling of the electrical properties of these devices with channel length and number of tubes per unit area reveal important aspects of the nature of charge transport through them. By combining *p*-channel and *n*-channel devices on a single substrate, it is possible to build complementary logic elements. A working inverter with gain larger than one demonstrates this capability.

II. EXPERIMENT

Figure 1(a) schematically illustrates the steps for building SWNT TFTs with printed electrodes. Random submonolayer networks of SWNTs (diameters between 1 and 3 nm, and lengths between 5 and 10 μm) were first grown onto SiO_2(100 nm)/Si wafers using established chemical-vapor deposition (CVD) techniques.[12] By controlling the growth conditions, we could select from low-density networks (1 tube/μm^2) that slightly exceed the percolation threshold (0.1–0.3 tube/μm^2) to high-density networks (30 tubes/μm^2). The general procedure involved diluting ferritin catalyst (Sigma-Aldrich Co.) in de-ionized water and then spin casting it onto degenerately doped Si substrates with a 100-nm-thick layer of thermal silicon dioxide. Heating these wafers to 900 °C oxidized the catalyst. Cooling them to room temperature in an air environment and then heating them to 900 °C in hydrogen reduced the catalyst. Growth was performed at 900 °C with CH_4[500 SCCM (standard cubic centimeter per minute)] and H_2(75 SCCM). The dilution ratio of the catalyst and the growth times defined the density of the networks. Reactive ion etching of the SWNTs through photolithographically defined patterns of resist created network stripes oriented along the transistor channels. These stripes facilitate electrical burnout procedures that enable high on/off current ratios in short channel devices; they also prevent electrical crosstalk between devices.[3] To create the stripes, Shipley 1805 photoresist was spin coated at 3000 rpm on the SWNT substrates, prebaked at 115 °C for 1 min, exposed to UV light for 6 s (~120 mJ/cm^2) with a photomask that had 5 μm line and spacing patterns, and developed for ~6 s in MF-319 developer. After rinsing with de-ionized (DI) water and drying with nitrogen, these substrates were placed in a reactive ion etching (RIE) chamber (Plasma Therm 760) to etch the exposed SWNTs with O_2 plasma. The etching was done in a 20 SCCM O_2 flow at a pressure of 200 mtorr for 30 s with 100 W radio-frequency power. The remaining photoresist was removed by acetone after the RIE treatment.

The SiO_2 and Si provided the gate dielectric and gate, respectively. Source and drain electrodes were formed directly on the SWNTs using the nTP technique. This procedure uses elastomeric stamps formed by casting and curing of polydimethyl siloxane (PDMS) against masters consisting of patterns of photoresist on silicon wafers. To fabricate masters for stamps that had 6 and 12 μm channel lengths, SU-8 5 photoresist was spin coated at 3000 rpm, prebaked at 120 °C for 5 min, exposed to UV light for 8 s (~160 mJ/cm^2), postbaked at 95 °C for 3 min, and then developed for ~30 s in SU-8 developer. SU-8 50 photoresist was spin coated at 4000 rpm, prebaked at 65 °C for 5 min and 95 °C for 15 min, exposed to UV light for 40 s (~800 mJ/cm^2), postbaked at 65 °C for 1 min and 95 °C for 4 min, and then developed for ~4 min in SU-8 developer to generate masters for the stamps that had 55 and 110 μm channel lengths. PDMS (Sylgard 184 from Dow Corning) prepolymer was mixed with curing agent and degassed, poured over the masters, and cured in the oven at 80 °C for 2 h. Peeling the cured PDMS from the masters completed the stamp fabrica-

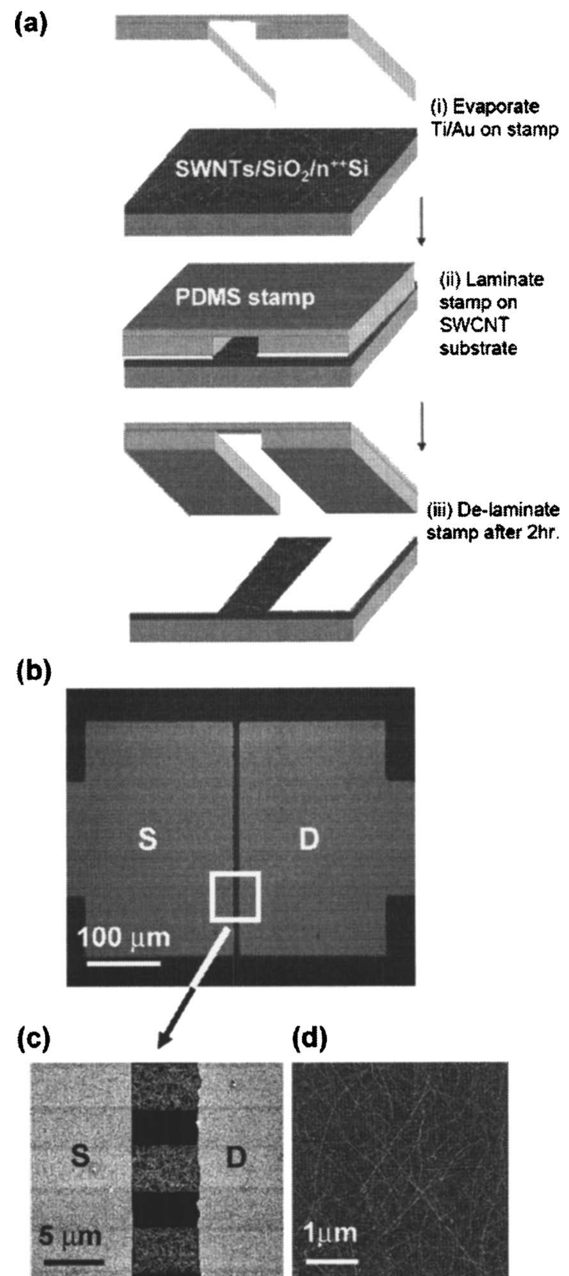

FIG. 1. (a) Schematic illustration of steps for building SWNT TFTs with nanotransfer printed electrodes. Contacting a metal-coated stamp to a SWNT/SiO_2/Si substrate followed by moderate heating causes the metal to remain on the substrate after removing the stamp. (b) Optical image of the printed electrodes, (c) SEM image of the printed electrodes and the striped SWNT networks, and (d) AFM image of the SWNTs in the channel.

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tion. Coating the stamps with a collimated flux of metal [Au (20 nm;0.5 nm/s) and then Ti (2 nm;0.1 nm/s) with a Temescal *e*-beam evaporator (BJD 1800)] generated discontinuous films on the raised and recessed regions. Placing such a metal-coated stamp onto a substrate leads to "wetting" that provides intimate contact between the two surfaces without the need to apply external pressure.[13,14] Contact for sufficient time at room temperature or slightly elevated temperatures, followed by the removal of the stamp, leaves a metal pattern in the geometry of the relief features on the substrate. The transfer process can be guided either through specific chemical interactions between the metals and the substrates[9–11] or, by general, noncovalent surface forces.[8] In the devices described here, we printed Ti(2 nm)/Au(20 nm) by placing the metal-coated stamps on the SWNT/SiO_2/Si substrates, baking at 70 °C for 1 h, and then removing the stamps. The geometries of relief define the dimensions of the electrodes: electrodes with separations as small as 150 nm have been demonstrated[15] and a few tens of nanometers are achievable.[9,11] Here we investigated devices with electrode separations (i.e., channel lengths) between approximately 5 and 100 μm.

Figures 1(b) and 1(c) show images of a representative pair of printed Ti (2 nm)/Au(20 nm) electrodes on a SWNT/SiO_2/Si substrate. Figure 1(d) shows an atomic force microscope (AFM) image of the SWNTs in this channel. The density of the tubes in this network is ~30 tubes/μm^2, as estimated from analysis of the AFM image.

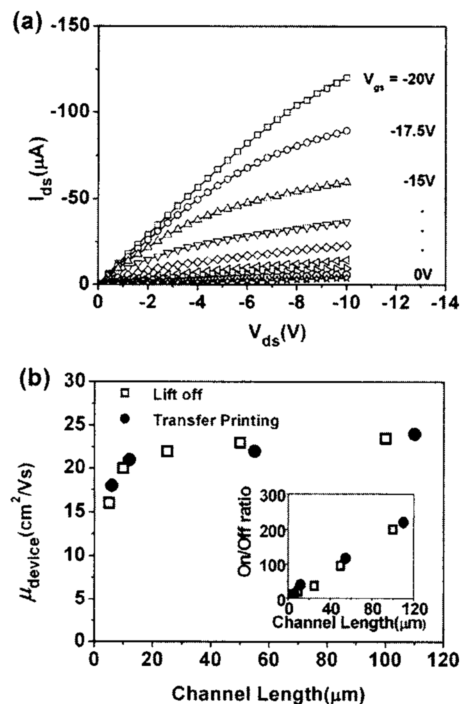

FIG. 2. (a) Drain-source current (I_{ds}) vs drain-source voltage (V_{ds}) for a printed SWNT TFT with 250 μm channel width and 100 μm channel length (gate voltage V_{gs}: −20 to 0 V from the top, 2.5 V step). (b) Comparison of the device mobilities ($\mu_{devices}$) of SWNT TFTs formed by conventional photolithography (solid circles) and by nanotransfer printing (open squares) as a function of channel length, with a fixed channel width of 250 μm. The inset shows on/off current ratios.

III. RESULTS

SWNT TFTs formed with these procedures have properties that compare well to those of devices whose electrodes are defined by conventional photolithography and lift-off. Figure 2(a) shows typical current-voltage characteristics of a printed device. These TFTs operate in the unipolar *p*-channel mode. To calculate the linear regime device mobility (μ_{device}), we evaluated the slope in the transfer characteristics and applied the standard formula, $\mu_{device}=(dI_{ds}/dV_{gs})/(\varepsilon\varepsilon_0 V_{ds} W/Lt)$, where I_{ds} the drain-source current, V_{gs} the gate voltage, V_{ds} the drain-source voltage, t the thickness of SiO_2 (100 nm), L the channel length, ε the dielectric constant of SiO_2 (3.9) and ε_0 is the permittivity of free space, and W the channel width. Effects of fringing fields on the capacitance, which can be important at low network densities, were not considered. We used the physical width W of the channel for these computations. (Mobilities computed using the summed widths of the stripes, rather than the physical widths of the electrodes, yield values that are approximately twice as large as those presented here. This higher value represents mobilities that are achievable in lithographically optimized striping geometries.) As shown in Fig. 2(b), the printed devices show mobilities and on/off current ratios similar to those of devices defined by photolithography for the entire range of channel lengths (L between 5 and 100 μm) investigated here. The slight decrease in μ_{device} with decreasing channel length observed in both types of devices could be due to resistances at the contacts between the metal electrodes and the SWNTs. Shifts in threshold voltages (V_t) are also observed in these devices, as shown in Fig. 3(a). These shifts as well as the apparent decreases in mobility may be due partly to a transition from transport dominated by network effects at large channel lengths to one strongly influenced by tubes that directly span the channel in short channel devices.[16] Empirical analysis of the device behavior showed effective contact resistances of a few tens of Ω cm, from linear fits of device resistances measured at different V_{gs} as a function of channel length, as shown in Fig. 3(b).[17] Linear fit to these data gives intrinsic device mobilities of ~22 cm^2/V s and intrinsic threshold voltages of ~−4 V.

The on/off current ratio also decreases sharply with L. For L less than $\langle L\rangle$, the average tube length, a substantial number of metallic tubes bridge the channel and give rise to significant off current. The on/off current ratio in this regime approaches a value comparable to that expected based on the 1/3 metallic tube content of these networks. The on/off current ratio increases with L larger than $\langle L\rangle$ due to the decreasing probability of purely metallic network pathways from source to drain electrode. We observed an increase in μ_{device} and a decrease in on/off current ratio with increasing density of the SWNT networks. For example, devices with lower densities (~14 tubes/μm^2) than the ones in Fig. 2 (~20 tubes/μm^2) showed on/off current ratios of ~10^4 at L =100 μm but with μ_{device}~20 cm^2/V s, as shown in Fig. 4. The off currents can be eliminated through selective breakdown of the metallic pathways. In this process, V_{ds} is slowly increased while V_{gs} held at a voltage that strongly turns off

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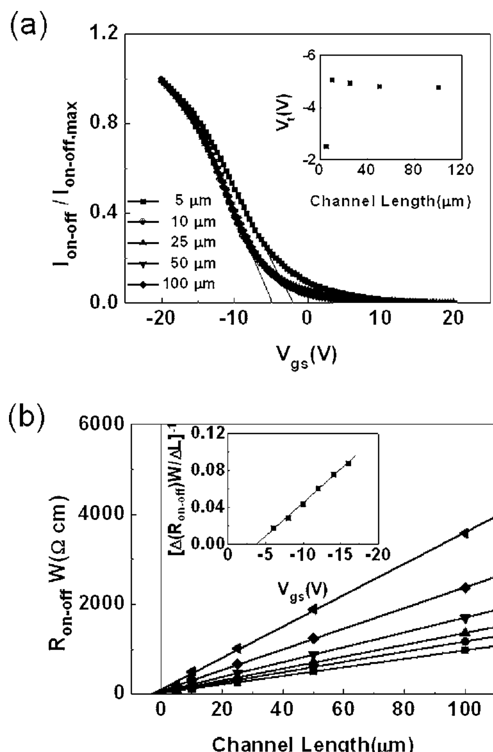

FIG. 3. (a) Normalized transfer curves as the channel length. The inset shows threshold voltage as a function of channel length. (b) Width-normalized resistance of devices in the on state minus that in the off state ($R_{\text{on-off}}W$) as a function of channel length L at the different gate voltages. To remove metallic tube effects, we subtracted off current from on current to calculate resistances. Gate voltages were −8, −10, −12, −14, −16, and −20 V from top to bottom. The solid lines represent the linear fits. The inset shows the sheet conductance $[(\Delta R_{\text{on-off}}W)/\Delta L]^{-1}$, determined from the reciprocal of the slopes of the linear fitting in Fig. 3(b), as a function of gate voltage.

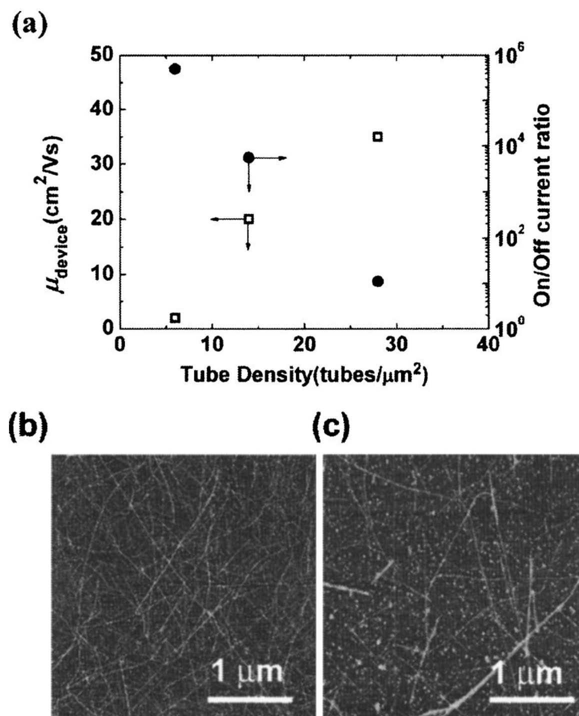

FIG. 4. (a) Device mobilities and on/off ratios as a function of tube density. The channel length and width were 100 and 250 μm, respectively. AFM image of SWNTs grown from (b) 20× diluted ferritin catalyst for 1 h, and (c) 40× diluted ferritin catalyst for 10 min.

the semiconducting tubes. At sufficiently high V_{ds}, I_{ds} irreversibly decreases to small values due to electrical breakdown of the metallic tubes.[3] A modest decrease in the mobility can accompany this electrical breakdown process. Chemical procedures are also available to increase the on/off ratio.[18,19]

As operated in open air, all of the SWNT TFTs showed unipolar p-channel operation, whether their electrodes were formed by printing or by photolithography. Obtaining both p- and n-channel devices is crucial to achieving efficient operation of complex logic circuits. Work on individual SWNT transistors shows that they also exhibit p-channel behavior in ambient conditions but that they can switch to n channel when they are annealed in vacuum.[20] We observed similar behavior in our network SWNT devices, as shown in Fig. 5. For realistic device applications, a more convenient means to control the device operation is required. Using ideas borrowed from work on single-tube transistors,[7] we previously showed that SWNT TFTs built by photolithography exhibit n-channel operation when coated with PEI.[3] This approach works equally well with the printed devices described here. Figures 6(a) and 6(b) show the transfer characteristics of devices before and after their conversion to n-channel operation by coating the entire active areas of the devices with a low molecular weight PEI (~800, Sigma-Aldrich Co.). The inset of Fig. 6(b) shows the output characteristics of a PEI-coated device whose channel length and width are 100 and 250 μm, respectively. As an extension of this approach, we demonstrated that PEO enables ambipolar operation in printed SWNT TFTs just as it does in single-tube devices.[21] Figure 6(c) shows the conversion. Figure 6(d) indicates that the channel length scaling properties of the n-channel devices are similar to those of the p-channel devices. The mobilities in the n-channel devices are, however, systematically lower compared to the original p-channel devices. This difference could be attributed to incomplete coating/interaction of the PEI with the tubes, the presence of O_2 adsorbed onto the devices prior to coating, or to an intrinsic difference in mobility for electrons and holes through the network. We observed a change from n-channel to ambi-

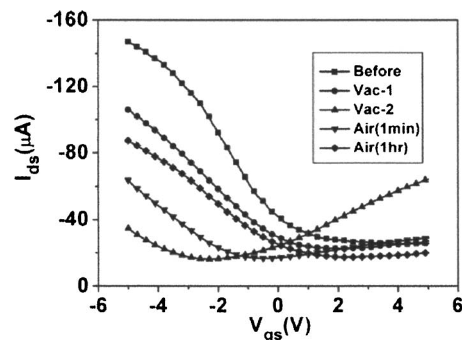

FIG. 5. Changes from p-channel to ambipolar behavior of network SWNT TFTs as a function of exposure to air. Vac-1: 1 day annealing at 10^{-5} torr at room temperature. Vac-2: 1 day annealing at 10^{-5} torr at 150 °C. Channel length and channel width were 5 and 250 μm, respectively, and V_{ds} was −0.5 V.

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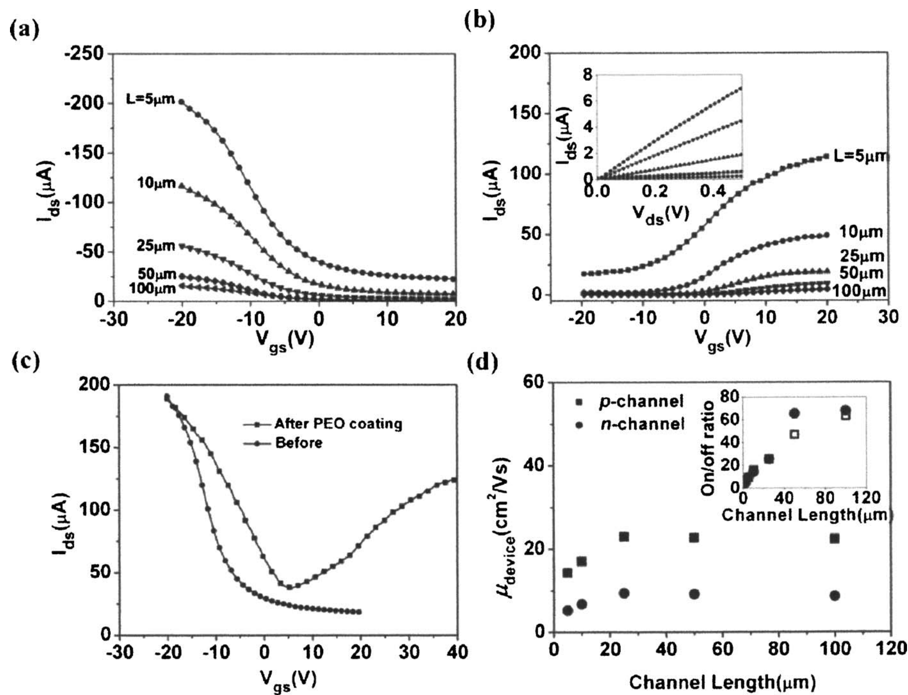

FIG. 6. (a) Transfer curves of a series of printed SWNT TFTs (V_{ds} was fixed to −0.5 V). (b) Transfer curves of a series of printed SWNT TFTs after uniformly coating with PEI (V_{ds} was fixed to −0.5 V). The inset shows the output curves for the device with 100 μm channel length (gate voltage V_{gs}: 20–0 V from the top, 5 V step). (c) Transfer curves of a SWNT TFT before (p channel, open diamonds) and after (ambipolar, open squares) applying a uniform PEO coating to a device with 5 μm channel length (V_{ds} was fixed to 0.5 V). (d) Device mobilities (μ_{device}) before (p channel, open squares) and after (n channel, solid circles) applying a uniform PEI coating, for various channel lengths. The inset shows on/off current ratios. In all cases [(a)–(d)], the channel widths were 250 μm.

polar operation of PEI-coated devices after washing away (to the extent possible) the PEI with methanol. Recoating the devices returned them to unipolar n-channel behavior, as shown in Fig. 7.

Studies of SWNT TFTs constructed with PEI coatings selectively confined to the central part of the channel and those with PEI only in the contact regions suggest that uniform PEI coatings can change not only the contact properties but also the electrical properties of the tubes themselves. The results of this type of experiment, the analog of which has not been carried out in single-tube devices, are consistent with previous connections drawn between the electron donating ability of the polymer[7] and changes in single-tube device properties. Changes in tube properties are also confirmed by optical measurements.[21] The same charge transfer and doping effects that control the behavior of polymer-coated single-tube transistors[7,21] likely govern the network-based TFTs described here. The ability to control the channel with insulating polymer coatings provides an important advantage of SWNT TFT devices compared, for example, to conventional organic semiconductors where different chemistries are typically required to achieve n- and p-channel operations and where n-type materials typically have much lower mobilities than p-type materials. A disadvantage of the PEI coating, however, is that it can degrade near the contacts at high voltages, which restricts the range of operating voltages (V_{ds}) in these devices.

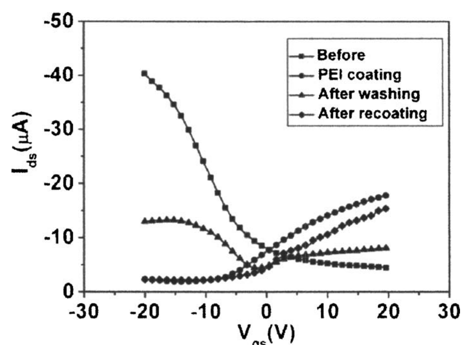

FIG. 7. Changes from p-channel to ambipolar behavior of network SWNT TFTs for different conditions of a PEI coating. Washing was performed by soaking the PEI-coated device for 1 day in methanol at room temperature. Channel length and channel width were 25 and 250 μm, respectively, and V_{ds} was −0.5 V.

We exploited the ability to control the operation of the devices to fabricate SWNT TFT-based complementary logic gates with bare p-channel devices and PEI-coated n-channel devices. Figure 8(a) shows a schematic illustration of the inverter configuration. The inverter in Fig. 8 showed a gain about 1.6, which is similar to inverters made with an individual nanotube by potassium doping[20] and to results that can be achieved with conventional organic semiconductor-based devices.

IV. SUMMARY AND CONCLUSIONS

This paper presents p-channel, n-channel, and ambipolar SWNT TFTs with electrodes defined by a high-resolution printing process. These devices show mobilities of $\sim 25\ cm^2/V\,s$ for p-channel devices (corresponding to $\sim 50\ cm^2/V\,s$ when the device width is computed from the summed widths of the striped regions) and ~ 10 (corresponding to $\sim 20\ cm^2/V\,s$ when the device width is computed from the summed widths of the striped regions) for n-channel devices. The ambipolar devices showed lower n-channel mobility than p channel when biased into the p and n modes. Selective polymer coatings and scaling studies with channel length and tube density provide insights into the operation of these devices. Complementary logic gates with these types of devices illustrate their suitability for complex circuits. Although these and other features of SWNT TFTs are attractive, there are disadvantages such as hyster-

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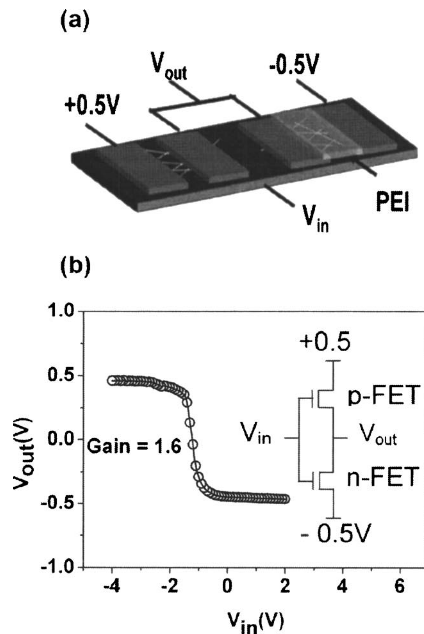

FIG. 8. (a) Schematic illustration of a complementary inverter based on SWNT TFTs. One side of channel was coated with PEI while other one was protected with PDMS. (b) Transfer characteristics of the inverter. The channel length and channel width were 50 and 250 μm for both devices.

esis in the device behavior, which is thought to be due to field concentration around the tubes, and modest on/off current ratios due to the presence of metallic tubes. Current research is identifying methods to circumvent both of these problems. We believe, as a result, that arrays and networks of SWNTs represent promising semiconductor materials for macroelectronics and other systems.

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[1]E. S. Snow, J. P. Novak, P. M. Campbell, and D. Park, Appl. Phys. Lett. **82**, 2145 (2003).
[2]K. Bradley, J. C. P. Gabriel, and G. Gruener, Nano Lett. **3**, 1353 (2003).
[3]Y. Zhou, A. Gaur, S. Hur, C. Kocabas, M. A. Meitl, M. Shim, and J. A. Rogers, Nano Lett. **4**, 2031 (2004).
[4]C. Kocabas, M. Meitl, A. Gaur, M. Shim, and J. A. Rogers, Nano Lett. **4**, 2421 (2004).
[5]R. Seidel, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Steinhoegl, F. Kreupl, and W. Hoenlein, Nano Lett. **4**, 831 (2004).
[6]C. Kocabas, S.-H. Hur, A. Gaur, M. Meitl, M. Shim, and J. A. Rogers, Small **1**, 1110 (2005).
[7]M. Shim, A. Javey, N. W. S. Kam, and H. Dai, J. Am. Chem. Soc. **123**, 11512 (2001).
[8]S. H. Hur, D. Y. Khang, C. Kocabas, and J. A. Rogers, Appl. Phys. Lett. **85**, 5730 (2004).
[9]Y. L. Loo, R. L. Willett, K. W. Baldwi, and J. Rogers, J. Am. Chem. Soc. **124**, 7654 (2002).
[10]J. Zaumseil, M. A. Meitl, J. W. P. Hsu, B. R. Acharya, K. W. Baldwin, Y. L. Loo, and J. A. Rogers, Nano Lett. **3**, 1223 (2003).
[11]E. Menard, L. Bilhaut, J. Zaumseil, and J. A. Rogers, Langmuir **20**, 6871 (2004).
[12]W. Kim, H. C. Choi, M. Shim, Y. Li, D. Wang, and H. Dai, Nano Lett. **2**, 703 (2002).
[13]K. J. Hsia, Y. Huang, E. Menard, J.-U. Park, W. Zhou, J. A. Rogers, and J. M. Fulton, Appl. Phys. Lett. **86**, 154106 (2005).
[14]Y. G. Y. Huang, W. X. Zhou, K. J. Hsia, E. Menard, J. U. Park, J. A. Rogers, and A. G. Alleyne, Langmuir **21**, 8058 (2005).
[15]J. Zaumseil, T. Someya, K. Baldwin, Z. Bao, Y.-L. Loo, and J. A. Rogers, Appl. Phys. Lett. **82**, 793 (2003).
[16]R. V. Seidel, A. P. Graham, B. Rajasekharan, E. Unger, M. Liebau, G. S. Duesberg, F. Kreupl, and W. Hoenlein, J. Appl. Phys. **96**, 6694 (2004).
[17]S. Luana and G. W. Neudeck, J. Appl. Phys. **72**, 766 (1992).
[18]C. J. Wang, Q. Cao, T. Ozel, A. Gaur, J. A. Rogers, and M. Shim, J. Am. Chem. Soc. **127**, 11460 (2005).
[19]L. An, Q. A. Fu, C. G. Lu, and J. Liu, J. Am. Chem. Soc. **126**, 10520 (2004).
[20]V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris, Nano Lett. **1**, 453 (2001).
[21]G. P. Siddons, D. Merchin, J. H. Back, J. K. Jeong, and M. Shim, Nano Lett. **4**, 927 (2004).

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