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Organic Nanodielectrics for Low Voltage Carbon Nanotube Thin Film Transistors and Complementary Logic Gates

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Aligned arrays and random networks of single-walled carbon nanotubes (SWNTs) represent thin film material types that are attractive as conducting/semiconducting elements of flexible electronic circuits.[1] The large carrier mobilities[2] and mechanical, chemical, and electrical robustness[3,4] of individual SWNTs imbue these films with remarkably good properties. However, high-performance thin film transistors (TFTs) using submonolayer SWNT films (arrays or networks) as the semiconductor[5] require high capacitance gate dielectrics to enable low voltage and possibly hysteresis-free operation. For complementary circuits, this dielectric must also be compatible with polymer coatings and other chemistries enabling unipolar n- or p-channel transport in SWNT TFTs.[6,7] Flexible electronic devices require the dielectric to be mechanically bendable; for systems that use plastic substrates, the ability to deposit the dielectric from solution at low temperatures is also important. Developing materials that satisfy all of these requirements is challenging. Thin liquid polymer electrolyte films provide gates and gate dielectrics that have some of these characteristics and were recently used with SWNTs to achieve TFTs with good properties.[8] However, drawbacks of this approach include long response times ($\sim$1$-$10 ms) associated with electrolyte migration and difficulties in integrating thin liquid layers into complex circuits. We report here that nanoscopic 3-D $\sigma-\pi$ self-assembled superlattices (SASs) function as exceptionally good dielectrics for n- and p-channel SWNT TFTs. The excellent performance characteristics of these devices and of complementary logic gates formed with them suggest that dielectrics of this general type offer a promising path to SWNT-based thin film electronics.

Figure 1a illustrates the device layout which includes patterned metal source and drain electrodes, a random SWNT network for the semiconductor, and a SAS multilayer for the dielectric, here on a doped silicon wafer serving as substrate and back gate. The SAS nanodielectric multilayer was deposited via solution methods describe previously.[9] This nanodielectric has a thickness of $\sim$16 nm and a capacitance of 170 $\pm$ 9 nF/cm^2 (10^3-10^6 Hz), as measured by impedance spectroscopy. Transfer printing techniques placed networks of SWNTs grown by chemical vapor deposition (CVD) on SiO_2/Si wafers directly onto the SAS nanodielectric.[4] The CVD growth conditions can be adjusted to achieve a relatively high SWNT coverage ($\sim$30 tubes/μm^2).[7] Figure 1b shows scanning electron micrographs (SEMs) of such SWNT networks transfer printed from CVD growth substrate onto the SAS nanodielectric layer. The tube density per unit area is similar in the two cases, consistent with the high transfer printing process efficiency. The holes visible in the transferred networks represent an artifact of the procedures used here and have near-negligible influence on

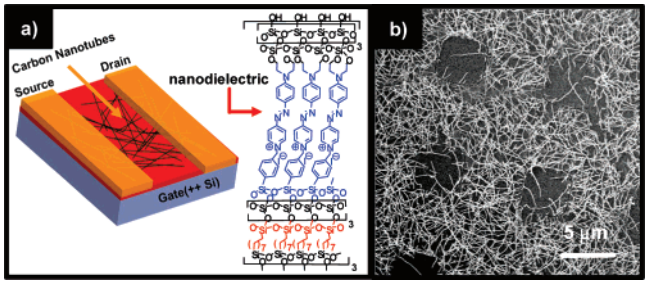

Figure 1. (a) Schematic illustration of a thin film transistor that uses a large number of individual SWNTs as an effective semiconducting "film" and a nanoscale SAS as the gate dielectric. (b) Scanning electron micrographs of single-walled carbon nanotube networks transfer printed from the CVD growth substrate onto the SAS nanodielectric layer (thickness $\sim$16 nm)/Si.

device performance. AFM (Supporting Information) suggests that the transferred SWNTs rest on the top surface of the dielectric and are not substantially pressed into it during transfer. SWNT$-$SAS adhesion, which is likely van der Waals in origin, leads to bonding sufficiently strong to pass "Scotch tape" tests. This good adhesion together with the robustness of the dielectric allows direct photolithographic patterning of source and drain electrodes by liftoff.

Figure 2 shows the current$-$voltage response of typical TFTs having the present design. As fabricated, and in ambient, they exhibit unipolar p-channel operation with moderate, positive threshold voltages and little hysteresis. This latter property is in sharp contrast to the behavior of devices that use a 100 nm SiO_2 layer as the dielectric (Supporting Information). In this case, large hysteresises, corresponding to 10$-$20 V shifts in threshold voltage, are observed in ambient, depending on the direction and range of gate voltage sweeps. This marked hysteresis, also present in single tube devices,[10] declines with decreasing SiO_2 thickness and decreasing gate voltage,[11] but still presents problems for operation of such devices in circuits, even with SiO_2 thicknesses in the 20 nm range (Supporting Information). Some work suggests that the hysteresis arises from charge injection into traps in the dielectric, especially at high gate voltages and when there is adsorbed water near the SWNTs.[10] Reports of high k[12] and ultrathin dielectric layers[13] exist, but few describe hysteresis in detail. Since fixed positive charges, interface state densities, and the surface chemistries of the SAS nanodielectric are similar to those of SiO_2,[9] we speculate that the low hysteresis is derived mainly from the low operating voltages enabled by the high capacitance. Devices using the SAS dielectric grown on a 100 nm SiO_2 layer exhibit hysteresis comparable to that in devices with SiO_2 alone (Supporting Information).

Low hysteresis allows accurate measurement of both linear and saturation regime behavior. By using a series model of the dielectric

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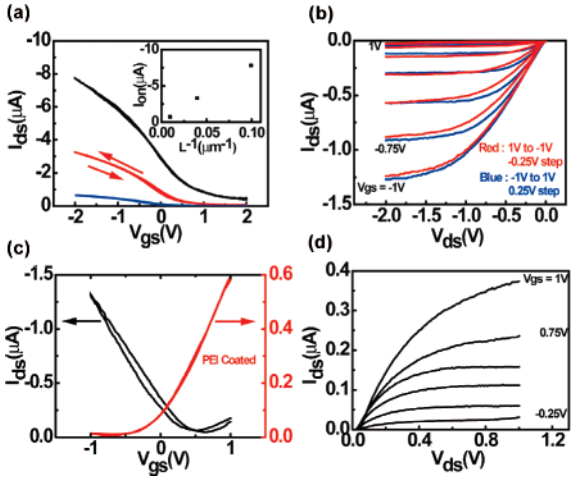

Figure 2. Plot of drain/source current (I_{ds}) as a function of gate voltage (V_{gs}) at a fixed drain/source voltage (V_{ds}) of −0.5 V collected from single-walled carbon nanotube TFTs using a SAS nanodielectric (a). The devices have channel widths (W) of 200 μm and varied channel lengths (L: blue, 100 μm; red, 25 μm; black, 10 μm). The data in the inset of (a) are consistent with the expected linear scaling of the maximum drain/source current (I_{ds}), denoted I_{ON} with L^{-1}. Plot of I_{ds} versus V_{ds} at different gate/source voltages (V_{gs}) collected from devices using a SAS nanodielectric (b). Plot of drain/source current I_{ds} as a function of V_{gs} at $V_{ds} = -1.5$ V before (black) and 1 V after PEI coating (red) (c). Plot of I_{ds} versus V_{ds} at different V_{gs} collected after PEI coating (d). Device in (b−d) have $L = 100$ μm and $W = 200$ μm.

capacitance (C_G) and the quantum capacitance (C_Q) of SWNTs according to $C_T = (1/C_G + 1/C_Q)^{-1}$, and $C_G \approx 170$ nF/cm^2, $C_Q \approx$ 100−400 nF/cm,[2,8] we estimate the total capacitance (C_T) to be ∼60−120 nF/cm^2. (Note that this estimate does not include fringing fields around the SWNT, which can be significant, especially at low tube densities.) Analysis using standard models yields effective device mobilities in the linear and saturation regimes of ∼5.6 ± 0.5 and 5.5 ± 0.4 cm^2/V·s, respectively, for the devices studied here (tube densities ∼10 tubes/μm^2). (Mobilities as high as 30 ± 5 cm^2/V·s are achieved at densities of ∼20 tubes/μm^2, but these devices have correspondingly lower on/off ratios.) The similarity of these quantities and the linear scaling of output current with 1/(channel length) (Figure 2a, inset) are consistent with device operation that is not limited by contacts in the present range of channel lengths. The threshold voltages in the linear and saturation regimes are 0.2 ± 0.05 and 0.3 ± 0.05 V, respectively, and do not vary substantially with channel length. The high capacitance of the dielectric and the good mobility lead to high transconductances of 15 μS at $V_{ds} = -2$ V for 10 μm channel length. The gate leakage current is ∼10 nA at $V_{gs} = -1$ V.

The SAS nanodielectric is also compatible with polymer coating chemistries that switch SWNT TFTs from unipolar p- to unipolar n-channel operation. Thus, a thin layer of polyethyleneimine (PEI, $M_n = 800$) was cast onto the channel regions of the devices, and Figure 2 shows typical n-channel electrical characteristics. Very low hysteresis is again observed, with mobilities and threshold voltages of ∼4.1 ± 0.5 cm^2/V·s and −0.2 ± 0.05 V, respectively. Combining n- and p-channel transistors on a single substrate can yield integrated complementary logic devices. As a simple example, Figure 3 illustrates typical transfer curves of a SWNT/SAS inverter. The high SAS capacitance and good mobilities lead to gains (∼8) that significantly exceed those previously reported for similar SWNT TFT logic gates using SiO_2 dielectrics (100 nm thickness).[7]

In conclusion, we have demonstrated that nanoscopic organic multilayers serve as excellent gate dielectrics for thin film transistors

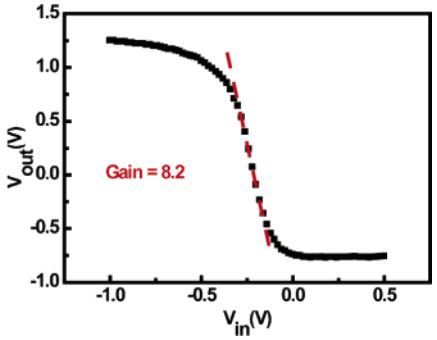

Figure 3. Transfer characteristic of inverter fabricated from p- and n-channel SWNTs/SAS TFTs. Channel length and width are 100 and 200 μm, respectively.

using SWNT semiconductors. These results, coupled with emerging approaches to improve current on/off ratios in SWNT TFTs by eliminating the effects of metallic tubes, suggest the potential importance of new carbon-based electronic materials for high-performance logic circuits, displays, and other systems, especially on plastic substrates.

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Supporting Information Available: AFM image of transferred SWNTs on nanodielectric and hysteresis behavior of SWNTs/SiO_2 (20 and 100 nm) devices. This material is available free of charge via the Internet at http://pubs.acs.org.

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