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Bendable GaAs metal-semiconductor field-effect transistors formed with printed GaAs wire arrays on plastic substrates

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Micro/nanowires of GaAs with integrated ohmic contacts have been prepared from bulk wafers by metal deposition and patterning, high-temperature annealing, and anisotropic chemical etching. These wires provide a unique type of material for high-performance devices that can be built directly on a wide range of unusual device substrates, such as plastic or paper. In particular, transfer printing organized arrays of these wires at low temperatures onto plastic substrates yield high-quality bendable metal-semiconductor field-effect transistors. Electrical and mechanical characterization of devices on poly(ethylene terephthalate) illustrates the level of performance that can be achieved. These results indicate promise for this approach to high-speed flexible circuits for emerging applications in consumer and military electronic systems. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2032609]

Field-effect transistors formed with high-quality single-crystalline semiconductor nano- and microstructures on large-area mechanically flexible plastic substrates are of great interest for a wide range of applications in displays, sensors, medical devices, and other systems.[1–3] A number of approaches have been demonstrated to transfer high-quality semiconductor materials (e.g., Si nanowires, microribbons, platelets, etc.) onto plastic substrates for mechanically flexible metal-oxide-semiconductor field-effect transistors.[4–8] Here, we report a process for fabricating bendable metal-semiconductor field-effect transistors (MESFETs) on plastic substrates using GaAs microwires (a class of material that we refer to as microstructured GaAs, or μs-GaAs) that have integrated ohmic source/drain contacts. The approach uses high-quality bulk GaAs wafers as the starting material, "top-down" fabrication procedures to form the micro/nanowires and transfer printing techniques that use elastomeric stamps to integrate well ordered arrays of these wires with plastic substrates. Electrical and mechanical measurements of MESFETs formed in this way demonstrate the good performance and excellent bendability that can be achieved.

Figure 1 depicts the major steps involved in the process for fabricating μs-GaAs MESFETs on a poly(ethylene terephthalate) (PET) substrate. A (100) semi-insulating GaAs wafer with an epitaxial Si-doped n-type GaAs layer (carrier concentration of $4.0\times10^{17}/\mathrm{cm}^3$, IQE Inc., Bethlehem, PA) provided the source material for generating the microwires. Photolithography and metallization via electron-beam (and/or thermal) evaporation generated arrays of narrow metal stripes (with width of 2 μm and spacing of 13 μm) composed of conventional multilayer stacks, i.e., AuGe(120 nm)/Ni(20 nm)/Au(120 nm) for ohmic contacts. Annealing the wafer at elevated temperature (i.e., 450 °C for 1 min) in a quartz tube with flowing N_2 formed ohmic contacts to the n-GaAs. Defining the metal stripes along the $(0\bar{1}\bar{1})$ crystalline orientation of GaAs enabled microwires (with integrated ohmic contacts) to be generated using a top-down approach described in our previous work.[9,10] In this process, a pattern of photoresist lines was defined on top of the metal stripes; the openings (3 μm widths) between these lines lie between adjacent metal stripes (step i). These openings allowed etchant (H_3PO_4(85 wt %):H_2O_2(30 wt %):H_2O=1:13:12 in volume) to diffuse to the GaAs surface to etch GaAs anisotropically. The photoresist protected the interface between ohmic stripes and GaAs from exposure. The anisotropic etching generated reverse mesas and undercuts

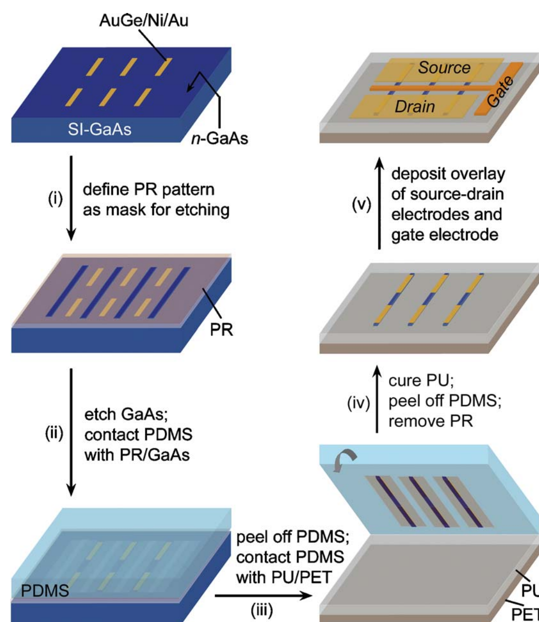

FIG. 1. (Color) Schematic illustration of the major steps for fabricating, on flexible plastic substrates, MESFETs that use arrays of single-crystalline GaAs wires with expitaxial n-type channel layers, and integrated ohmic contacts of AuGe/Ni/Au. Anisotropic chemical etching produces wires from a standard (100) GaAs wafer. A printing technique that uses an elastomeric stamp transfers these wires from the wafer to the plastic device substrate in a manner that preserves spatial organization (i.e., ordered arrays). PR denotes photoresist.

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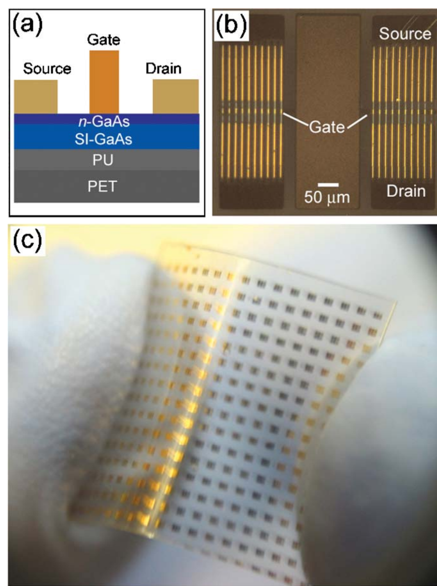

FIG. 2. (Color) (a) Schematic geometry of a GaAs wire-based MESFET on a plastic substrate (PU/PET). The source/drain electrodes form ohmic contacts to the *n*-GaAs layer. The gate electrode forms a Schottky contact to this layer. (b) Optical image of two MESFETs, each of which uses an array of ten GaAs wires. (c) Optical image of a 2 cm × 2 cm PET sheet with hundreds of devices.

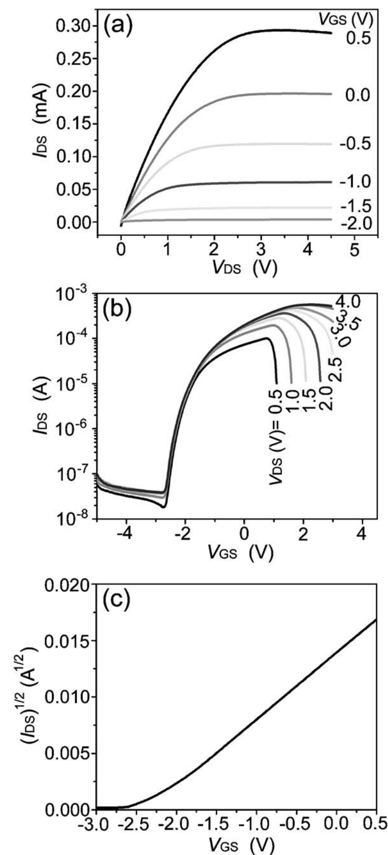

FIG. 3. Electrical response (dc) of a GaAs wire-based MESFET with a channel length of 50 μm and a gate length of 15 μm. (a) Typical *I*-*V* characteristics at gate voltages between 0.5 to -2.0 V with steps of 0.5 V. (b) Transfer curves of this device at different V_{DS}. (c) Transfer curve plotted as $(I_{DS})^{1/2}$ vs V_{GS} at V_{DS}=4.0 V.

along the surface of GaAs, resulting in the formation of GaAs wires with triangular cross section and narrow width released from mother wafer. The undercut can yield GaAs wires with widths down to micrometer and/or nanometer length scales by controlling the geometry of the resist and the etching time.[9] Each wire has two ohmic stripes separated by a gap that defines the channel length of the resultant MESFET. Contacting a flat elastomeric stamp of poly(dimethylsiloxane) (PDMS) to the photoresist-coated GaAs wires formed a van der Waals bond between the hydrophobic surfaces of the PDMS and the photoresist (step ii). This interaction led to the removal of all of the GaAs wires from the wafer to the surface of the PDMS when the stamp was peeled back from the mother wafer (step iii). This process preserved the lithographically defined spatial organization (i.e., aligned arrays) of the wires. The PDMS stamp with GaAs wires was then laminated against a PET sheet covered with a thin layer of liquid polyurethane (PU) (NEA 121, Norland Products Inc., Cranbury, NJ), a kind of photocurable polymer. Curing the PU, peeling off the PDMS stamp, and removing the photoresist by O_2 reactive ion etching (RIE) (Uniaxis 790, Plasma-Therm Reaction Ion Etching System) left the ordered GaAs wires with exposed ohmic stripes embedded on the surface of the PU/PET substrate (step iv). Further lithographic processing on the PU/PET substrate defined electrodes (250 nm Au) that connect the ohmic stripes to form the source and drain, and for gate electrodes [Ti(150 nm)/Au(150 nm)] (step v). The resultant arrays of MESFETs are mechanically flexible due to the bendability of PU/PET sheet (thickness of ~200 μm) and the GaAs wires (widths and thicknesses less than 5 μm).

Figure 2(a) presents a schematic cross section of a μs-GaAs MESFET on plastic. The strong interaction between the cured PU and the side walls of the GaAs wires bonds the wires to the PU/PET substrate. In this geometry and with the processing approach described previously, the active *n*-GaAs layer (i.e., the transistor channel) never contacts any polymeric materials other than photoresist. The Ti/Au gate electrode forms a Schottky contact with the *n*-GaAs surface; the barrier allows one to apply a relatively negative voltage (i.e., <0.5 V) to modulate the flow of current between the source and drain electrodes, as in a conventional MESFET. Figure 2(b) shows a representative image of two GaAs wire-based MESFETs on plastic, fabricated according to the procedures of Fig. 1. The wires have a well-aligned orientation and uniform widths of ~1.8 μm. Au pads with widths of 150 μm and lengths of 250 μm connect the ohmic stripes on ten GaAs wires to form source and drain electrodes for each individual MESFET. A Ti/Au stripe with width of 15 μm deposited in the 50 μm gap (transistor channel) between the source and drain electrodes provides the gate electrode. These stripes connect to a larger metal pad for probing. The contrast difference between the metal on the wires and that on the plastic is likely due to surface roughness on the PU generated during RIE of the photoresist. Figure 2(c) shows the image of a 2 cm × 2 cm PET sheet with a number of transistors, clearly showing its flexibility. Multiple printing steps and/or wire fabrication runs can generate large numbers of wires patterned over large areas on plastic substrates. Various parameters, such as the widths of the GaAs wires, the widths of the source/drain electrodes, the channel, and gate lengths, can be adjusted easily to yield MESFETs with desired output characteristics.

We characterized the dc performance of the transistors. Figure 3 presents results from a GaAs MESFET with a channel length of 50 μm and a gate length of 15 μm, similar to

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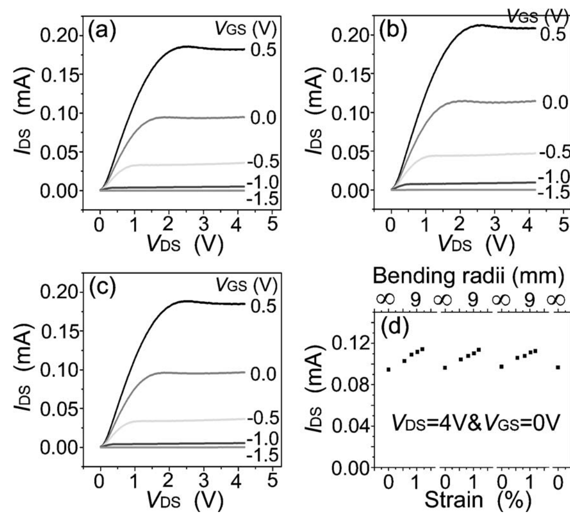

FIG. 4. Gate-modulated current-voltage characteristics of a GaAs wire-based MESFET on a flexible PET substrate (a) before bending; (b) after bending to a bend radius of 8.4 mm (calculated surface tensile strain of 1.2%); and (c) after relaxing the bent substrate to its flat unbent state. (d) Dependence of I_{DS}, measured at V_{DS}=4 V and V_{GS}=0 V, on bend radius and strain.

the one shown in Fig. 2(b). Figure 3(a) shows the current-voltage (*I-V*) (between drain and source electrodes) curves at different gate voltages. The I_{DS}-V_{DS} characteristics are comparable to conventional wafer-based MESFETs built with *n*-type GaAs layer and standard techniques, i.e., I_{DS} saturates in the regions of high V_{DS} and I_{DS} decreases with decrease of gate voltage.[11] In the linear region, the channel resistance at V_{GS}=0 V is $R_{channel}$=6.4 kΩ. The transfer characteristics (i.e., I_{DS} versus V_{GS}) were measured at different V_{DS}, and are shown in Fig. 3(b). All of the curves have minima at the same gate voltage, i.e., −2.65 V. The drop of I_{DS} at high positive gate voltages is due to the significant leakage current from gate to source that develops through the Schottky contact in this regime. Figure 3(c) shows the transfer curve at V_{DS}=4 V, plotted as $(I_{DS})^{1/2}$ versus V_{GS}, clearly showing a linear relationship as expected for a MESFET.[11] The pinch-off voltage and transconductance at I_{DS}=0.19 mA and V_{DS} =4 V are V_p=2.65 V and g_{m0}=168 μS, respectively. These characteristics indicate that the transistors fabricated on PET substrates resemble the behavior of typical GaAs MESFETs fabricated on wafers by traditional approach.

Mechanical flexibility represents a critical parameter of devices on plastic substrates for the target applications that are being considered. We tested the transistors by bending the supporting PET sheet using a setup described elsewhere.[5] Figures 4(a) and 4(b) compare the performance of a transistor before and after the substrate was bent to a radius of 8.4 mm, i.e., corresponding surface stain of 1.2% (tensile in this case) for the 200 μm thick substrate. The results indicate that the transistor can withstand these high strains without failure. In fact, the saturated current at V_{GS}=0 V, increases by ~20% in this case. After releasing the strain, i.e., such that the substrate becomes flat again, the transistor recovers the performance of its original state [Fig. 4(c) versus 4(a)]. Figure 4(d) shows the variation of I_{DS} at V_{DS}=4 V and V_{GS}=0 V in three cycles in terms of bending (with different surface strains)/unbending, indicating that these MESFETs can survive multiple bending cycles that cause the tensile strain at the device to vary between 0% and 1.2%, without a significant change in their performance (<20%). If the tensile strain is higher than 1.25%, I_{DS} decreases with a big jump (>80%), indicating the failure of devices. The systematic changes observed with strain could be related to the fact that mechanical strain causes displacement of crystalline lattice of GaAs wires and their distribution of energy levels.[12] In the absence of additional data, however, it is difficult to assign a specific cause to the reversible variations that we observe.

In summary, this letter reports an approach that involves: (i) the generation of ohmic contacts by high-temperature annealing on GaAs wafers, (ii) the production of GaAs microwires with these integrated ohmic contacts by anisotropic chemical etching, (iii) the dry transfer printing of these wires onto plastic substrates with an elastomeric stamp, and (iv) the fabrication of high-quality MESFETs by low-temperature processing of these wires on plastics, to yield the flexible GaAs MESFETs on plastic substrates. The intrinsic properties of GaAs (e.g., high mobilities), the ability to make the MESFETs with short gate lengths and the straightforward paths for integrating these devices into complex circuits (potentially with other transistors built using similar approaches but with other semiconductors) suggest a strong possibility for achieving high-frequency response for advanced communication, space, and other systems.[13] These advantages as well as the remarkably good mechanical flexibility of these devices make GaAs wire MESFETs interesting for flexible macroelectronic systems.

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