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[18] Version 1.30, July 2003, Wayne Rasband, National Institutes of Health.
[19] The shell thickness cannot be obtained by simply taking the difference in mean diameters between the coated and bare spheres because shrinking of the cores can occur as a result of condensation of unreacted Si-OH groups when the spheres are re-dispersed in a basic solution for coating. See C. J. Brinker, G. W. Scherer, *Sol–Gel Science: The Physics and Chemistry of Sol–Gel Processing*, Academic, Boston, MA **1990**.
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[22] Although the quantum yields of as-synthesized core–shell CdSe/ZnS NCs used were as high as 38 %, subsequent loss of the original surface ligands due to cap-exchange with AP and APS can lead to diminished quantum yields. Furthermore, the decline in the quantum yield due to processing is very dependent on the quality and thickness of the ZnS shell on the NCs, which can vary from sample to sample.
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High-Performance n- and p-Type Single-Crystal Organic Transistors with Free-Space Gate Dielectrics**

By *Etienne Menard*, *Vitaly Podzorov*, *Seung-Hyun Hur*, *Anshu Gaur*, *Michael E. Gershenson*, and *John A. Rogers**

Study of intrinsic transport properties in single-crystal organic semiconductors has the potential to yield fundamental insights into the behavior of plastic transistors for flexible electronics.[1–4] The organic field-effect transistors (OFETs) that facilitate these studies are, however, complex structures whose properties depend on interactions between the semiconductor, gate dielectric, and electrodes.[5–7] Carrier trapping, charge doping, molecular reorientation, dipole formation, and a range of possible chemical interactions are among the many phenomena that can occur at the semiconductor/dielectric interface and degrade device performance.[8–11] We introduce an unusual device design that entirely avoids these effects by replacing the standard solid dielectric layer with a thin free-space gap that can be occupied by air, nitrogen, other gases, or even a vacuum. When combined with high-quality organic crystals, this design reveals the ultimate in OFET performance, determined solely by the intrinsic (not limited by disorder) polaronic transport on the pristine surface of the crystals. We demonstrate this approach by building p- and n-channel devices with extremely good mobilities and normalized sub-threshold slopes.

Unlike the effects associated with electrical contacts, which can be subtracted from the device response by four-point probing or channel-length-scaling analysis, it is difficult or impossible to predict or account for interactions between a semiconductor and a conventional dielectric material.[12,13] The free-space dielectric simply eliminates these effects by eliminating the insulating dielectric material. It is uniquely well-suited to the study of organic semiconductors, which do not possess the types of dangling bonds or surface states that are present in many inorganic materials. Figure 1a schematically

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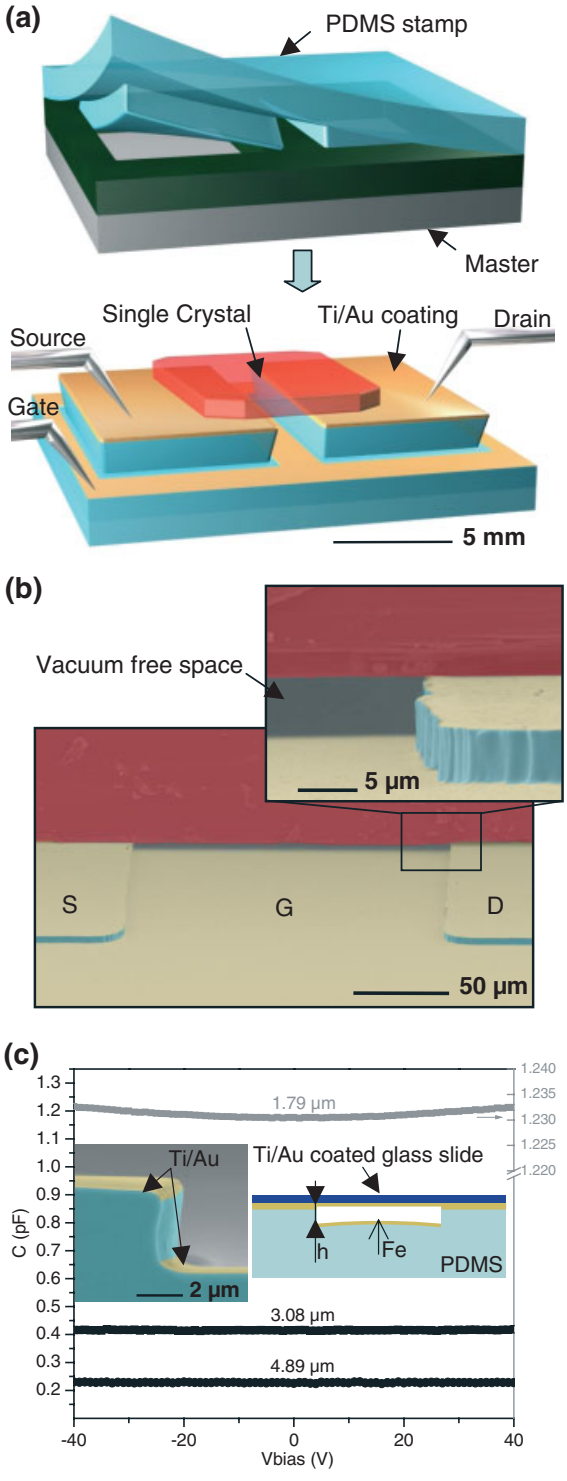

Figure 1. Organic single-crystal transistors with free-space gate dielectrics. a) Schematic illustration of the steps used to produce the devices. b) Scanning electron micrograph of such a device that uses a single crystal of rubrene. c) The capacitance–voltage dependences measured for different air-dielectric thicknesses for test structures with 50 μm × 1.8 mm in-plane dimensions. The results for the 1.79 μm thickness are plotted using the expanded vertical axis (right axis), to give more details about the capacitance variations. The voltage-independent capacitance and the ability to withstand high voltages are two important features for applications as gate dielectrics.

illustrates the steps used in building these devices. Casting and curing a prepolymer of poly(dimethylsiloxane) (PDMS; Sylgard 184, Dow Corning Corp.) against a pattern of photoresist (SU8, Microchem Corp.) on a silicon wafer defines an elastomeric element with relief features in the geometry of the resist. Coating this element with a collimated flux of metal generates electrically isolated electrodes on the raised and recessed regions. This single processing step defines source and drain electrodes (raised regions) together with a self-aligned gate electrode (recessed region). The size of the electrodes and their separation are limited only by the resolution of the soft-lithographic casting and curing procedures: dimensions as small as a few tens of nanometers are achievable.[14] Gently placing a single-crystal sample onto the surface of such an element leads to soft van der Waals' contacts to the source/drain electrodes. The crystal itself forms a free-standing bridge that spans the gap between these electrodes. The thin space between the bottom surface of the crystal and the gate electrode plays the role of the gate dielectric. This space can be filled with any gas (e.g. air) or by a vacuum, depending on the experimental conditions implemented during or after device assembly. Figure 1b shows a scanning electron micrograph of a rubrene single-crystal laminated on top of a Ti/Au-coated (2 nm:20 nm) elastomeric element. The dielectric is vacuum in this case.

These transistors rely critically on acceptable electrical behavior of this unusual type of gate dielectric. The low (3 V μm^{-1}) dielectric strength of most gases together with the low modulus (2–5 MPa) of the elastomer might suggest that devices with this design would be suitable only for very low electric-field operation. Our results show, however, that this inference is incorrect for two reasons. First, the breakdown fields for air gaps which are much narrower than the mean free path of an air molecule can be exceptionally high owing to suppression of the avalanche phenomena that generate discharges in unrestricted geometries.[15] We observed, in agreement with Paschen's law for atmospheric pressures, breakdown voltages greater than 100 V with air gaps as narrow as 1.8 μm. In fact, breakdown of the PDMS (rather than the air) caused by fringing fields at the edges of the device can limit the operating voltages. Second, even relatively large electric fields applied to gaps with these dimensions are insufficient to deform the elastomer. Finite-element modeling indicates that gate biases of 100 V compress air gaps thicker than 3 micrometers (50 μm wide) by less than ~4 nm (Supporting Information, Figs. S1,S2). Figure 1c shows that test structures with air gaps even as thin as ~1.8 ± 0.03 μm exhibit small variations in capacitance (< 0.2 %) for bias voltages up to 40 V. The magnitude of the capacitance, which includes contributions from fringing fields that pass through the elastomer, can be accurately predicted by finite-element modeling of the electrostatics (Supporting Information, Figs. S2,S3). For the voltages probed in the experiments described here moderate fields are achieved, corresponding to charge-doping at the surface of the organic crystal up to 60 nC cm^{-2} or a carrier density up to 4×10^{10} cm^{-2} (2×10^{-4} holes/molecule). It is pos-

sible to operate at fields that are ten times larger than these values. The main limitations are breakdown and onset of deformation in the PDMS the elastomer, which can distort the empty-space dielectric in a way that depends nonlinearly on the electrostatic and surface forces. This deformation can, in some cases, lead to runaway collapse of the empty space. High-modulus materials can eliminate this effect.

We built transistors with a wide range of channel dimensions and dielectric thicknesses using single crystals of two different molecules: tetracyanoquinodimethane (TCNQ) and rubrene. Figure 2a shows the molecular structure and crystal packing of TCNQ,[16] which grows with large, flat facets oriented perpendicularly to the *c*-axis of the crystal. The device geometry and transistor characteristics, obtained using a four-point probe–transistor geometry[1] and a free-space dielectric thickness of 4.7 ± 0.1 μm, appear in Figure 2b. Here, transport occurs in the *a*–*b* plane. The conductivity of the channel, $\sigma = I_{DS}/V_{4W}$ (I_{DS} is the source–drain current, V_{4W} is the potential difference between the voltage probes), increases with increasing positive gate bias, V_G, consistent with n-type behavior. It represents the first n-channel single-crystal organic transistor. The free-space dielectric is critical to the successful operation of the device. Attempts to use conventional solid dielectric materials (PDMS, parylene, and others) resulted in negligibly small mobilities and on/off ratios. A typical result for the case of the PDMS dielectric appears in Figure 2b. We attribute the poor performance to trapping and doping due to the interactions between the dielectric and TCNQ, which has a very high electron affinity.[17] Doping associated with the PDMS dielectric leads to a relatively large "off" conductivity and small "on/off" ratio.

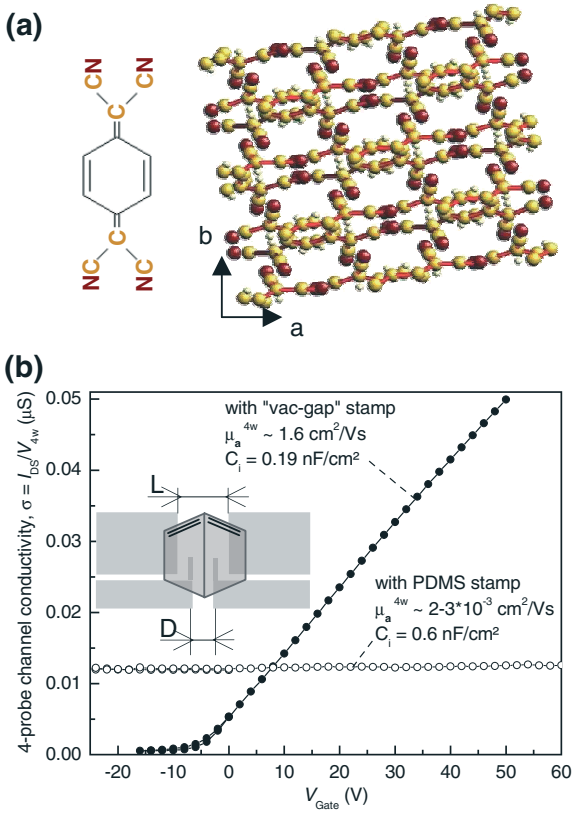

Figure 2. a) Molecular structure and crystal packing in TCNQ. b) Gate-dependent channel conductivity along the *a*-axis of a TCNQ crystal measured by laminating it on top of elastomeric transistor elements that use vacuum and PDMS as gate dielectrics. Intrinsic carrier mobilities in these devices are 1.6 and ~ 2–3 × 10^{-3} $cm^2 V^{-1} s^{-1}$, respectively. The vacuum device has a channel length (*L*) of 1 mm, a channel width (*W*) of 1.15 mm, a dielectric thickness (*d*) of 4.7 μm, and a distance between voltage probes (*D*) of 0.39 mm. The PDMS device used *L* = 1 mm, *W* = 1.3 mm, *D* = 0.25 mm, and *d* ~ 5 μm.

Analysis of the response of the device using standard methods for the linear régime yields a gate-voltage-independent intrinsic carrier mobility of 1.6 ± 0.1 $cm^2 V^{-1} s^{-1}$ and a normalized sub-threshold slope[1b] of 1.5 ± 0.1 > V nF $decade^{-1} cm^{-2}$. These values are better than those of the best thin-film organic n-channel transistors by a substantial margin.[18] Despite the anisotropic shape of the molecules and their packing in the crystal, the transport characteristics depend only very weakly on the orientation of the *a*- and *b*-axes of the crystal relative to the transistor channel (as determined by multiple measurements on a large number of TCNQ crystals). The absence of anisotropy is consistent with our observation that at room temperature, the conductivity of TCNQ transistors is still thermally activated and is dominated by a trap-and-release mechanism.[3]

Figure 3a presents transfer characteristics of rubrene transistors formed with air dielectrics (thickness 4.7 ± 0.1 μm) on the large, flat crystal surfaces that expose the *a*–*b* plane. Effective device mobilities are 13 ± 1 $cm^2 V^{-1} s^{-1}$ along the *b*-axis and 5.5 ± 0.5 $cm^2 V^{-1} s^{-1}$ along the *a*-axis, and on/off ratios are greater than 10^6. These devices, like those built with TCNQ, show no measurable hysteresis (instrument-limited change of < ± 0.2 % in current for a 60 V cycle). They also exhibit little or no degradation of the transfer characteristics after detaching and then re-attaching a crystal onto the elastomeric element, or during measurements for periods of many hours, and storage for days. The devices behaved like ideal, long, channel transistors[19] with very good quadratic scaling of the saturation current with gate voltage (Fig. 3b). Linear- and saturation-régime effective mobilities are similar (within ~ 10 %), indicating a good carrier injection at the laminated source contact. Four-point probing structures allow separate measurement of the contact resistance and the channel resistance.[1] The results reveal intrinsic mobilities as high as 20 ± 2 $cm^2 V^{-1} s^{-1}$ for transport along the *b*-axis.[3] As expected for Schottky contacts the resistivity decreases with increasing gate bias and increases with decreasing temperature, in accordance with the thermionic-emission model (Fig. 3c inset).[18] A semi-log plot of the resistance as a function of temperature can be fit by two linear segments. Interestingly, the crossover between these régimes at ~ 175 K correlates with the observed transition from the intrinsic polaronic transport to the trap-dominated conduction in the channel.[3] At low temperature, the transport in the channel is thought to be dominated by trapping processes, which might be responsible for the larger

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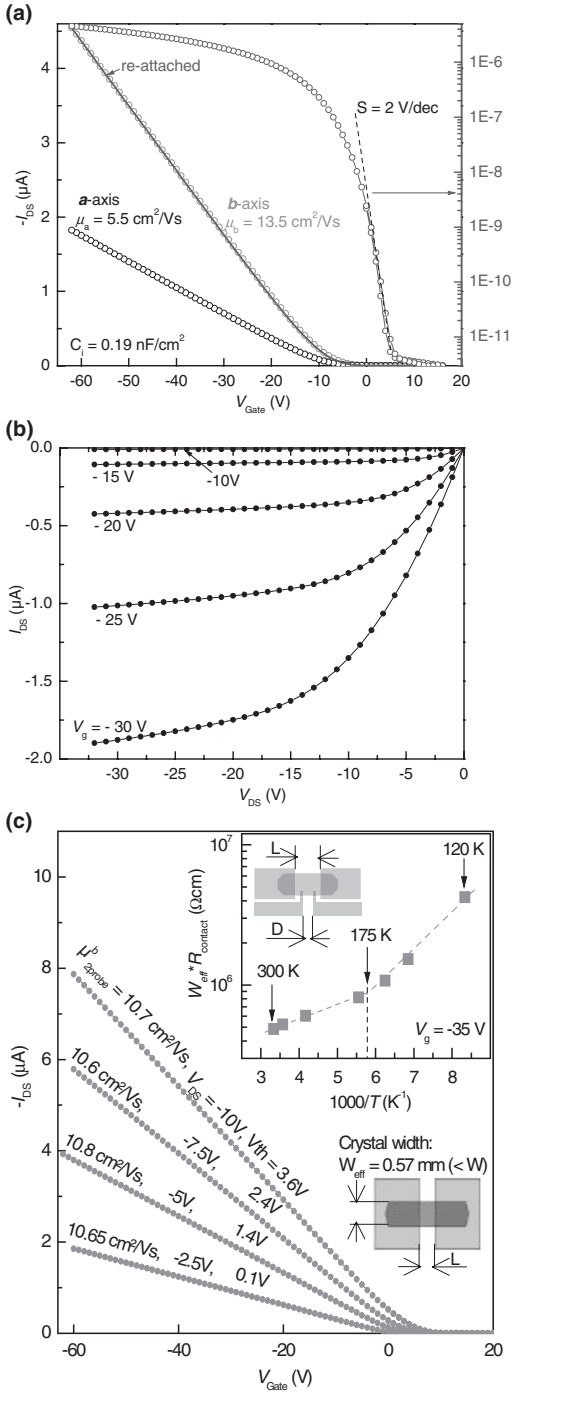

Figure 3. Rubrene field-effect transistor that uses air as the gate dielectric, with source/drain electrodes oriented along the *a*- and *b*-axes of the single crystal. a) The transfer characteristics have been measured at the source/drain voltage $V_{DS} = -5$ V after the crystal was laminated (circles), peeled back, and re-attached (solid line). The transfer characteristic along the *b*-axis is also shown in semi-log plot (right axis) ($L = 149$ μm, $W = 1$ mm, $d = 4.7$ μm). b) Current–voltage characteristics measured along the *b*-axis ($L = 196$ μm, $W = 1$ mm, $d = 4.7$ μm). c) Transfer characteristics along the *b*-axis measured at different values of V_{DS} ($V_{DS} = -10 - -2.5$ V, $L = 149$ μm, $W_{eff} = W_{crystal} = 0.57$ mm, $d = 3$ μm). The inset shows an Arrhenius plot of the normalized contact resistance ($W_{eff} \times R_{contact}$) for transport along the *b*-axis ($L = 0.75$, $W_{eff} = 1.25$ mm, $D = 0.25$ mm, $C_i = 0.2$ nF cm^{-2}).

slope of the contact resistance versus $1/T$ plot. The connection between the properties of the contacts and the transport in the channel remains unclear; it is a topic of current study.

The transport characteristics of the conducting channel depend critically on the properties of the rubrene crystals and, in particular, on the interface between the rubrene and air. Atomic force microscopy (AFM) measurements reveal monomolecular steps (heights of $\sim 1.5 \pm 0.1$ nm) on the *a*–*b* plane with a preferred orientation along the *b*-axis (Fig. 4a, inset) in most samples. These steps may affect the transport: it is expected that the effect of steps should become increasingly im-

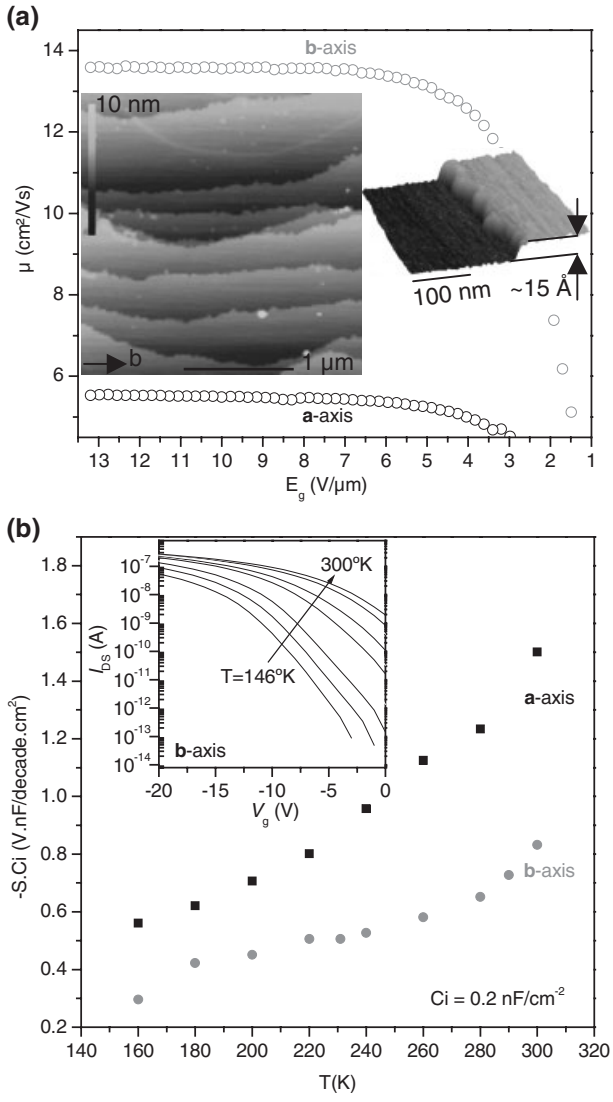

Figure 4. Semiconductor–gate-dielectric interface characterization. a) Variation of the linear-régime carrier mobility along the *a*- and *b*-axes of a single rubrene crystal as a function of the gate electric field measured in an air-gap transistor. The inset shows low- and high-resolution AFM images of the *a*–*b* plane surface of a typical rubrene crystal sample. b) Variation of the normalized sub-threshold swing with temperature for a rubrene crystal along the *a*- and *b*-axes. The inset shows, on a semi-log plot, the transfer characteristics measured along the *b*-axis at different temperatures.

portant at stronger gate fields, when the carriers are pulled closer to the crystal surface.[20] Our observation that the mobilities along both the *a*- and *b*-axis directions are independent of the gate-induced electric field over a wide range of V_g (Fig. 4a) suggests that the effect of steps is minor in the case of the studied crystals, which have a relatively low density of steps.

The high quality of the rubrene/air-dielectric interface clearly manifests itself in the sub-threshold device behavior. Figure 4b presents the temperature dependence of the drain current as a function of gate voltage in the sub-threshold region (the inset). As expected, the sub-threshold swing increases linearly with temperature for transistors measured along the *a*- or *b*-axis of the rubrene.[19] At room temperature, the normalized sub-threshold swings along the *b*-axis varied typically from 0.4 to 0.8 V nF decade^{-1}cm^{-2}, with a 'best' value of 0.38 ± 0.04 V nF decade^{-1}cm^{-2}.

Laminated single-crystal organic transistors with vacuum dielectrics represent perhaps the most straightforward route to artifact-free measurement of the intrinsic gated transport in this class of materials. The results presented here demonstrate many features of this approach, including its successful use with two classes of small-molecule organics to yield n- and p-channel devices with exceptionally good properties. Temperature-dependent measurements and surface-analytic studies reveal some basic aspects of transport, contacts, and semiconductor/dielectric properties. The approach also provides i) sufficiently high resolution for transport studies on nanometer length-scales, ii) reversible device assembly for studies of device reliability, and iii) direct access to the accumulation channel for sensing applications. These areas represent fruitful directions for research.

Experimental

Building the Transistors: Casting and curing a liquid prepolymer against a 'master' with suitable relief structures in photoresist defined a soft rubber element. Collimated deposition of a metal coating produced, in a single step, source/drain electrodes and a self-aligned gate electrode on this element with geometries defined by the master. Laminating an organic single-crystal on top of this structure completed the fabrication of a transistor whose gate dielectric was defined by the free space, or gap, below the bottom surface of the crystal and the top surface of the gate electrode. The electric measurements of the FETs' characteristics were carried out using Keithley SourceMeters K2400, and Electrometers K6512 and K617. For the measurement of the TCNQ single-crystal devices, the chamber of the probing station was evacuated with a zeolite sorption pump which created a vacuum of ~1 mtorr.

Preparing the Masters: SU-8 photoresist was spin-coated at 3000-5000 rpm, pre-baked at 120 °C for 5 min, exposed to UV light for 8 s (~160 mJ cm^{-2}), post-baked at 95 °C for 3 min, and then developed for ~20 s in SU-8 developer.

Preparing the Stamps: PDMS (Sylgard 184 from Dow Corning, www.dowcorning.com) was mixed and degassed, poured over the masters and cured in an oven at 80 °C . Immediately before loading the stamp in an electron-beam chamber, its surface was plasma-oxidized using an Uniaxis 790 Plasma-Therm Reactive Ion etching system in an oxygen flow of 20 standard cubic centimeters per minute, at a pressure of 30 mtorr for 20 s with 10 W of radiofrequency power. The 2 ± 0.4 nm of Ti (0.3 nm s^{-1}) and 20 ± 4 nm of Au (1 nm s^{-1}) were sequentially evaporated with a Temescal electron-beam system (BJD 1800). Pressures during evaporation were typically $\sim 3 \times 10^{-6}$ torr or less.

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