Bendable single crystal silicon thin film transistors formed by printing on plastic substrates

E. Menard, R. G. Nuzzo, and J. A. Rogers[a)]
University of Illinois at Urbana-Champaign, Department of Materials Science and Engineering, Department of Chemistry, Beckman Institute and Frederick Seitz Materials Research Laboratory, Urbana, Illinois 61801

(Received 25 October 2004; accepted 13 January 2005; published online 25 February 2005)

Bendable, high performance single crystal silicon transistors have been formed on plastic substrates using an efficient dry transfer printing technique. In these devices, free standing single silicon objects, which we refer to as microstructured silicon (μs-Si), are picked up, using a conformable rubber stamp, from the top surface of a wafer from which they are generated. The μs-Si is then transferred, to a specific location and with a controlled orientation, onto a thin plastic sheet. The efficiency of this method is demonstrated by the fabrication of an array of thin film transistors that exhibit excellent electrical properties: average device effective mobilities, evaluated in the linear regime, of $\sim$240 $cm^2/V\,s$, and threshold voltages near 0 V. Frontward and backward bending tests demonstrate the mechanical robustness and flexibility of the devices. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1866637]

Flexible, large area circuits represent a new form of electronics that could have wide ranging applications in sensors, displays, medical devices, and other areas. Fabricating the required transistors on plastic substrates represents a challenge to achieving these "macroelectronic" systems. Some approaches use modified, low temperature versions of fabrication strategies for amorphous or polycrystalline silicon thin film transistors.[1] The high temperatures associated with directional solidification processes for producing single-crystal silicon films make them unsuitable for use with plastic substrates.[2] Pulsed laser based approaches have achieved some success, although their use with plastic substrates remains a topic of current study.[3,4] Direct full wafer transfer of preformed circuits onto plastic substrates can yield the necessary devices, but this approach is difficult to scale to large areas and it does not retain printing type fabrication sequences that might be important for low cost, large area macroelectronics.[5] Organic semiconductor materials provide an alternative path to flexible electronics; here the organic based electronic materials can be naturally integrated, via room temperature deposition, with a range of plastic substrates.[6,7] Known organic semiconductors, however, enable only modest device mobilities. Even high quality single crystals of these materials have mobilities in the range of $1-2\ cm^2/V\,s$ and $\sim 10-20\ cm^2/V\,s$ for *n*- and *p*-type devices, respectively.[8–10]

Innovative approaches such as fluidic assembly of prefabricated semiconductor nanowires can be used to build devices on plastic substrates.[11] The manufacturability of these methods is uncertain, and the properties of the semiconductors (e.g., doping levels, etc.) are often not well known. A room temperature dry transfer printing technique, with potentially excellent registration capability,[12] has been successfully used to deposit on plastic substrates a range of high quality semiconductors, including single crystal Si ribbons,[13] Ga–As and InP wires,[14] and single-walled carbon nanotubes.[15] This letter describes the fabrication, electrical characteristics, and mechanical bendability of thin film type transistors formed with well organized arrays of dry transfer printed silicon ribbons, which we refer to as microstructured silicon (μs-Si) on low cost plastic substrates. An important result is that the bendability (i.e., strain at which failure occurs) is comparable to that of devices made with organic semiconductors.

Figure 1(a) illustrates the steps used to fabricate the devices. First, photolithography defined a pattern of photoresist on the surface of a silicon-on-insulator wafer (Soitec unibond SOI with a 100 nm top Si layer and 145 nm buried oxide). This resist served as a mask for dry etching the top silicon layer of the SOI wafer with a SF_6 plasma (Plasmatherm RIE system, 40 sccm SF_6 flow with a chamber base pressure of 50 mTorr, 100 W rf power for 25 s. A concentrated HF solution etched the buried oxide and freed (but did not completely float off) the Si objects from their substrate. A flat piece of poly(dimethylsiloxane) (PDMS) was brought into conformal contact with the top surface of the wafer and then carefully peeled back to pickup the interconnected array of ribbons. The interaction between the photoresist and the PDMS was sufficient to bond the two together for removal, with good efficiency. An indium-tin-oxide (ITO) thickness $\sim$100 nm coated poly(ethyleneteraphtalate) (PET) (thickness $\sim 180\ \mu m$) plastic sheet served as the device substrate. Washing it with acetone and isopropopanol, rinsing it with de-ionized water, and then drying it with a stream of nitrogen cleaned its surface. Treating the ITO with a short oxygen plasma (Plasmatherm RIE system, 20 sccm O_2 flow with a chamber base pressure of 100 mTorr, 50 W rf power for 10 s) promotes adhesion between it and a spin cast dielectric layer of epoxy (3000 rpm for 30 s of Microchem SU8-5 diluted with 66% of SU8-2000 thinner). This photosensitive epoxy was precured at 50 °C on a hot plate during $\sim$1 min. Bringing the PDMS with the μs-Si on its surface into contact with the warm epoxy layer and then peeling back the PDMS led to the transfer of the μs-Si to the epoxy. Evidently, the bonding forces between the silicon and the soft epoxy layer

a)Author to whom correspondence should be addressed; electronic mail: jrogers@uiuc.edu

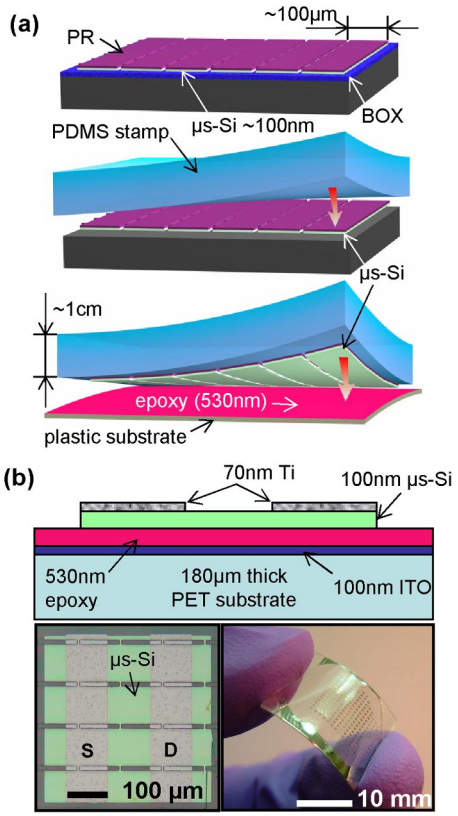

FIG. 1. (Color online) (a) Schematic illustration of steps for transfer printing microstructured silicon (μs-Si) ribbons to a plastic substrate. (b) Device structure schematic of a high performance thin film transistor built on a PET substrate. The bottom insets show high and low magnification optical images of a device array. Each device uses four interconnected microstrips of 100-nm-thick single crystal silicon.

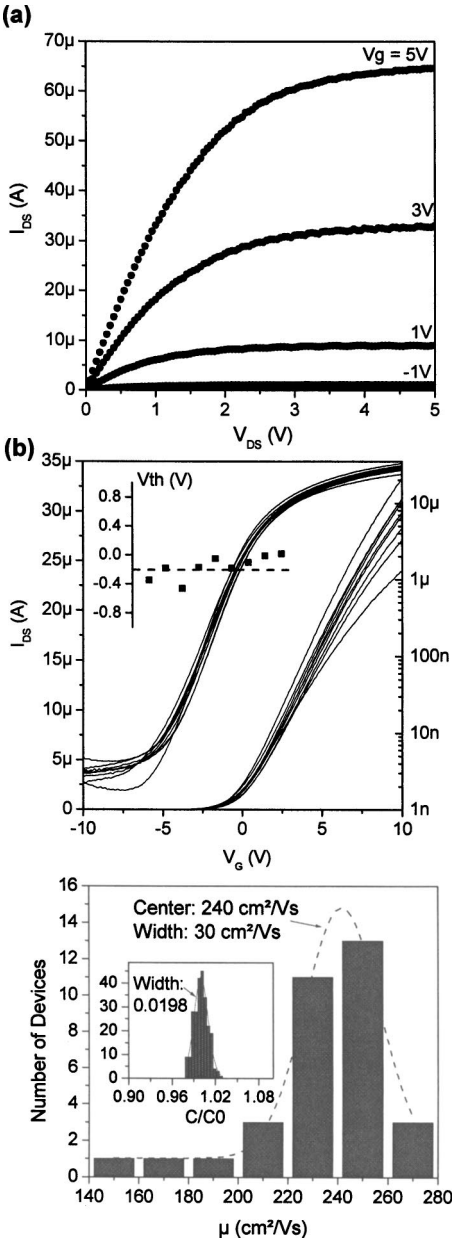

FIG. 2. Electrical characterization of the high performance thin film transistor devices on PET substrate. Part (a) shows $I-V$ characteristics of one of the devices. Part (b) shows on a linear (left axis) and logarithm (right axis) plot several transfer characteristics of the transistors measured at a drain-source bias $V_{DS}=0.5$ V. The threshold voltage values of these devices are displayed on the inset plot. Part (c) shows the distribution of the devices' field effect mobilities. The inset shows the very compact Gaussian distribution of the gate dielectric capacitances values measured on a ~15 $\times$15 mm array of 256 capacitors.

(some of which are mechanical, due to the flow of epoxy around the μs-Si edges) are stronger than those between the photoresist and the PDMS stamp. The epoxy layer was fully cured at 100 °C for 5 min, exposed to UV light from the backside of the transparent substrate for 10 s, and then post-baked at 115 °C for 5 min to crosslink the polymer. The photoresist mask (which, conveniently, prevents contamination of the top surface of the Si during the transfer steps) was dissolved with acetone and the sample was then abundantly rinsed with de-ionized (DI) water. Source and drain electrodes were formed with Ti (~70 nm; Temescal electron beam evaporator) deposited on the top Si surface. Etching (1:1:10 $HF:H_2O_2:DI$ for ~2 s) through a photoresist mask (Shipley S1818) patterned on the Ti defined the geometry of these electrodes. The last step of the fabrication involved dry etching (SF_6 using the RIE parameters given earlier) through a photoresist mask to define islands of silicon at the locations of the devices. Figure 1(b) presents a schematic illustration of this bottom gate device configuration together with high and low magnification optical images of part of the device array.

Figure 2(a) presents current voltage characteristics of a device that shows an effective device mobility of 140 $cm^2/V\,s$ in the saturation regime and 260 $cm^2/V\,s$ in the linear regime, as evaluated by application of standard field effect transistor models that ignore the effects of contacts.[16] The high resistance (~90 Ω cm) of the Schottky contacts in these devices, however, has a significant effect on the device response. Figure 2(b) presents transfer characteristics of several devices, plotted on linear (left axis) and logarithmic (right axis) scales. The plot in the inset shows that the threshold voltages have a narrow distribution near 0 V. Small (<4% in current for a ±10 V cycle) hysteresis in the transfer characteristics indicates a low density of trapped charge at the interface between the silicon (with native oxide) and the epoxy dielectric. The small values ($\leqslant$13 V nF/dec cm^2) of the normalized subthreshold slopes confirm the good quality of this interface, which may be governed primarily by the interface between the silicon and its native oxide. Figure 2(c) shows the distribution of the linear effective mobilities of the devices. A Gaussian fit indicates a center value of 240 $cm^2/V\,s$ with a standard devia-

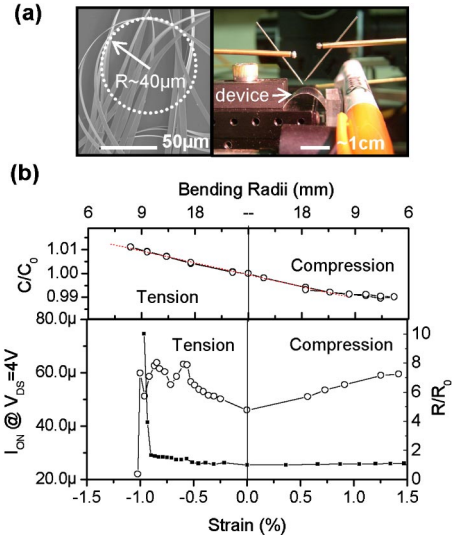

FIG. 3. (Color online) Bending test of the devices built on a 180-μm-thick PET plastic substrate. Part (a) left inset shows a high-resolution scanning electron microscopy pictures of μs-Si ribbons solution deposited on the surface of a silicon wafer. The right inset shows a picture of the precision mechanical stage used to frontward (and backward) bend the plastic circuit. Part (b) shows the variation of the dielectric capacitance value together with the device saturation current when the plastic circuits are subject to compressive or tensile mechanical strain. The ITO normalized resistivity is plotted on the right axis.

tion of 30 $cm^2/V\,s$. Some of the low values are associated with visible defects in the electrodes or other components of the devices. The uniformity of the epoxy dielectric was investigated by building, using the same substrate and methods used to prepare the transistor gate dielectric, an array of 256 (200×200 μm) square capacitors. The inset shows the measured capacitance values. A Gaussian fit indicates a standard deviation lower than 2% confirming the excellent electrical and physical properties uniformity of the epoxy layer. Capacitance measurements carried out at various frequencies (between 1 kHz and 1 MHz) indicated a small ($<3\%$) frequency dependence of the dielectric constant.

The mechanical flexibility and robustness of these devices were investigated by performing frontward and backward bending tests. Figure 3(a) left inset presents a high-resolution scanning electron micrograph of solution cast ribbons illustrating the remarkable flexibility of the thin Si objects. The right inset shows a picture of the setup used to bend the devices. A relatively thick (~180 μm) plastic substrate was used in order to maximize the strain induced in the devices when the plastic sheet is bent. Figure 3(b) top inset shows the small ($\sim<1\%$) linear variation of the epoxy dielectric capacitance when subject to tensile and compressive strains. The bending radius and strain values where computed using a finite element model of the buckling sheet. Comparisons of the bending profiles of the buckling sheet (for several bending radius) to the profiles obtained with the finite element method confirmed the accuracy of the simulations. The second inset presents the variation of the saturation current of a device measured for a gate and drain bias voltages of both 4 V. The maximum value of the tensile strain at which the device can be operated seems to be limited by the failure of the ITO gate electrode (which fails a tensile strain value of $\sim-0.9\%$). The devices operate well even at compressive strains as high as 1.4%. This level of bendability is comparable to that recently reported for organic transistors based on pentacene. The failure mechanism of our silicon devices is the subject of current study. Takahiro *et al.* demonstrated that micron-sized single crystal silicon objects etched from the top layer of a SOI wafer can withstand remarkably high tensile stress ($>6\%$).[17] The cause of the modest variation in output current with strain in our devices requires further investigation. The known variation in mobility with strain contributes (but does not fully account for) these changes. Devices of the type that we describe here might, in fact, enable opportunities to investigate the charge transport in mechanically strained silicon at strain values not easily reached when bulk Si wafers are bent.[18]

In summary, this letter demonstrates bendable single crystal silicon transistors formed on plastic substrates by a simple and efficient parallel printing process for the silicon. The same general approaches are also applicable to devices that use other inorganic semiconductors (e.g., GaAs, GaN, etc.). This type of technology could be useful for a range of applications in macroelectronics, and possibly other areas.

The work was partially supported by the Defense Advanced Projects Agency under Contract No. F8650-04-C-710 and by the U.S. Department of Energy under Grant No. DEFG02-91-ER45439. Devices were fabricated using the Frederick Seitz Materials Research Laboratory facilities and characterized in the Center for Microanalysis of Materials, University of Illinois, which is partially supported by the U.S. Department of Energy under Grant No. DEFG02-91-ER45439. Scanning electron microscopy imaging and finite element modeling were carried out at the Beckman Institute.

[1]For reviews and references, see *Thin Film Transistors*, edited by C. R. Kagan and P. Andry (Marcel Dekker, New York, 2003).
[2]E. I. Givargizov, *Oriented Crystallization on Amorphous Substrates* (Plenum, New York, 1991).
[3]S. D. Theiss, P. G. Carey, P. M. Smith, P. Wickboldt, T. W. Sigmon, Y. J. Tung, and T.-J. King, Tech. Dig. - Int. Electron Devices Meet. **1998**, 257.
[4]M. A. Crowder, P. G. Carey, P. M. Smith, R. S. Sposili, H. S. Cho, and J. S. Im, IEEE Electron Device Lett. **19**, 306 (1998).
[5]Y. Lee, H. Li, and S. J. Fonash, IEEE Electron Device Lett. **24**, 19 (2003).
[6]M. Ando, M. Kawasaki, S. Imazeki, H. Sasaki, and T. Kamata, Appl. Phys. Lett. **85**, 1849 (2004).
[7]H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, J. Appl. Phys. **92**, 5259 (2002).
[8]E. Menard, V. Podzorov, S.-H. Hur, A. Gaur, M. E. Gershenson, and J. A. Rogers, Adv. Mater. (Weinheim, Ger.) **16**, 2097 (2004).
[9]C. Goldmann, S. Haas, C. Krellner, K. P. Pernstich, D. J. Gundlach, and B. Batlogg, J. Appl. Phys. **96**, 2080 (2004).
[10]For reviews and references, see R. W. I. De Boer, M. E. Gershenson, A. F. Morpurgo, and V. Podzorov, Phys. Status Solidi A **201**, 1302 (2004).
[11]S. Jin, D. Whang, M. C. McAlpine, R. S. Friedman, Y. Wu, and C. M. Lieber, Nano Lett. **4**, 915 (2004).
[12]E. Menard, L. Bilhaut, J. Zaumseil, and J. A. Rogers, Langmuir **20**, 6871 (2004).
[13]E. Menard, K. J. Lee, D.-Y. Khang, R. G. Nuzzo, and J. A. Rogers, Appl. Phys. Lett. **84**, 26 (2004).
[14]Y. Sun and J. A. Rogers, Nano Lett. **4**, 1953 (2004).
[15]M. A. Meitl, Y. Zhou, A. Gaur, S. Jeon, M. L. Usrey, M. S. Strano, and J. A. Rogers, Nano Lett. **4**, 1643 (2004).
[16]S. Sze, *Semiconductor Devices: Physics and Technology* (Wiley, New York, 1985), pp. 204–206.
[17]T. Namazu, Y. Isono, and T. Tanaka, J. Microelectromech. Syst. **9**, 450 (2000).
[18]S. Maikap, C.-Y. Yu, S.-R. Jan, M. H. Lee, and C. W. Liu, IEEE Electron Device Lett. **25**, 40 (2004).