NANO LETTERS

2004
Vol. 4, No. 10
1953−1959

Fabricating Semiconductor Nano/Microwires and Transfer Printing Ordered Arrays of Them onto Plastic Substrates

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Received July 22, 2004; Revised Manuscript Received August 5, 2004

ABSTRACT

Ordered arrays of single-crystalline nano- and microwires of GaAs and InP with well-controlled lengths, widths, and cross-sectional shapes have been fabricated over large areas from high quality bulk wafers by the use of traditional photolithography and anisotropic, chemical wet etching. A printing technique using elastomeric stamps can transfer these wire arrays to plastic substrates, with excellent retention of order and crystallographic orientation of the wires. Electrical measurements on simple test structures demonstrate the high degree of mechanical flexibility of the resulting wire arrays on plastics. The combination of "top down" wire fabrication and "dry" transfer printing might represent an effective route to ultrahigh performance macroelectronic systems.

Semiconducting materials that are processed into free-standing elements such as wires, ribbons, platelets, rods, crystallites, and other shapes gain interesting new properties compared to their bulk counterparts. For example, they can be dispersed in solution and transferred to virtually any substrate, including low-cost plastics and even paper, both of which are intrinsically incompatible with procedures used to make conventional bulk wafers of most inorganic semiconductors.[1] Also, the properties of these elements can depend strongly on their geometry; this attribute offers new application possibilities.[2,3] Many classes of devices can be built with wires, ribbons, or other structures that have aspect ratios large enough to enable easy electrical connection.[4]

Compound III−V semiconductors are core active materials for high-speed digital circuits, monolithic microwave integrated circuits, RF communications, and high performance optoelectronic devices (e.g., laser diodes, light emitting diodes, and photodiodes) because of their high electron mobility, high saturated drift velocity, wide direct band gap, and wide range of working temperature.[5,6] Nanowires of these materials (e.g., GaAs and InP) can be prepared in gaseous media as well as in liquid media. The gas-phase procedures are generally guided by the vapor−liquid−solid (VLS) mechanism in which vapors of target materials are generated by laser ablation[7] and/or thermal decomposition of corresponding compounds.[8] In a typical synthesis, metal nanoparticles (e.g., Au, Ag, and Cu) catalyze the growth of the nanowires. The vapor determines the composition of the wires, and the size of the particles determines their diameter. Buhro and co-workers extended the VLS growth process to liquid phase by using nanoparticles made of metals (e.g., In and Ga) with low melting points as catalysts (called solution−liquid−solid process, or SLS).[9] For example, GaAs nanowires with diameters of 6.0−16.8 nm and narrow diameter distributions (i.e., 14.1−16.2%) are generated by refluxing 1,3-diisopropylbenzene solutions of $(^tBu)_3Ga$ and $As(SiMe_3)_3$ in the presence of In nanoparticles.[9b] Korgel et al. demonstrated that metal nanoparticles (i.e., Au) with high melting points could serve as catalysts to prepared GaAs nanowires when supercritical hexane was used as reaction medium.[10] The synthesized nanowires usually are produced in the form of random assemblies on substrates (for VLS growth) or in solution (for SLS growth). The resultant nanowires always have very broad length distributions, with maximum lengths in the range of 100 μm.[7−10] The growth conditions (i.e., carrier gas flow, temperature, etc.) and the diameter distribution of catalysts lead to some dispersion in wire diameter. In most cases, it remains unclear how the purity, doping, crystallinity, and other related properties of wires formed using these synthetic, or "bottom up", ap-

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10.1021/nl048835l CCC: $27.50
Published on Web 08/18/2004

proaches compare to bulk single crystal wafers that are grown and doped using the extremely well controlled techniques that have been developed over the last several decades to support the semiconductor industry.

Organization of high quality nanowires into ordered architectures is critical for the fabrication of functional devices.[1,11] The assembly of semiconductor nanowires/microwires on plastic substrates is particularly important since electronic devices built on plastics with inorganic semiconductors might provide merits in terms of performance, flexibility, reliability, and cost compared to analogous devices built with organic semiconductors or amorphous silicon.[1] Wires can be aligned to some degree by microfluidic shear forces, electric fields, and Langmuir−Blodgett (LB) based techniques.[12] Scaling these approaches to high speeds and large areas might be challenging. Also, the uniformity in wire spacing, length, and crystalline orientation all require improvement for many applications. Vertically aligned GaAs (or InP) wires can be produced by predepositing metal catalyst (random or patterned distributions) on a GaAs (or InP) wafer with orientation of (111)B (i.e., the growth direction of wires), followed by growth via the VLS process.[13] These kinds of wire arrays are well aligned on the mother substrate, but they might be difficult to transfer to plastic sheets while preserving their order.

Here we report a simple "top down" approach to the fabrication of nanowires/microwires of GaAs and InP that combines conventional lithographic techniques and anisotropic chemical etching with high quality bulk single-crystal wafers of GaAs or InP. This approach gives excellent control over wire width, length and spatial position. Wire arrays generated in this manner can be dry transfer printed onto plastic substrates with good retention of order and crystallographic orientation. Electrical measurements show that simple devices built on these substrates have good mechanical flexibility. These approaches might be important for future large area, high performance "macroelectronic" systems.

Figure 1 summarizes steps for generating and transferring nanowire arrays of GaAs to a plastic substrate, e.g., a poly(ethylene terephthalate) (PET) sheet coated with a thin layer of cured polyurethane (PU). The process begins with a piece of GaAs wafer with its surface oriented along the (100) direction (American Xtal Technology, Fremont, CA). Defining an etch mask of SiO_2 in the form of lines oriented along the $(0\ \bar{1}\ \bar{1})$ direction prepares the structure for anisotropic etching in the aqueous solution of H_3PO_4 and H_2O_2 consisting of H_3PO_4 (85 wt %): H_2O_2 (30 wt %): H_2O = 1:13:12 in volume (step i).[14] This etching chemistry, when applied in this fashion, exhibits high anisotropy, i.e., sharply defined reverse mesa-shaped profiles are generated under the SiO_2 mask stripes.[15] For sufficient etching times, the two side walls of each reverse mesa intersect, resulting in the formation of a wire with triangular cross section (see the top inset of Figure 1A). When the patterned SiO_2 lines are surrounded by bulk SiO_2 film, both ends of each GaAs wire connect to the mother wafer. This connection confines the wires and preserves the spatial orientation and layout defined by the pattern of SiO_2. Free-standing GaAs wires (see a typical SEM shown in Figure 2A) can be obtained from GaAs wafer patterned with isolated SiO_2 lines. It is worthy of note that lateral undercutting of GaAs occurs along with the vertical etching, resulting in the ability to decrease the width of resultant GaAs wires down to nanometer scale even with SiO_2 lines that have micron widths.

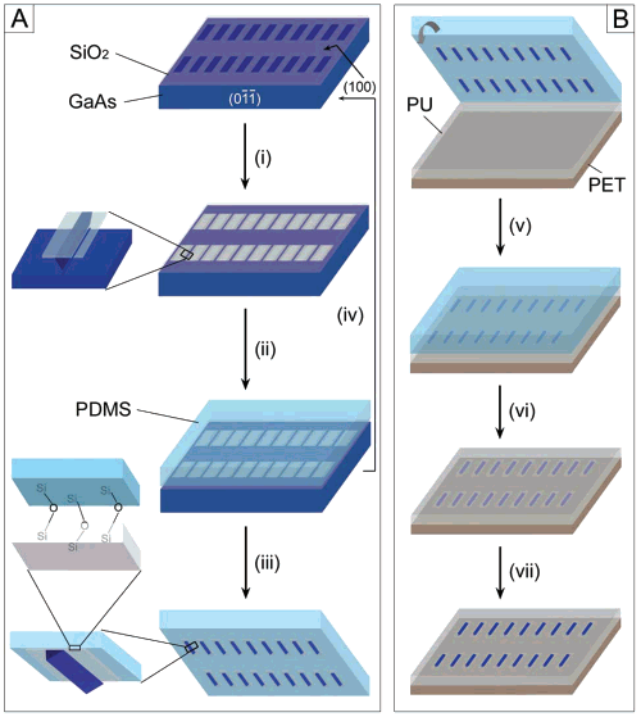

Figure 1. Schematic illustration of the process of generating and transfer printing GaAs wire arrays onto plastic substrates. (A) The steps involved in the fabrication and transfer of GaAs wire arrays to a PDMS stamp: (i) anisotropic chemical etching of a GaAs wafer using SiO_2 stripes as mask produces GaAs nanowire arrays; (ii) contact between PDMS and SiO_2 leads to the formation of siloxane (Si−O−Si) bonds via a condensation reaction; (iii) peeling the PDMS stamp from the GaAs substrate lifts off the wires; (iv) polishing the remaining GaAs wafer enables a new cycle of wire fabrication and lift-off. (B) The steps involved in the transfer process of GaAs wire arrays from PDMS stamp to PET sheet coated with a thin layer of PU: (v) contact between a PDMS stamp (with GaAs wires) and liquid film of PU cast on PET sheet causes the PU to flow to conform to the wires; (vi) curing PU with UV light bonds the wires to the PU and the PU to the PET then peeling off the PDMS stamp leaves the wires embedded in PU; (vii) BOE etching removes the SiO_2.

GaAs wire arrays can be transfer printed to plastic sheets with retention of the orientation and relative position of individual wires. In the first step, a conformable elastomeric transfer element (i.e., flat piece of poly(dimethylsiloxane), or PDMS, Sylgard 184, A/B = 1:10, Dow Corning) is placed on the GaAs wafer to pick up the wires (step ii). Relatively strong bonding between the PDMS sheet and the SiO_2 mask layer is required to break the crystalline connections to the underlying substrate at the ends of wires. Cleaning the PDMS stamp and GaAs wafer (with SiO_2 mask) with a weak oxygen plasma can promote the formation of covalent siloxane (Si−O−Si) bonds between PDMS and SiO_2 by a condensation reaction (see the middle inset of Figure 1A).[16] The

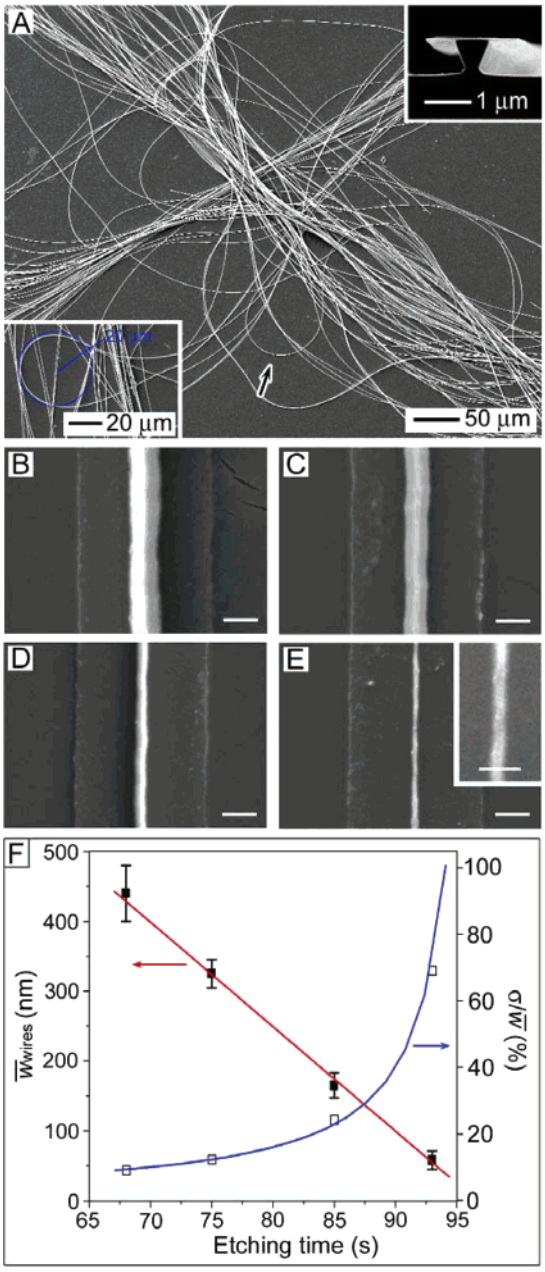

Figure 2. (A) SEM images of long GaAs wires randomly assembled on the mother substrate. The lower inset shows an SEM image of a nanowire with a bend radius less than 20 μm. (B−E) SEM images of individual GaAs wires obtained by etching GaAs wafers with the same mask pattern for different times: (B) 68, (C) 75, (D) 85, and (E) 93 s. The scale bars of (B−E) represent 500 nm. The scale bar of the inset of E represents 200 nm. (F) Dependence of the average width of as-obtained wires ($\bar{w}_{wires}$) and the ratio between width variation (σ) along individual wires and their average width ($\bar{w}$) on the etching time.

density of bonds over the interface is proportional to the number of $-O_nSi(OH)_{4-n}$ group on the PDMS surface, which is highly dependent on the intensity of oxygen plasma and the treatment time.[17] Treatment with a strong plasma for a long time can induce bonding that is too strong to release the wires from PDMS to the desired plastic substrates. Controlled experiments indicate that the PDMS and SiO_2-coated GaAs wafer treated by the plasma generated from O_2 at pressure of 10 mTorr, flow rate of 10 sccm, and power intensity of 10 W (Uniaxis 790, Plasma-Therm Reactive Ion Etching System) for 3 and 60 s, respectively, generated the best results. The interaction between the e-beam evaporated SiO_2 mask layer and GaAs is strong enough to prevent delamination during the transfer process.[18] Peeling the PDMS stamp away from the GaAs substrate after leaving it in contact for ~2 h lifts off all of the wires (step iii). The GaAs wafer after this transfer step can be polished to regenerate a flat surface for another run of wire fabrication (step iv).[19] The combination of wafer polishing with wire fabrication as described above makes it possible to generate a huge number of GaAs wires from a single piece of wafer. For example, one piece of GaAs wafer with diameter of 10 cm and thickness of 450 μm (commercially available from American Xtal Technology) can generate enough wires (~2.2 billion wires with widths of ~400 nm and lengths of 100 μm) to densely cover the entire surface of a plastic substrate with an area of 1.76 m^2 if one cycle of anisotropic etching and polishing consumes 2 μm GaAs in thickness (typical of the results described here).[20]

Exposing the PDMS stamp with bonded GaAs wires to ambient environment for 1 day or by rinsing it with ethanol reconstitutes the PDMS surface to its native, hydrophobic status.[21] The hydrophobic property prevents the PDMS from strongly interacting with adhesives that are normally hydrophilic. When the recovered PDMS stamp is placed against an adhesive layer (e.g., PU obtained from Nolarland products, Cranbury, NJ) spin-coated onto a plastic substrate (e.g., PET of ~175 μm in thickness, Mylar film, Southwall Technologies, Palo Alto, CA), only the GaAs wires/SiO_2 mask stripes are wettable to the adhesive. The thickness of the PU layer can be varied from 1 to tens of microns by controlling the spin speed. Illuminating the sample with an ultraviolet lamp (Model B 100 AP, Black-Ray, Upland, CA) for 1 h cures the PU layer and forms a strong bond between the cured PU and the GaAs wires and SiO_2 mask stripes and between the cured PU and the underlying PET sheet (step v).[22] Peeling away the PDMS stamp leaves the GaAs wires and SiO_2 stripes embedded in the matrix of cured PU with preservation of order and crystallographic orientation similar to those of wires prior to lift-off (step vi). The separation of SiO_2 from PDMS stamp is enabled by two possible effects: (i) moderate adhesion strength associated with sparse siloxane bonds at the interface between PDMS and SiO_2 which might further weaken during the process of reconstituting PMDS surface; and (ii) an ultrathin layer of SiO_2 (with thickness of several nanometers) that remains on the PDMS after cohesive failure of the SiO_2, which is amorphous and possibly incompact and fragile. Immersing the plastic sheet in a solution of buffered oxide etchant (BOE, NH_4F (40 wt %): HF (49 wt %) = 10:1) for 15 min removes the SiO_2 mask stripes, leaving the clean (100) top surfaces of the GaAs nanowires (step vii) facing out.

This simple "top down" approach to the fabrication and dry printing of GaAs wire arrays offers many advantages. For example, the geometries (i.e., length and width) of the wires and their spatial organization can be defined by the initial lithographic step to satisfy the design of the desired

electronic or optical end application. The transfer printing technique can generate yield as high as 100% with preservation of the patterns defined by the lithography. The well oriented crystallographic facets of the transferred wires (i.e., the top (100) surface) on plastic substrates provide an extremely flat top surface (similar to that of original wafer) for device fabrication. Furthermore, the SiO_2 mask stripes prevent the top surfaces of GaAs wires from becoming contaminated by organics (e.g., PDMS and PU) and solvents used in the processing. Embedding the GaAs wires in cured PU prevents them from moving, especially when the plastic substrates are bent or twisted. PU and PET are only examples; other adhesives (e.g., NEA 155, another product from Norland) and plastic sheets (e.g., Kapton polyimide film) can be used. Repetitive application of wire fabrication followed by wafer polishing steps enables cost-effective use of the bulk wafers.

Unlike "bottom up" approaches, the "top down" process can generate GaAs nanowires with uniform lengths from several microns up to tens of centimeters (i.e., the diameter of original wafers). Figure 2A shows an SEM image of free-standing GaAs nanowires with widths of ~400 nm and lengths of 2 cm which were randomly assembled on the mother wafer. The long nanowires formed curved structures during the drying process, indicating the high degree of flexibility that is afforded by their narrow widths.[23] As shown in the lower inset of Figure 2A, the circled nanowire has a bend radius as small as ~20 μm, implying that nanowires with width of ~400 nm could withstand strain of ~1.3%.[24] The upper inset gives an SEM image of the cross section before a nanowire lift off, clearly showing the formation of inverse mesa and undercutting from anisotropic etching.

The width of the GaAs wires could be controlled by changing the width of SiO_2 mask lines as well as the etching time. Widths between hundreds of microns and tens of nanometers are possible. Controlling etching time provided an easy way to generate nanowires from SiO_2 patterns with micron widths. Figures 2B−E show SEM images of individual wires obtained by etching the GaAs wafer patterned with 2 μm wide SiO_2 lines. The wires were transferred to a PDMS surface using the procedures described above to measure precisely the average width of their top surfaces (referred to as $\bar{w}_{wires}$). The dependence of $\bar{w}_{wires}$ on etching time is plotted in Figure 2F, which indicates that GaAs wires with widths down to 50 nm can be obtained in this fashion. The inset of Figure 2E gives a high-magnification SEM image of a high-quality section of such an individual 50-nm nanowire, clearly showing its rough surface and nonuniform width. The linear relationship between width and etching time is consistent with previous studies on etching kinetics of GaAs in $H_3PO_4-H_2O_2-H_2O$ solution, i.e., the etching rate was proportional to etching time when the molar ratio between H_2O_2 and H_3PO_4 ($n_{H_2O_2}/n_{H_3PO_4}$) was larger than 2.3 and the molar fraction of H_2O (r_{H_2O}) was equal to or less than 0.9 ($n_{H_2O_2}/n_{H_3PO_4}$ and r_{H_2O} of the etchant used in our experiments were 7.8 and 0.9, respectively).[25] The statistic results showed that the distributions of the widths of the wires (as determined by averaging along their lengths) was <9% for wires with widths of ~50 nm, which is somewhat narrower than the >14% variation in one type of "bottom up" nanowires that have average widths of ~16.8 nm.[9b] The SEM images shown in Figures 2B−D also show that the triangular cross sections of the wires are preserved during the thinning process, indicating that the etching was still highly anisotropic, even for the free-standing GaAs wires. Close observations of the wires show that there is some roughness on their side walls. Much of this roughness comes directly from the lithographic procedures used to define the SiO_2 mask stripes; some is induced by the misalignment of mask lines and etching itself. It is this roughness that determines the width of smallest continuous wires that we could obtain. As shown in Figure 2F, the ratio between the width variation along individual wires and average wire width ($\sigma/\bar{w}$) was also highly dependent on the etching time. Continuous GaAs nanowires could be prepared when the ratio was less than 100%. The curve indicates that the width of nanowires obtained from our approach could be decreased down to ~40 nm. Nanowires with different average widths exhibited essentially the same width variation along individual wires (i.e., ~40 nm), which was close to the width variation along individual SiO_2 mask lines (i.e., ~36 nm). This comparison confirms that the roughness of wire side walls is mainly initiated by the rough edges of SiO_2 mask stripes, regardless of etching times. It is possible, then, that lithographic procedures that reduce the roughness of the mask stripes will reduce the roughness on the edges of the wires. Although this roughness could have adverse effects for certain device applications, it is important to note that the transfer printing exposes the pristine, ultraflat unetched top surface of the wires for electrical connection and device fabrication on the final substrate (i.e., the PET of Figure 1).

Figure 3 shows images of GaAs wire arrays printed on PDMS and PU/PET substrates. The wires in this case have widths of ~400 nm and lengths of ~100 μm. The corresponding SiO_2 mask lines had widths of 2 μm and lengths of 100 μm oriented along the (0 $\bar{1}$ $\bar{1}$) direction on the (100) GaAs wafers. Panel A is an SEM image taken from an GaAs wire array bonded to a flat PDMS stamp via the SiO_2 mask layer, indicating that the order of wires was preserved. The inset shows the ends of three wires with relatively higher magnification, clearly revealing the breakage at their ends. Peeling the PDMS stamp away from the cured PU left a smooth surface (as smooth as that of the PDMS) with the SiO_2 mask stripes facing out (Figure 3B). As shown in Figure 3C, etching away the SiO_2 layers with BOE exposes the pristine top surfaces of GaAs wires. Figure 3D presents an optical image collected from a PU/PET substrate with embedded GaAs wires, indicating that large-area of wire arrays can be routinely printed on the PU/PET substrate using the approach of Figure 1. GaAs wire arrays with other patterns (e.g., patches consisting of wires with different lengths) could also be transferred to PU/PET substrates (see the Supporting Information). The transfer process could be repeated to print multiple layers of GaAs wire arrays on the same PET substrate by spin-coating a new layer of PU. Figures 3E and F give typical images of samples with double

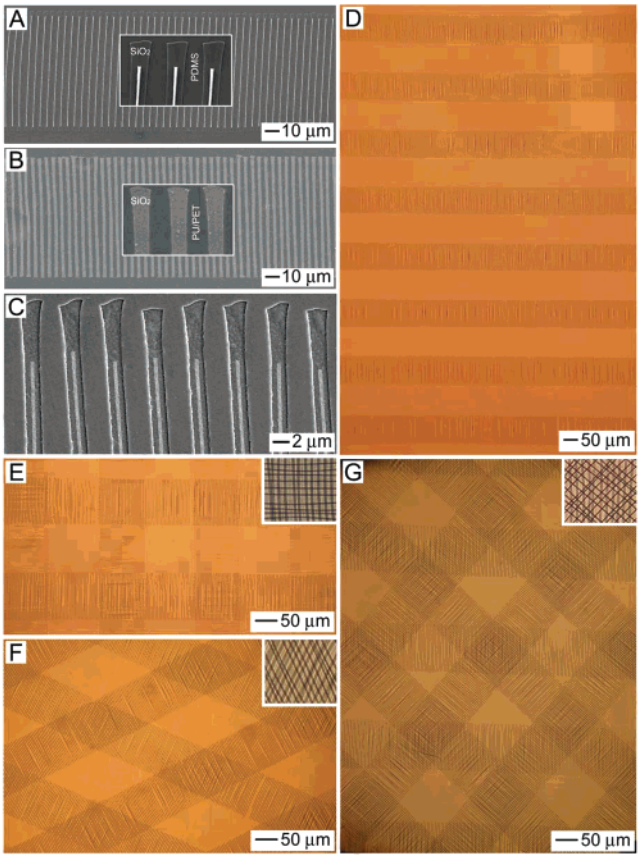

Figure 3. Images of GaAs wire arrays on PDMS stamp and PU/PET sheets. (A) SEM image of a GaAs wire array bonded to PDMS via the SiO_2 stripes. (B, C) SEM images of a GaAs wire array on PU/PET sheets before (B) and after (C) removing the SiO_2 stripes. (D−G) Optical micrographs of GaAs wire arrays on PU/PET sheets with different numbers of layers of wires: (D) single layer; (E) double layers with cross angle of ∼90°; (F) double layers with cross angle of ∼45°; (G) triple layers. The insets show high-magnification images of the areas containing multiple layers of GaAs wire array. Wires at different depths focus at different positions.

layers of GaAs wire arrays obtained by rotating the second layer with different angles (∼90° and ∼45° for E and F, respectively) relative to the first layer. PU/PET substrates with three layers of GaAs wire arrays (a typical image shown in Figure 3G) were obtained by repeating the printing process on samples shown in Figures 3E and F. The thickness of the PU layer, which can be controlled by tuning the spin speed, controls the spacing between the wire arrays. This type of multilayer capability does not, of course, require any form of epitaxial growth, and the PU insulates the arrays in different levels. This fabrication capability could be useful for various applications.

The wire fabrication and printing technique can be used to generate wire arrays of other semiconductor materials on plastic substrates by using suitable anisotropic etchants. For example, InP wires with triangular cross sections can be fabricated by etching the (100) InP wafer with SiO_2 mask lines along the (0 $\bar{1}$ $\bar{1}$) direction in a 1% (v/v) methanol solution of Br_2.[26] Figure 4 shows SEM images of an InP wire array on PMDS and PU/PET substrates. These wires were fabricated from an InP wafer patterned with SiO_2 lines of 50 μm in length and 2 μm in width. The wires had lengths

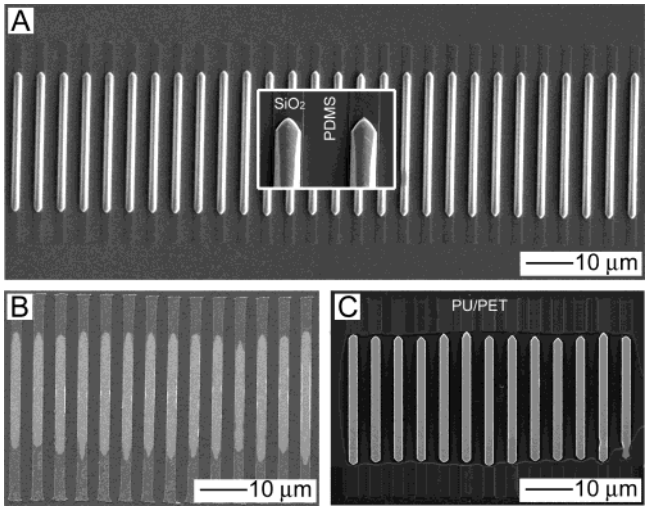

Figure 4. SEM images of InP wire arrays on (A) PDMS stamp and (B, C) PU/PET sheets before (B) and after (C) removing the SiO_2 stripes.

and widths of ∼35 μm and ∼1.7 μm, respectively. The etching behavior of InP in methanol solution of Br_2 was significantly different from that of GaAs in aqueous solution of $H_3PO_4-H_2O_2$ in terms of profile of wire ends and lateral undercutting. For example, the etching disconnected all the ends of InP wires from the mother wafer even with an etch mask that was similar to the one used in fabrication of GaAs wires (Figure 3). The degree of undercutting in InP is less than that in GaAs, implying that InP wires with small widths (less than 500 nm) might be most easily prepared by using narrow SiO_2 stripes rather than by controlling the etching time.

The mechanical flexibility of a simple two-terminal diode device made with GaAs wire arrays (same as those shown in Figure 3 which were fabricated from Si-doped n-GaAs wafer with carrier density of $1.1-5.6 \times 10^{17}$ cm^{-3}) on a PU/PET substrate was evaluated by measuring the electrical properties as a function of bend radius. The structures were fabricated with GaAs wire arrays defined according to the procedures of Figure 1. Photolithography and metal deposition defined on these wires two Schottky contacts made of Ti/Au (5 nm/150 nm) and separated by 10 μm (Figure 5A). Dipping the substrate into a concentrated HCl solution for 10 min removed the native oxide layers on the surfaces of GaAs wires just before deposition of electrodes. Figure 5B shows the current−voltage ($I-V$) curves recorded at different bend radii. These curves all exhibit expected diode characteristics.[6b,27] The small differences among these curves suggest that almost no GaAs nanowires were broken even when the bend radius (R) of substrate was 0.95 cm. The strain on the PET surface in this case was ∼0.92%, which is less than that estimated to exist in the free-standing GaAs nanowire shown in the inset of Figure 2A. These results further confirm that GaAs nanowires fabricated by the "top down" approach are flexible and can be integrated with bendable plastic sheets. We note that the data show that when the substrate was relaxed after first bending, the current was ∼40% smaller than that recorded from the original device before bending (the black curve in Figure 5C). The lack of variation

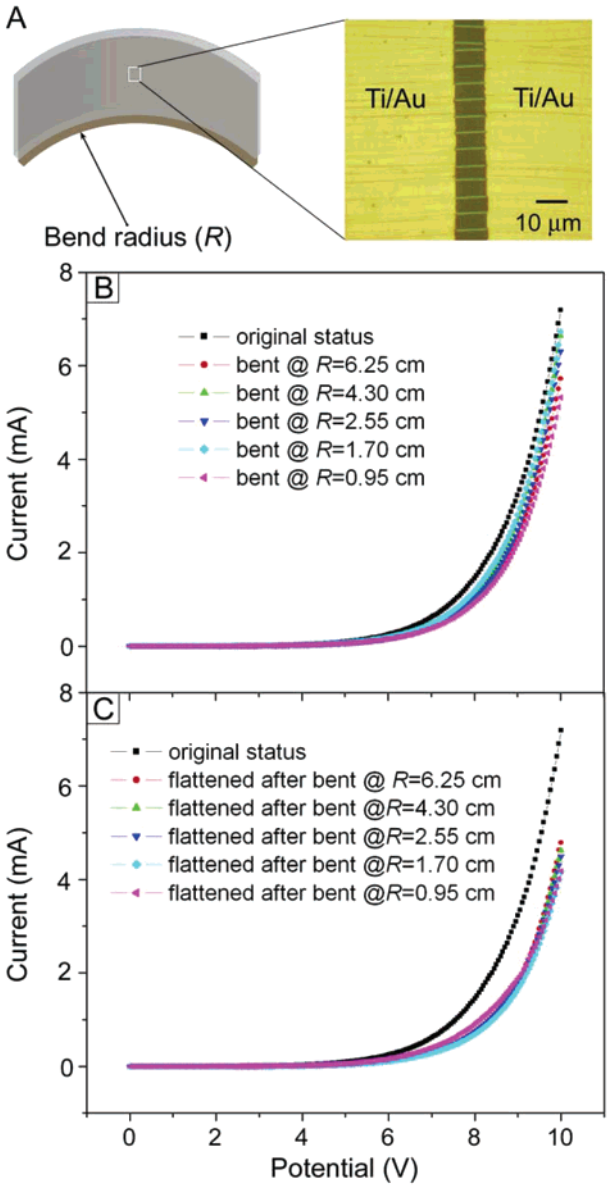

Figure 5. (A) Schematic illustration of the geometry of a bent PU/PET sheet and optical micrograph of Ti/Au electrode pads separated by 10 μm and contacted to an array of GaAs wires. (B) $I-V$ curves obtained at different bend radii. (C) $I-V$ curves recorded when the substrate was returned to its unbent configuration after different bend radii.

in the $I-V$ characteristics with bend radius and with multiple bending/unbending cycles after the first one suggests, however, that the one-time decrease in current might be caused by an initial variation in the properties at the interface between the electrodes and the wires.

In summary, the combined use of traditional photolithography and anisotropic chemical etching with bulk high quality single-crystal wafers of these materials forms an attractive "top down" route to nano- and microwires of GaAs and InP with triangular cross sections. The dimensions of the wires and their organization are defined by the lithography and the etching conditions (e.g., etching time). Precise control over the important parameters, such as the concentration of etchant, solution temperature, ambient light, and sample holder generates reproducible results. The as-obtained wire arrays on the mother substrates can be transfer printed with high fidelity to plastic substrates coated with a thin layer of adhesive in which the wires are embedded. The mother wafer can be reused after polishing, which enables large numbers of wires to be generated from a single wafer. This "dry" printing of "top down" nanowires/microwires represents a new class of transfer process that could offer many advantages over "wet" assembly of "bottom up" nanowires in terms of preservation of order and crystallographic orientation of the wires as well the purity of their active surfaces. Its main disadvantage is that the roughness associated with the lithography (simple contact mode photolithography for the work described here) can limit the uniformity in the widths of the wires. For macroelectronics, where wires wider than 100−200 nm might be useful, the top down approach has many attractive features. The systems of wires on plastic substrates demonstrated here illustrate excellent bendability and significant potential for use in this class of application.

Acknowledgment. We thank T. Banks for help with the process and Dr. Lolita Rotkina for her useful inputs at the very beginning of the project. This work was supported by the DARPA-funded AFRL-managed Macroelectronics Program (FA8650-04-C-7101). Funding is also partially provided by the U.S. Department of Energy under grant DEFG02-91-ER45439.

Supporting Information Available: Figures S1 and S2 showing GaAs wire arrays with alternative patterns (e.g., patches consisting of wires with different lengths) transferred to PU/PET substrates. This material is available free of charge via the Internet at http://pubs.acs.org.

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(14) In a typical run of wire fabrication, a layer of photoresist (AZ 5214, Clariant) was spin coated on the (100) GaAs wafer at the speed of 5000 rpm for 30 s, followed by soft-baking at 100 °C for 60 s. Exposing the wafer to UV light (Suss MJB3 mask aligner) through the proper photomasks defined the patterned lines parallel to the (01$\bar{1}$) direction of GaAs. Developing the exposed wafer in AZ developer (diluted with the same volume of deionized water) for 30 s generated photoresist patterns. A SiO_2 layer with thickness of 100 nm was deposited on the wafer surface via e-beam evaporation. Lift-off of photoresist in acetone left the SiO_2 mask lines (as shown in Figure 1A) on the GaAs wafer. The etchant was prepared by mixing 4 mL of H_3PO_4 (85 wt %), 52 mL H_2O_2 (30 wt %), and 48 mL of deionized water in the ice−water bath. Immersion of GaAs wafer with SiO_2 etch mask in the etchant generated GaAs wires through the anisotropic etching. The resultant sample was rinsed with deionized water and ethanol, dried, and readied for transfer printing.
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(20) The experimental results indicate that the ratio between the etching rates parallel (undercutting) and vertical to the wafer surface was ∼1.05 and the angle between wafer surface and side wall was ∼70°. For the 2 μm wide SiO_2 mask stripes, the GaAs wires could be released from the mother wafer by etching 0.71 μm of GaAs in thickness. If the polishing process thinned the GaAs wafer by an additional 1 μm, then a total 2 μm thick top layer of GaAs generates one layer of GaAs wires. Therefore, the GaAs wire arrays fabricated from one piece of GaAs wafer (10 cm in diameter and 450 μm in thickness) could print a plastic sheet over an area of 255 times larger than that of the mother GaAs wafer.
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NL048835L